8x930A*x* (8x930AD, 8x930AE) SPECIFICATION UPDATE

Release Date: February 1997
Order Number: 272940-008

The 8x930A*x* may contain design defects or errors known as errata. Characterized errata that may cause the 8x930A*x*'s behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-879-4683, Europe 44-0-1793-431-155,
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REVISION HISTORY

Rev. Date	Version	Description
08/30/96	001	This is the new Specification Update document.
09/17/96	002	Added erratum number 9609001. Modified workaround for specification clarification number 001. Added document changes 001 and 002.
09/20/96	003	Added erratum number 9609002.
10/04/96	004	Added errata numbers 9610001, 9610002, 9610003, 9610004. Added A-2 stepping information.
11/13/96	005	Added errata numbers 9611001 and 9611002. Added A-1, A-2, and A-3 stepping information.
12/04/96	006	Added errata numbers 9612001 and 9612002. Corrected the errata table to indicate that five of the errata items were fixed in the A3 stepping: 9609001, 9610001, 9610002, 9610003, and 9610004. Added specification clarification 002. Deleted document changes 001 and 002. The changes were implemented in the datasheet (Order Number 272917-002). Added document changes 003, 004, 005, 006, 007, and 008.
1/8/97	007	Changed status of 9609002, 9610003, 9611002, 9612001 and 9612002 to Fixed. Changed status of 9611001 to No Fix. Added specification changes 001, 002, and 003. Updated specification clarification 002. Added documentation changes 009 and 010. Added information for stepping A-4.
2/5/97	008	Added documentation changes 011, 012, 013, and 014.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
8X930Ax Universal Serial Bus Microcontroller data sheet	272917-002
8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual	272949-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8*x*930A*x* product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings				Page	Status	ERRATA
	A1	A2	A3	A4			
9609001	X	X			9	Fixed	The V_{OH} of the 8*x*930A*x* A-1and A-2 Stepping Does Not Meet the V_{OH} DC Specification Published in the Data Sheet
9609002	X				9	Fixed	8*x*930A*x* Transmit FIFO Underrun During an Isochronous Transfer Does Not Set the TXERR Bit in TXSTAT
9610001	X				9	Fixed	Powerdown Wake-up with External Reset
9610002	X	X			10	Fixed	Occasional Timeout by Function Endpoint
9610003	X	X			10	Fixed	SOF# Pin Pulses When the Microcontroller Leaves Suspend Mode
9610004	X	X			10	Fixed	CRC16 Error on a Data Packet While the Endpoint's Receive FIFO Is Not Ready
9611001	X	X	X	X	10	No Fix	Clearing RXSETUP Bit When Transmit FIFO Data Register Is Not Empty In Low-clock Mode
9611002	X	X			11	Fixed	Low Speed Functionalities Not Guaranteed Below 4.5 V
9612001	X	X	X		12	Fixed	Receive FIFO RXFFRC Error
9612002	X	X			14	Fixed	Low-speed Signaling Marginal on Some Devices

Specification Changes

Number	Steppings				Page	Status	SPECIFICATION CHANGES
	A1	A2	A3	A4			
001			X	X	15	Doc	V_{OH} When I_{OH} = -60 µA
002			X	X	15	Doc	Extended Data Float Option
003			X	X	15	Doc	AC Characteristics Changed

Specification Clarifications

Number	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	A1	A2	A3	A4			
001	X	X			17	Doc	T_{RHDZ1} Timing
002			X	X	20	Doc	Extended Data Float Option

Documentation Changes

Number	Document Revision	Page	Status	DOCUMENTATION CHANGES
003	001	24	Doc	Nonvolatile Memory Verification Port Labeled Incorrectly
004	001	24	Doc	Incorrect Address Given for TXSTAT SFR
005	001	24	Doc	Incorrect Signature Byte
006	001	24	Doc	Power-on Reset Capacitor Value Changed
007	001	24	Doc	SCON SFR's REN Bit Description Incorrect
008	001	24	Doc	Extraneous Footnote in RXCON SFR
009	001	25	Doc	Power Off Flag Voltage Values
010	001	25	Doc	W_{CLK} Description Incorrect
011	001	25	Doc	Configuration Byte Misspelled

Documentation Changes (Continued)

012	001	25	Doc	RTWCE Description Inaccurate
013	001	25	Doc	RL Instruction Misspelled
014	001	25	Doc	Footnote Incorrect in Data Instructions Table

IDENTIFICATION INFORMATION

Markings

Product	Part Number	Stepping	Marking	Comment
8x930Ax Step A1	N80930AD	A1	Q 866	sample QDF
	N80930AE		Q 892	sample QDF
	N83930AE		R xxxx	
8x930Ax Step A2	N80930AD2	A2	no marking	shipping media = tubes
			Q 873	sample QDF
			S L23D	shipping media = tape ‘n’ reel
	N83930AD2		R xxxx	
	N83930AE2		R xxxx	
8x930Ax Step A3	N80930AD3	A3	no marking	ship media = tubes
			Q 873	sample QDF
			S L24E	shipping media = tape ‘n’ reel
	N83930AD3		R xxxx	
	N83930AE3		R xxxx	
8x930Ax Step A4	N80930AD4	A4	no marking	ship media = tubes
			Q 802	sample QDF
			S L26M	shipping media = tape ‘n’ reel
	N83930AD4		R xxxx	
	N83930AE4		R xxxx	

ERRATA

9609001. The Voh of the 8x930Ax A-1and A-2 Stepping Does Not Meet the Voh DC Specification Published in the Data Sheet

PROBLEM: When Port 1, 2, and 3 are in quasi-bidirectional mode, their V_{OH}s are below the target specification as below:

$V_{OH} = V_{CC}$ - 0.8 V (instead of V_{CC} - 0.3 V) @10 µA
$V_{OH} = V_{CC}$ - 1.7 V (instead of V_{CC} - 0.7 V) @30 µA
$V_{OH} = V_{CC}$ - 2.7 V (instead of V_{CC} - 1.5 V) @60 µA

IMPLICATION: The fanout of port 1, 2, and 3 pins are reduced.

WORKAROUND: External buffers can be used to provide the required drive capability needed for interfaces that require more drive than the 8*x*930A*x* can support.

9609002. 8x930Ax Transmit FIFO Underrun During an Isochronous Transfer Does Not Set the TXERR Bit in TXSTAT

PROBLEM: A transmit FIFO underrun in the 8x930Ax during an isochronous transmission does not set the TXERR bit in the TXSTAT special function register (SFR). As a result, the 8x930Ax remains in an infinite IN-token state and responds with an invalid packet identification (PID) of FFH for subsequent IN-tokens.

IMPLICATION: In this state, the 8x930Ax will not respond correctly to host USB commands.

WORKAROUND: Firmware must avoid causing a FIFO underrun. If a FIFO underrun occurs, the firmware can clear the FIFO by setting the TXCLR bit in the TXCON special-function register (SFR) to recover from the infinite IN-token state.

9610001. Powerdown Wake-up with External Reset

PROBLEM: If an external reset is applied to wake up the microcontroller from powerdown mode, the instruction following the powerdown instruction may be executed before the branch to the reset vector occurs.

IMPLICATION: The instruction executed may corrupt a memory location (RAM, registers, or SFRs). This is an issue for systems that require data retention in memory after a reset.

WORKAROUND: Add a no-operation (NOP) instruction after the powerdown instruction to prevent memory corruption.

9610002. Occasional Timeout by Function Endpoint

PROBLEM: The function occasionally times out (stops communicating with the USB host) if the LC bit of the PCON SFR is cleared frequently.

IMPLICATION: The function loses communication with the host occasionally.

WORKAROUND: None. Firmware should check the LC bit and, if it is already clear, firmware should not clear it again.

9610003. SOF# Pin Pulses When the Microcontroller Leaves Suspend Mode

PROBLEM: When a resume or a remote wake-up causes the microcontroller to exit suspend mode, a pulse occurs on the SOF# pin.

IMPLICATION: An invalid SOF# pulse is generated. An application that uses the SOF# pulse may see an invalid SOF# time stamp.

WORKAROUND: None.

9610004. CRC16 Error on a Data Packet While the Endpoint's Receive FIFO Is Not Ready

PROBLEM: When a CRC error on a data packet (from the host) appears on an endpoint while the endpoint's receive FIFO is not ready, subsequent host transactions are ignored. (The "not ready" condition can be the result of a FIFO underrun, a FIFO overflow, or the FIFO's RXFLG register's RXFIF1:0 bits = '11'.) Any IN tokens to that endpoint will time out. The endpoint will respond only to OUT tokens.

IMPLICATION: The endpoint will be unable to respond correctly to subsequent IN tokens.

WORKAROUND: None.

9611001. Clearing RXSETUP Bit When Transmit FIFO Data Register Is Not Empty In Low-clock Mode

PROBLEM: For control endpoint only, when the following conditions below are true, clearing the RXSETUP bit in the RXSTAT Special Function Register (SFR) may put the device in a continuous NAKing state unless the Transmit FIFO data register is flushed (by setting the TXCLR bit in TXCON SFR).

1. LC bit in PCON Special Function Register (SFR) is SET, that is, the CPU core and peripherals is running at 3MHz, specifically for bus-powered applications,
2. The Transmit FIF0 data register is not empty, that is, if the TXFIF1 and TXFIF0 bits in

TXFLG SFR is not 00, and
3. The device is continuously NAKing the host's IN token.

This problem is seen on the USB OHCI system.

IMPLICATION: The device will not be able to respond to host command and, host will time-out and the device will not be served by the host.

LC mode is used during bus enumeration by the bus-powered application, thus the self-powered application will not see this issue if the LC bit is cleared immediately after device reset.

WORKAROUND: To avoid the device going into continuous NAKing state, the transmit FIFO data register must be empty, that is, the TXFIF1:0 bits in the TXFLG special function register (SFR) are "00", when the RXSETUP bit is cleared.

9611002. Low Speed Functionalities Not Guaranteed Below 4.5 V

PROBLEM: The low speed functionalities of the 8*x*930A*x* (A-1 and A-2) are not tested below the operating voltage of 4.5v. Therefore, these low-speed functions are not guaranteed below the operating voltage of 4.5v.

IMPLICATION: The A-1 and A-2 parts cannot be used in low-speed, bus-powered devices where the supply voltage at the parts is less than 4.5 V.

WORKAROUND: No workaround. This is not an issue with full speed operation.

9612001. Receive FIFO RXFFRC Error

PROBLEM: After the RXFFRC bit of the RXCON register is set, the RXFIF1:0 bits in the RXFLG register remain “11”. According to specifications, RXFIF1:0 should immediately decrement when RXFFRC is set. This problem occurs when the following conditions are simultaneously met:

1. The function interface unit (FIU) and serial bus interface engine (SIE) write a byte count to the RXCNTL SFR of endpoint 1’s receive FIFO.
2. The CPU sets the RXFFRC bit for any other endpoint’s receive FIFO (not endpoint 1).
3. The receive FIFO for the endpoint in (2) has RXFIF1:0 bits = “11”.

This problem is most likely to occur in low-clock mode when the device has a high data receive rate (bulk mode) on endpoint 1 and one or more of the other receive FIFO endpoints.

IMPLICATION: When the problem occurs, having RXFIF1:0 remain as “11” will cause firmware to incorrectly assume that there are two packets left in the receive FIFO (in dual packet mode), when in reality there is only one packet left. If firmware attempts to read the non-existent second packet, hardware will set the RXURF bit. When the RXURF bit gets set, the 8*x*930A*x* continues to NAK all OUT packets on the affected FIFO. At this point, the FIFO will be in an unknown state, requiring firmware to reset/clear that FIFO.

WORKAROUND: Additional code must be added to the firmware location(s) where a non-endpoint 1 receive FIFO is released. This code must determine if the RXFIF1:0 bits are “11” before and after setting the RXFFRC bit. If this is true, and if the RXSEQ bit has not been toggled by hardware during this time, then the error has occurred. At this point, firmware must attempt to release the RXFIFO again by re-setting the RXFFRC bit. This process must be repeated until the RXFIFO is successfully released.

Insert a firmware routine similar to the example shown in Figure 1 in your code at the point where you release the receive FIFO for all endpoints except endpoint 1. The code must be duplicated for each endpoint (except endpoint 1), replacing the “x” in the example’s code labels with the endpoint number.

```
;*****************************************************
; RXFFRC Firmware Workaround
;*****************************************************
; Note: Registers 11 through 14 are utilized in this example.
; Please be sure to save and restore these registers as needed.

RELEASE_FIFO_x:
          mov     A,      RXFLG
          mov     R12,    RXFLG         ; before
          mov     R13,    RXSTAT

          setb    RXFFRC

          ; if (RXFLG_BEFORE = RXFLG_AFTER)
          ;  then { continue and check if RXFIF="11" }
          ;  else { setting RXFFRC was successful }
          cjne    A,    RXFLG, REL_FIFOx_OK

          ; if we get here R11 has RXFLG before and after - no
          ; change
          mov     R14,    RXSTAT

          ; if (RXFLG_AFTER = "11")
          ;  then { continue and check RXSEQ data toggle }
          ;  else { jump to REL_FIFOx_OK}
          anl     R11, #11000000b          ; check RXFIF after
          cjne    A,   #11000000b,  REL_FIFOx_OK

          ; RXFIF bits are "11"    RXFLG="C0"
          ; if (RXSEQ_BEFORE = RXSEQ_AFTER)
          ;  then
          ;   { no data toggle - set RXFFRC again }
          ;  else
          ;   { data toggle - OK jump to REL_FIFOx_OK}
          anl     R13, #10000000b
          anl     R14, #10000000b
          cmp     R13,   R14
          jne     REL_FIFOx_OK

          ; FIFO errata condition: RXFIF was "11" before & after; &
          ; RXSTAT didn't change
RELEASE_FIFO_x_AGAIN:
          ljmp    RELEASE_FIFO_x

REL_FIFOx_OK:
```

Figure 1. RXFFRC Firmware Workaround

STATUS: Fixed. Refer to Summary Table of Changes for affected steppings.

9612002. Low-speed Signaling Marginal on Some Devices

PROBLEM: When some A1- and A2-stepping devices are used at low speed (1.5 Mbps), the signals driven out of the transceiver (D_{P0} and D_{M0}) may have longer rise and fall times. As cable length increases, rise and fall times increase, and the crossover point between D_{P0} and D_{M0} decreases. As this crossover point decreases, the data is less likely to be interpreted correctly by the host PC.

IMPLICATION: This problem will cause the host to not recognize signals sent by the device. The host will then terminate communication with the device.

WORKAROUND: There is no workaround, although screening samples may eliminate those devices that exhibit marginal low-speed signaling.

SPECIFICATION CHANGES

001. Voh When Ioh = -60 µA

ITEM: The V_{OH} specification given in the DC Characteristics section of the *8X930Ax Universal Serial Bus Microcontroller Datasheet* is changed to V_{OH} = {min} V_{CC} – 1.7 V when I_{OH} = -60 µA.

002 Extended Data Float Option

ITEM: Default timings and extended data float timings for the A3 and A4 steppings of the 8*x*930A*x* are provided in Table 3 on page 21 and Table 4 on page 23.

003 AC Characteristics Changed

ITEM: AC characteristics have changed for the A3 and A4 steppings of the 8*x*930A*x* in "Compatibility Mode." The differences between the new characteristics and the AC characteristics for the A2 stepping are summarized in Table 1.

Table 1. Summary of 8*x*930A*x* AC Characteristics Changes

Symbol	Parameter	8*x*930A*x* A2 (ns) (1)	8*x*930A*x* A3/A4 (ns) "Compatibility Mode" (EDF# = 1) (2)
T_{AVLL}	Address Valid after ALE Low	(0.5+M) T_{CLK} – 15 [Min]	(0.5+M) T_{CLK} – 13 [Min]
T_{LLAX}	Address Hold after ALE Low	4 [Min] (3)	10 [Min]
T_{WLWH}	WR# Pulse Width	(1+N) T_{CLK} – 12 [Min]	(1+N) T_{CLK} – 10 [Min]
T_{LLRL}	ALE Low to RD# or PSEN# Low	8 [Min]	10 [Min]
T_{LHAX}	ALE High to Address Hold	(1+M) T_{CLK} – 43 [Min]	(1+M) T_{CLK} – 27 [Min]

NOTES:

1. Worst-case numbers based on silicon data collected to date.
2. Device configured with default data float timing for fast memory interface
3. At 50° C, T_{LLAX} is 8 ns.
4. Typical value is 0 ns.

Table 1. Summary of 8*x*930A*x* AC Characteristics Changes (Continued)

Symbol	Parameter	8*x*930A*x* A2 (ns) (1)	8*x*930A*x* A3/A4 (ns) "Compatibility Mode" (EDF# = 1) (2)
T_{RLDV}	RD# or PSEN# Low to Valid Data/Instruction In	(1+N) T_{CLK} – 33 [Max]	(1+N) T_{CLK} – 30 [Max]
T_{RLAZ}	RD# or PSEN# Low to Address Float	0 [Max]	3 [Max] (4)
T_{RHDZ2}	Data Float After PSEN# or RD# High	T_{CLK} [Max]	T_{CLK} +10 [Max]
T_{RHLH2}	RD# or PSEN# High to ALE High (Data)	T_{CLK} [Min]	T_{CLK} +10 [Min]
T_{WHLH}	WR# High to ALE High	T_{CLK} + 5 [Min]	T_{CLK} +10 [Min]
T_{AVDV2}	Address (Demuxed) to Valid Data/Instruction In	(2+M+N) T_{CLK} – 48 [Max]	(2+M+N) T_{CLK} – 38 [Max]
T_{AVRL}	Address Valid to RD# or PSEN# Low	(1+M) T_{CLK} – 43 [Min]	(1+M) T_{CLK} – 40 [Min]
T_{AVWL1}	Address (Muxed) Valid to WR# Low	(1+M) T_{CLK} – 43 [Min]	(1+M) T_{CLK} – 40 [Min]

NOTES:

1. Worst-case numbers based on silicon data collected to date.
2. Device configured with default data float timing for fast memory interface
3. At 50° C, T_{LLAX} is 8 ns.
4. Typical value is 0 ns.

SPECIFICATION CLARIFICATIONS

001. Trhdz1 Timing

PROBLEM: The T_{RHDZ1} (Instruction Float After RD#/PSEN# High) specification on the 8*x*930A*x* when operating at 12 MHz is 10 ns. However, a slow memory device such as an EPROM typically takes approximately 30 – 90 ns to float its output. (This specification, generically called T_{PHZ}, may vary depending on the memory type and manufacturer.) Figure 2 and Figure 3 illustrate the T_{RHDZ1} timing.

The difference between the T_{RHDZ1} and T_{PHZ} specifications causes contention on the data bus (P0 in nonpage page, P2 in page mode). The 8X930A*x* begins to drive the address for the next bus cycle while the memory device is still driving data from the previous bus cycle.

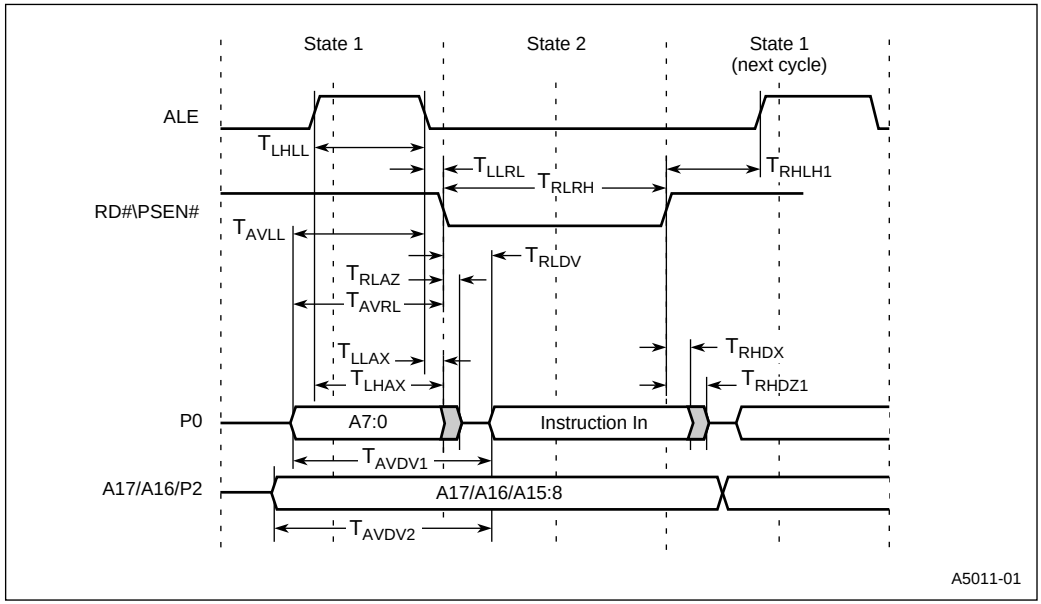

Figure 2. External Code Fetch, Nonpage Mode

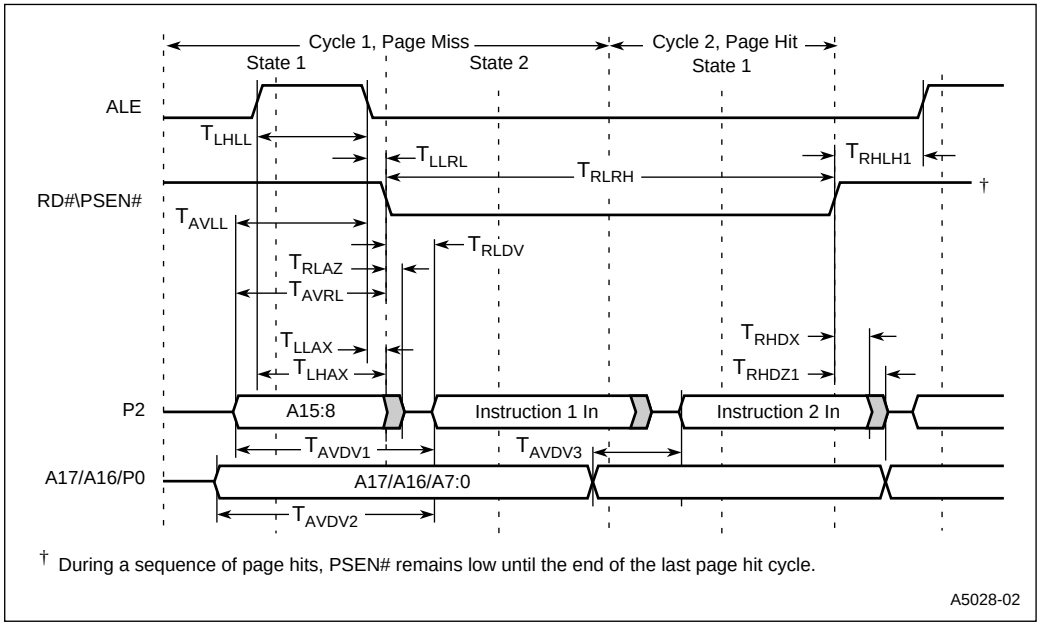

Figure 3. External Code Fetch, Page Mode

To prevent this contention, designers can use a buffer to isolate the output of the memory device from the data bus (port 0 or port 2) of the 8*x*930A*x*. This will prevent the memory device from driving the data bus during the critical period after T_{RHDZ1} expires. We suggest a buffer such as the 74F541 octal, three-state line driver shown in Figure 4.

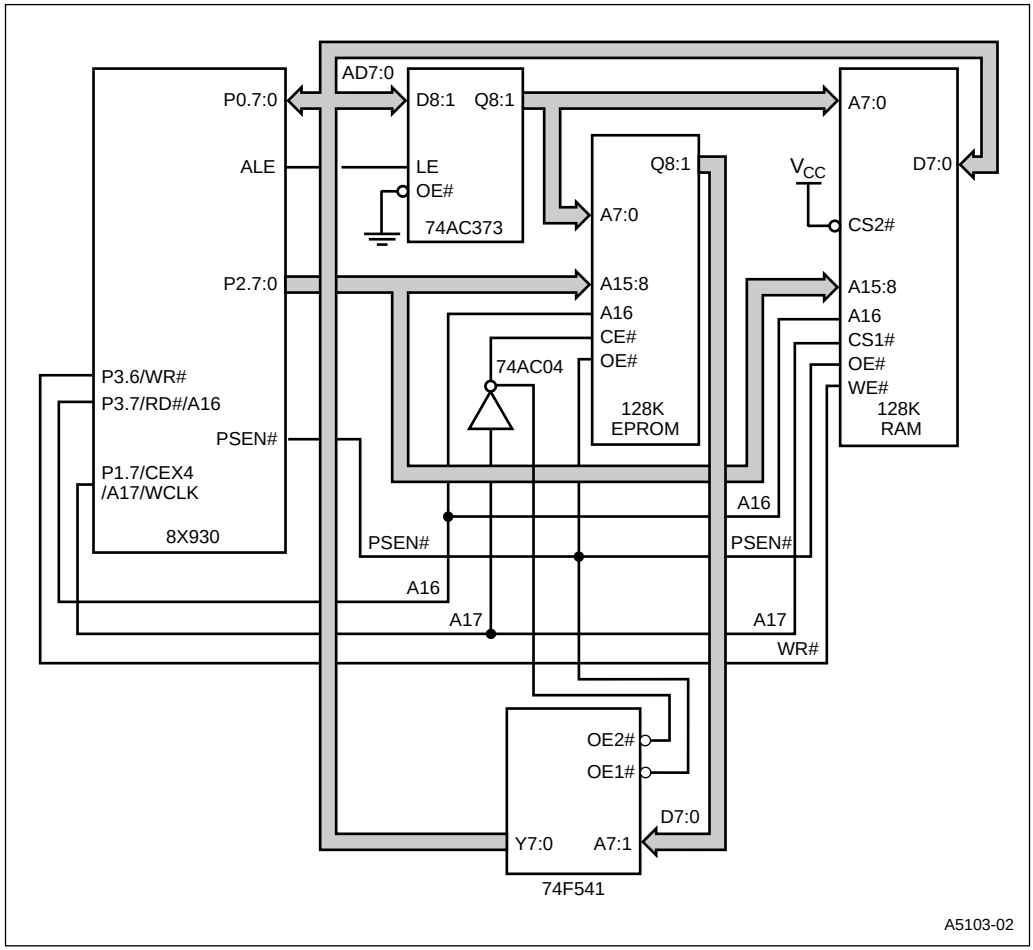

Figure 4. Example Bus Contention Solution for 8X930Ax (Nonpage Mode)

Figure 4 illustrates the connections of an 8X930Ax configured for nonpage mode with EPROM and RAM in external memory. If your system uses a different configuration, your circuit will be different from the example. The 74F541 is enabled to pass data from the EPROM to the 8X930Ax (port 0) when OE1# and OE2# are active. Table 2 is a truth table for the 74F541.

Table 2. Truth Table for 74F541

Inputs			Outputs
OE1#	**OE2#**	**A7:1**	**Y7:1**
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

During a read, PSEN# turns the buffer on (OE1# and OE2# are active), connecting the EPROM's output to the 8X930Ax's port 0.

When PSEN# goes high after a read, OE1# and OE2# are deasserted, and the buffer's output switches to the high-impedance state in approximately 9.5 ns (T_{PHZ} for a typical 74F541; the value may vary from one manufacturer to another). Thus, contention on the data bus is prevented. This or a similar hardware solution is recommended for 8X930Ax designs in which memory devices do not meet the T_{RHDZ1} timing specification.

002. Extended Data Float Option

PROBLEM: The T_{RHDZ1} (Instruction Float After RD#/PSEN# High) specification on the 8*x*930A*x* when operating at 12 MHz is 10 ns. However, a slow memory device such as an EPROM typically takes approximately 30 – 90 ns to float its output. (This specification, generically called T_{PHZ}, may vary depending on the memory type and manufacturer.)

IMPLICATION: The difference between the T_{RHDZ1} and T_{PHZ} specifications causes contention on the data bus (P0 in nonpage mode, P2 in page mode). The 8*x*930A*x* begins to drive the address for the next bus cycle while the memory device is still driving data from the previous bus cycle.

WORKAROUND: In addition to the workaround involving the use of tristate buffers, as described in Specification Clarification 001, Intel has modified the 8*x*930A*x* to provide another solution.

In the A-3 stepping of the 8*x*930A*x*, Intel has added an option that allows system designers to increase the value of T_{RHDZ1}. This option is controlled by bit 3 of configuration byte UCONFIG1. This new bit is called the extended data float bit (EDF#). When EDF# is set (1), the controller behaves according to the existing specifications. When EDF# is cleared (0), extended data float timings are in effect and new bus timing specifications apply to the 8*x*930A*x*. The affected parameters are shown in Table 3 and Table 4.

Table 3. 8*x*930A*x* Default and Extended Data Float Timings

Symbol	Parameter	Default Data Float Timing (EDF# =1) "Compatibility Mode" (ns) (1) (2) (4) (5)	Extended Data Float Timing (EDF#=0) "Increased T_{RHDZ1} mode" (ns) (1) (3) (4) (5)
T_{LLAX}	Address Hold after ALE Low	10 [Min]	20 [Min]
T_{RLRH}	RD# or PSEN# Pulse Width	(1+N) T_{CLK} – 10 [Min]	(1+N) T_{CLK} – 32 [Min]
T_{WLWH}	WR# Pulse Width	(1+N) T_{CLK} – 10 [Min]	(1+N) T_{CLK} – 32 [Min]
T_{LLRL}	ALE Low to RD# or PSEN# Low	10 [Min]	20 [Min]
T_{LHAX}	ALE High to Address Hold	(1+M) T_{CLK} – 27 [Min]	(0.5+M) T_{CLK} + 15 [Min]
T_{RLDV}	RD# or PSEN# Low to Valid Data/Instruction In	(1+N) T_{CLK} – 30 [Max]	(1+N) T_{CLK} – 50 [Max]
T_{RHDZ1}	Instruct. Float after PSEN# or RD# High	10 [Max]	(0.5)T_{CLK} – 5 [Max]
T_{RHDZ2}	Data Float After PSEN# or RD# High	T_{CLK} + 10 [Max]	1.5 T_{CLK} – 5 [Max]

NOTES:

1. Worst-case numbers based on silicon data collected to date.
2. Device configured with default data float timing for fast memory interface
3. Device configured with extended data float timing for slow memory interface.
4. Values listed in this table are for F_{CLK} = 12 MHz. For F_{CLK} = 6 MHz, T_{CLK} will double to equal 166.6 ns.
5. M = 0,1 is the extended ALE state; N = 0,1,2,3 is the RD#/PSEN#/WR# wait state.

Table 3. 8*x*930A*x* Default and Extended Data Float Timings (Continued)

Symbol	Parameter	Default Data Float Timing (EDF# =1) "Compatibility Mode" (ns) (1) (2) (4) (5)	Extended Data Float Timing (EDF#=0) "Increased T_{RHDZ1} mode" (ns) (1) (3) (4) (5)
T_{RHLH1}	RD# or PSEN# High to ALE High (Instruction)	10 [Min]	0.5 T_{CLK} – 7 [Min]
T_{RHLH2}	RD# or PSEN# High to ALE High (Data)	T_{CLK} +10 [Min]	1.5 T_{CLK} – 7 [Min]
T_{WHLH}	WR# High to ALE High	T_{CLK} + 10 [Min]	1.5 T_{CLK} – 7 [Min]
T_{AVDV1}	Address (Muxed) Valid to Valid Data/Instruction In	(2+M+N) T_{CLK} – 60 [Max]	(1.5+M+N) T_{CLK} – 28 [Max]
T_{AVRL}	Address Valid to RD# or PSEN# Low	(1+M) T_{CLK} – 40 [Min]	(0.5+M) T_{CLK} + 10 [Min]
T_{AVWL1}	Address (Muxed) Valid to WR# Low	(1+M) T_{CLK} – 40 [Min]	(0.5+M) T_{CLK} + 10 [Min]
T_{AVWL2}	Address (Demuxed) Valid to WR# Low	(1+M) T_{CLK} – 17 [Min]	(1+M) T_{CLK} + 10 [Min]

NOTES:

1. Worst-case numbers based on silicon data collected to date.
2. Device configured with default data float timing for fast memory interface
3. Device configured with extended data float timing for slow memory interface.
4. Values listed in this table are for F_{CLK} = 12 MHz. For F_{CLK} = 6 MHz, T_{CLK} will double to equal 166.6 ns.
5. M = 0,1 is the extended ALE state; N = 0,1,2,3 is the RD#/PSEN#/WR# wait state.

Table 4. 8*x*930A*x* Real-time Wait AC Timing Specifications

Symbol	Parameter	F_{CLK} Variable (ns) Default Data Float Timing (EDF# =1) "Compatibility Mode"			F_{CLK} Variable (ns) Extended Data Float Timing (EDF#=0) "Increased T_{RHDZ1} mode"		
		Min	Typ	Max	Min	Typ	Max
T_{RLYV}	RD# or PSEN# Low to Wait Setup	0		0.5 T_{CLK} – 13	0		0.5 T_{CLK} – 35
T_{WLYV}	WR# Low to Wait Setup	0		0.5 T_{CLK} – 13			0.5 T_{CLK} – 35

DOCUMENTATION CHANGES

003. Nonvolatile Memory Verification Port Labeled Incorrectly

ITEM: The illustration “Setup for Verifying Nonvolatile Memory” (Figure 17-1 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User’s Manual*) incorrectly depicts P1 as the Verify Modes port. The correct port for Verify Modes is P0.

004. Incorrect Address Given for TXSTAT SFR

ITEM: The USB Function SFR tables (Tables 3-11 and C-7) in the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User’s Manual* give an incorrect address for the TXSTAT SFR. The correct address is S:F2H.

005. Incorrect Signature Byte

ITEM: Section 17-6 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User’s Manual* mention a signature byte at 61H. There is no signature byte at 61H.

006. Power-on Reset Capacitor Value Changed

ITEM: Figure 14-1 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User’s Manual* depict a 1 µF power-on reset capacitor. The correct value for this capacitor is 0.3 µF.

007. SCON SFR’s REN Bit Description Incorrect

ITEM: The description for the Serial Port Control SFR’s REN bit (SCON.4), as given in Figure 13-2 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User’s Manual*, is incorrect. The text should say ”To enable reception, set this bit. To disable reception, clear this bit.”

The SCON SFR also appears in Appendix C of the same manual.

008. Extraneous Footnote in RXCON SFR

ITEM: The dagger footnote (†) does not apply to the RXFFRC and RXISO bits in the RXCON SFR, as shown in Figure 7-15 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User’s Manual*. The RXCON SFR also appears in Appendix C. Note that the dagger footnote *does* apply to the SFR’s ADVWM and REVWP bits.

009. Power Off Flag Voltage Values

ITEM: Section 15.2.2 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual* states that "the hardware sets the Power Off Flag (POF) in PCON when V_{CC} rises from < 3 V to > 3 V to indicate that on-chip volatile memory is indeterminate...since for V_{CC} < 3 V data may have been lost or some logic may have malfunctioned." The voltage value should be 3.5 V for all references, not 3 V.

010. Wclk Description Incorrect

ITEM: The description for the wait clock output (W_{CLK}) given in Table 16-1 and Table B-2 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual* is incorrect. Instead of "When enabled, the W_{CLK} output produces a square wave signal with a period of one-half the oscillator frequency," the final sentence should read "When enabled, the W_{CLK} output produces a square wave signal with a period of T_{CLK}."

011. Configuration Byte Misspelled

ITEM: On page 16-11 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual*, in the third paragraph of the note, UNCONFIG0 should be UCONFIG0.

012. RTWCE Description Inaccurate

ITEM: On page 16-11 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual*, in Figure 16-11, the description of RTWCE should say "with RTWE set, setting RTWCE will enable the WAIT clock....." In other words, setting RTWCE alone will not enable the wait clock, both bits must be set.

013. RL Instruction Misspelled

ITEM: On page A-4 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual*, the 'A' should be moved to the second line for RLA and RLCA. The instruction is RL A not RLA.

014. Footnote Incorrect in Data Instructions Table

ITEM: On page A-6 of the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual*, Note 2 for Table A-9 is not correct. ORL, ANL, and XRL all have one instruction that uses DRk (see page A-38 for an example).