ECR #: 22
Title: IDSEL and an A.G.P. Compliant master
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Impact: Clarification
Spec Version: A.G.P. 1.0

Summary: Because of loading on the AD bus, IDSEL needs to be connected internally to AD16 when operating as an A.G.P. compliant device.

Background: The rev 1.0 interface specification states that IDSEL is connected to AD16 externally to the component.

Change Current Specification as shown:

Add new section.

Configuration of an A.G.P. Compliant Master

Initialization of an A.G.P. compliant device is done via the configuration mechanism defined by the PCI Bus specification and this specification does not define a new mechanism. An A.G.P. compliant master is composed of a PCI compliant target interface and an A.G.P. compliant master interface. (Optionally the device can also include a PCI compliant master interface when required.) The PCI compliant target interface follows the PCI bus specification. This requires the device to respond to a PCI configuration transaction when a configuration command (read or write) is decoded and **AD1** and **AD0** are both "0" and the device's **IDSEL** is asserted. Since **IDSEL** is not a signal in the A.G.P. connector it must be connected to **AD16** at the component. The designer of the A.G.P. compliant master must be careful as to how this connection is made. It must be connected internally for A.G.P. operation while it must be connected externally for PCI operation. The next two sections will describe how this connection must be made based on the targeted market of the device

Device for A.G.P. only operation

When the device is designed for exclusive operation on the A.G.P. interface the device does not have an external **IDSEL** pin. In this implementation the device asserts **DEVSEL#** when the bus command is Configuration (read or write), **AD16** is a '1' while **AD1** and **AD0** are '00'. Under all other conditions the device's configuration space has not been selected and the device does not assert **DEVSEL#** to claim the access. System software will scan all configuration spaces supported by asserting a different **AD** signal between **AD16** and **AD31** while performing a PCI configuration read or write command. A device located on that segment can only assert **DEVSEL#** for a single configuration space which is uniquely identified by having its **IDSEL** asserted when **AD1-0** are "00". The exception is for a multi-function device that has bit 7 of the header type field set. In this case, the different functions are selected based on the function number decoded (**AD10-AD8**). See the PCI Bus specification for more details.

Device for PCI and A.G.P. operation

When a device is designed to be used on both A.G.P. and PCI bus segments, then the device needs to have two modes of operation. When in the A.G.P. mode it generates **DEVSEL#** as described in the A.G.P. only implementation. When used in a PCI mode of operation, the device must provide an external **IDSEL** that is connected to one of the **AD** signals. Which **AD** signal it is connected to is determined by the system designer and NOT by the component designer. In this case, the device must be "strapped" to indicate which mode it is operating in. Note: that besides how **DEVSEL#** is generated during configuration accesses, the device must also know the strength in which it drives its output buffers. Note: A.G.P. requires only half the strength of a PCI buffer, since A.G.P. is a point to point connection and not a bus environment like PCI.