ECR #: 10
Title: Remove 50 ohm loads from test specs
Release Date: 12/11/96
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary:

The test and measurement section (4.2.2.3) should be revised to reflect the point to point nature of A.G.P. by removing requirement for 50Ω loading and by adding slew rate, flight time and skew waveforms

Change Current Specification as shown:

Change the AC specs to be 10 pF capacitive loads only and all measurements be made to VREF as VTEST. Section 4.2.2.3 to be changed as attached.

4.2.2.3 Measurement and Test Conditions

This section gives the measurement and test conditions for design. Production test systems and boards have different capacitive loads than specified below. It is the responsibility of the manufacturer to correlate those systems to the reference points given in this section.

The reference point for all AC timings measurements is 0.4VCC. The output capacitive loading (C_L) for all maximum timings is 10pf and for all minimum timings is 0 pF.

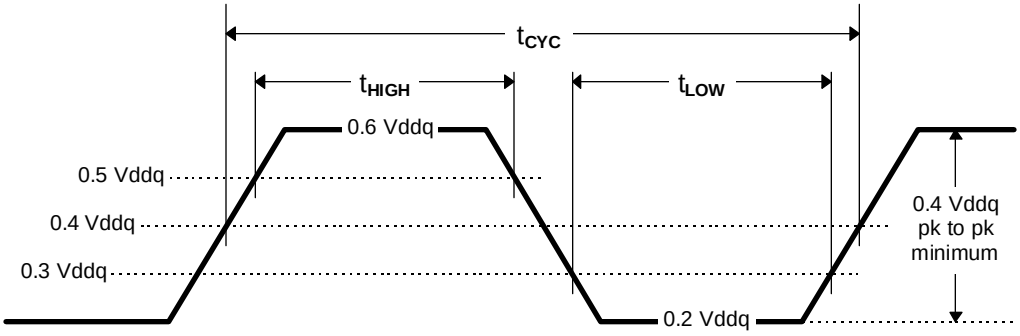

Figure 0-1: Clock Input Measurement Conditions

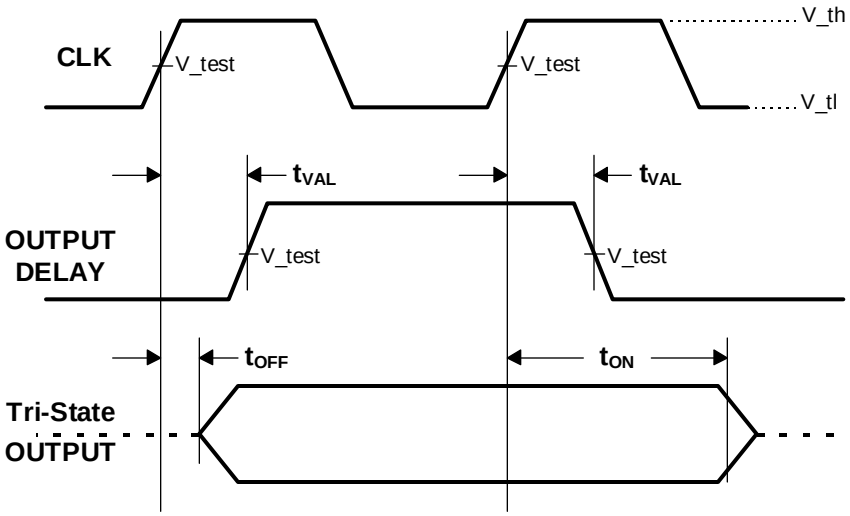

Figure 0-2: Output Timing Measurement Conditions

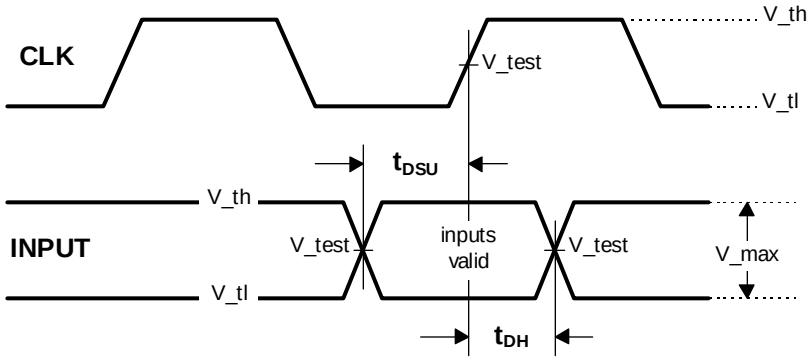

Figure 0-3: Input Timing Measurement Conditions

Table 0-1: Measurement and Test Condition Parameters

Symbol	Signaling Levels	Units	Notes
V_{th}	0.6Vddq	V	1
V_{tl}	0.2Vddq	V	1
V_{test}	0.4Vddq	V	
V_{max}	0.4Vddq	V	1
Input Signal Slew Rate	1.5-4.0	V/ns	2

NOTES:

1. The test is done with 0.1*Vddq of overdrive. V_{max} specifies the maximum peak-to-peak waveform allowed for testing input timing.

2. Outputs will be characterized and measured at the package pin with the load shown in Figure 0-4. Input signal slew rate will be measured between $0.2V_{ddq}$ and $0.6V_{ddq}$.

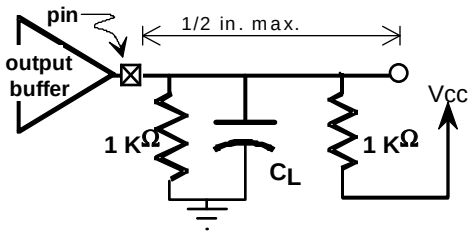

Figure 0-4: Load for testing output timings

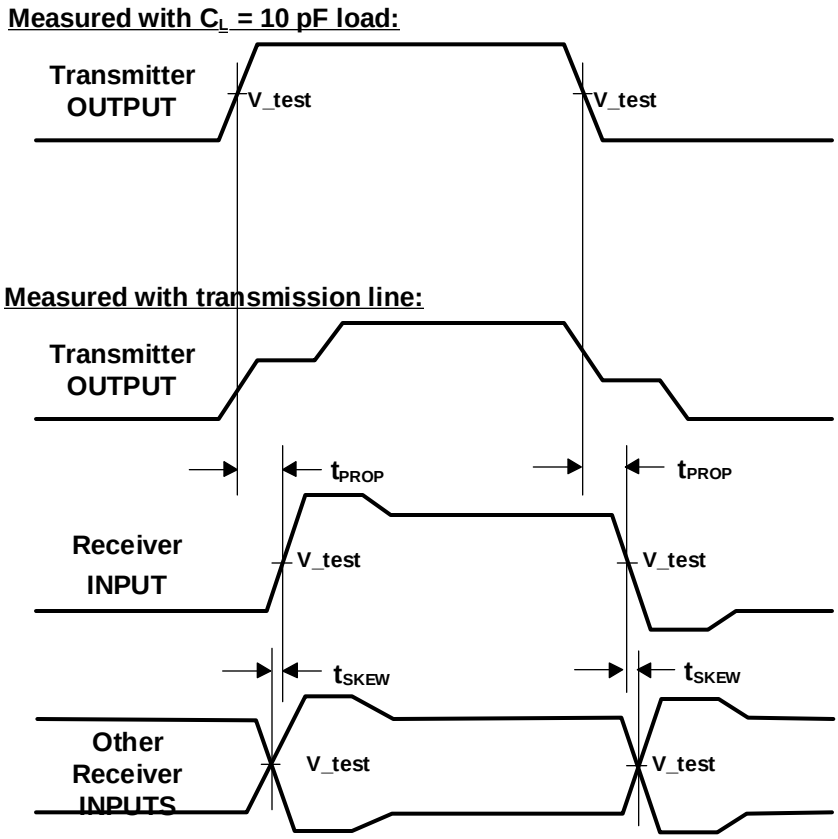

Figure 0-5: Flight Time and Skew Measurement