

# Audio Codec '97 Technical FAQ Sheet

revision 1.0



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## **Introduction**

Primary goals of the Audio Codec '97 (AC '97) specification are to widely enable high quality audio and promote a baseline set of audio capabilities which will support emerging PC applications cost effectively for high volume market segment platforms in 1997.

The AC '97 interoperability goals benefit IHVs, OEMs, and the end user. AC '97 Controller / Codec interoperability is desirable for baseline solutions, as is adherence to the 48- and 64-pin package recommendations whenever possible.

However, vendors are encouraged to exceed the baseline recommendations by adding value via differentiated solutions. In many cases this can be achieved in a scaleable manner which is interoperable with baseline implementations. In other cases differentiated solutions may require that the OEM select a matched Controller / Codec pair sourced by the same vendor, or two vendors who have partnered in developing a complete solution. Combined Audio/Telephony is a good example of a matched Controller / Codec solution which may even require that the vendor deviate from the 48- and 64-pin package recommendations.

As more and more of the PC audio resources migrate to the digital domain the differentiation emphasis may continue to shift towards the digital Controller. The intent of AC '97 is to create an architecture with scaleability of features in the digital Controller and scalability of quality (and analog features) in the analog Codec.

The following are responses and clarifications based on questions that the Intel Audio team have received:

Q1. Will there be an AC '97 logo certification program?

A1. No, there will be no AC '97 logo program. The Intel Audio team will continue to focus on assisting the industry in meeting the primary goals (quality/capabilities/cost). The team also supports industry wide efforts to validate interoperability and establish quality standards.

## **Sample Rates and Sample Rate Conversion (SRC)**

AC '97 encourages the migration of multi-stream functionality into the digital realm. The adoption of a fixed sample rate Codec and the requirements for SRC and mixing in the digital Controller were major architectural considerations, and carefully evaluated. These capabilities support the industry wide trend of migrating all audio towards digital. Several of the 1-chip multimedia audio Codec vendors are already shipping fixed rate Sigma-Delta DACs and ADCs and utilizing digital SRC and mixing, and many others are developing this capability.

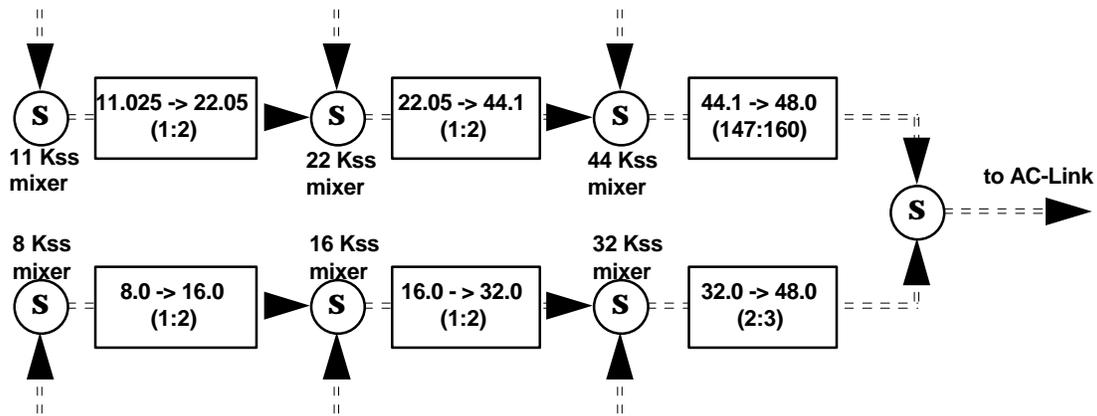
Q2. Why did the AC '97 Codec adopt the fixed 48KHz sample rate instead of 44.1KHz ?

A2. With the introduction of the DVD-ROM drive the PC audio subsystem needs to support MPEG movie audio with encoded AC-3 and/or MPEG audio soundtracks at 48 KHz sample rate. It is more attractive to upsample all audio material to the 48 KHz rate than to compromise the bandwidth or quality of these audio soundtracks.

Q3. Doesn't high quality digital sample rate conversion add cost to the audio solution?

A3. A PCI based audio Codec needs to support multiple concurrent input and output sources at diverse sample rates, such as PCM, MIDI, CD digital audio streamed from memory, or decoded AC-3 streamed from memory. The choice is either implement multiple DACs and ADCs running at various sample rates followed by analog mixing, or perform digital sample rate conversion and mixing at one common rate. The digital solution is preferred based on quality, cost and flexibility of implementation.

The following is one possible implementation of digital SRC and mixing which can efficiently support an arbitrary number of digital PCM output sources at any of the standard PC sample rates with a minimum of dedicated SRC hardware resource:



### **AC '97 mixer, analog functions, input and outputs**

The AC '97 specification defines a baseline set of interoperable features for the analog mixer, and Codec. Vendors are free to differentiate themselves by adding capabilities beyond the baseline interoperable solution. Such enhancements may require that the OEM select a matched Controller / Codec pair sourced by the same vendor, or two vendors who have partnered in developing a complete solution.

Q4. Can the mixer input be an independent mix instead of a mux?

A4. The Working Group which generated the AC '97 Component Specification carefully considered mux vs. mix and concluded that virtually all usage models can be supported at lower cost via the mux. Vendors are encouraged to implement the 3rd ADC input channel as a way of adding additional flexibility to the input capabilities.

However, it is possible to use the vendor specific control registers to design a fully symmetric analog input mixer which, for interoperability purposes, can also appear to a generic AC '97 Controller as the baseline AC '97 mixer input mux.

Q5. What about supporting 2 independent mics? What about supporting 2 phone lines?

A5. Nothing prevents vendors from differentiating themselves by adding capabilities above the baseline interoperable solution. The vendor specific control registers can be used for this purpose.

Q6. What is the intended function of the PC\_BEEP input, and how should it be implemented?

A6. PC\_BEEP supports motherboard AC '97 Controller /Codec implementations. The intention of routing PC\_BEEP through the Codec analog mixer is to eliminate the requirement for an onboard speaker or piezoelectric device by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC\_BEEP signal needs to reach the output jack at all times, with or without the audio driver's support.

The primary sources of PC\_BEEP are:

- Power On Self Test (POST) error reporting (at system boot time before the audio driver has loaded)
- Windows system alerts (when no audio driver is installed)
- DOS applications which make BIOS calls or write directly to IO port 61 (independent of audio driver)

The AC '97 Component Specification recommends a passive connection between PC\_BEEP and LINE\_OUT\_L/R whenever the AC-link RESET# is held active low. PC\_BEEP for POST error reporting can be guaranteed if the AC '97 Controller holds AC-link RESET# low until after the AC '97 Controller is first accessed (by BIOS) following a cold reset. It may also be possible to enable the passive PC\_BEEP connection whenever the AC '97 mixer is in powerdown state (this is an option left up to the IHV).

The following is one possible power on sequence which supports the PC\_BEEP passive connection:

1. Cold reset	1. AC '97 Controller powers up.
2. BIOS performs POST	2. During this stage the AC '97 Controller holds AC-link RESET# active low, and the PC_BEEP passive connection is enabled.
3. BIOS begins PnP	3. BIOS PnP configures AC '97 Controller legacy & native PCI audio device(s). AC '97 Controller de-asserts RESET# and begins Codec initiation sequence. PC_BEEP switchover from passive to active begins. BIOS completes AC '97 Controller PnP config and moves on w/o waiting for AC '97 Codec to be fully powered on.
4. BIOS completes PnP	4. AC '97 Codec completes power up (0-500ms later), AC '97 Controller completes legacy device initialization, including unmuting the AC '97 mixer master volume. Sound Blaster is now ready.
5. DOS prompt	5. PC_BEEP through AC '97 Codec mixer enabled.
6. Win 95 loads	6. Win 95 AC '97 driver loads and initializes native PCI device(s).

Care should be taken to avoid the introduction of a pop when powering the mixer up or down, and that the above described functionality for the passive PC\_BEEP connection does not jeopardize the audio quality of LINE\_OUT (i.e. introduce unwanted noise). Support for this feature should not come at the expense of the AC '97 quality goals, the OEM has the option to route PC\_BEEP external to the AC '97 Codec.

Q7. What are the 3D stereo enhancement parameters 'center' and 'depth'.

A7. The 3D control register defines 2 16-step controls for the 3D Stereo Enhancement function. These controls can be used to support center and depth, but can also be used generically. If the lower 8-bits of the 3D control register are non-zero, then the depth/generic1 control is fixed, otherwise it is variable. If the upper 8-bits of the 3D control register are non-zero, then center/generic2 control is fixed, otherwise it is variable.

### **Optional modem DAC and ADC support**

Modem functionality has not been defined as an interoperable solution, and therefore requires a matched Controller / Codec pair sourced by the same vendor, or two vendors who have partnered in developing a complete solution. This essentially gives the vendor(s) a high degree of freedom to implement the combined audio/telephony solution.

Q8. Is it required to support the optional modem DAC and ADC at 48 KHz?

A8. Either a fixed rate or variable rate approach may be taken.

From a quality standpoint, where audio is running concurrently with modem operation, it may be desirable to avoid introducing interference within the AC '97 Codec by running the modem DAC and ADC at 48 KHz and resampling on the digital side to the desired modem rate. If the fixed 48 KHz rate approach is taken, it may be advantageous to band limit the modem ADC input to ~3300 Hz within the analog section in order to simplify the digital resampling task. Similar optimizations may apply to the DAC output.

However, the fixed rate acquisition with digital resampling may introduce undesirable delays or complexity. Through use of the modem rate register, AC-link slot tag bits and implementation of re-timing FIFOs on one or both sides of the AC-link it should be possible to acquire and transfer data at other rates.

Q9. Does use of the modem rate register require that all rates be supported?

A9. The modem rate register can be used in whatever manner the vendor wishes, or it can be ignored.

Q10. What is the function of the modem HxAp and HxAn pins?

A10. AC '97 allocates up to 6 pins for implementation of the hybrid interface. There is no requirement for a vendor to implement a 6-pin hybrid interface. There are several 6-pin hybrid interface designs on the market which incorporate HxAp and HxAn for hybrid matching/balancing. If all 6 pins are not used the remaining pins can be used in a vendor specific manner, such as general purpose I/O for hook switch control etc.

### **AC '97 Codec package**

Standardizing the AC '97 pins and package was done to enable development time/cost savings for an OEM. The standard package allows an OEM the ability to reuse the tuned analog portion of a PCB layout across multiple designs, including designs utilizing different vendors' AC '97 Codecs.

Q11. What about an AC '97 implementation in a non-standard package?

A11. Once the AC '97 Codec moves to a non-standard package, design reusability is lost. However, as stated earlier in this FAQ, there is no logo certification program for AC '97 compliance. The IHVs are free to decide for themselves what is in their best interest when implementing products.

Q12. What is the function of the "reserved" pins on the 64-pin QFP package?

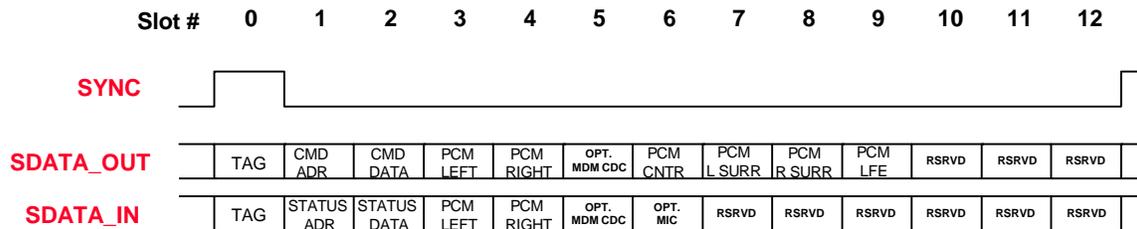
A12. The 4 reserved pins on the 64-pin package are provided to ensure package and layout interoperability for 6 channels of output in the future. A 6-channel AC '97 Codec might be desirable inside a Family Room PC, on an external USB or IEEE 1394 based "dongle", or embedded within the

consumer audio equipment.. The preference is that these pins be reserved for future outputs, but vendors may choose to use the 4 pins for proprietary extensions.

For those who wish to implement 6-channels of audio output, the following pinout and AC-link time slot assignments are suggested:

64-pin package

- pin 41 LINE\_OUT\_LFE
- pin 42 LINE\_OUT\_SURROUND\_R
- pin 43 LINE\_OUT\_SURROUND\_L
- pin 44 LINE\_OUT\_CENTER
- pin 45 LINE\_OUT\_L
- pin 46 LINE\_OUT\_R



**AC-link operation and architectural headroom**

Q13. What are the recommendations regarding multi-channel output?

A13. The price sensitive volume market segment PC will continue to ship with 2-channel audio. The base AC '97 architecture reflects this with its 2 baseline DACs. AC-link defines 2 PCM time slots in the base definition to accommodate 2-channel digital playback for the digital mix of all digital audio sources in the system. There are many promising techniques for enhancing 2 speaker audio, such as 3D stereo enhancement, cross-talk cancellation, and binaural Head Related Transfer Function (HRTF) processing for 3D positional audio or "virtual" speakers.

Support for multi-channel output should be carefully targeted to the output system. In addition to the traditional analog PC speakers, we may soon see digital speakers which accept USB, S/P-DIF or IEEE 1394. Existing consumer equipment accepts stereo (or Pro Logic encoded) analog audio via RCA jacks. Newer A/V receivers also accept stereo digital audio (or encoded AC-3) via S/P-DIF. The latest generation of "AC-3 Ready" A/V receivers have preamps which accept decoded AC-3 via 6 RCA jacks or a DB25 connector (endorsed by Dolby Labs and Lucasfilm). In the near future we may also see USB or IEEE 1394 connections built into A/V equipment.

Sufficient headroom is provided in the AC-link architecture to allow for the addition of 4 more digital output channels (slots) if there is a demand for it. Additionally, as mentioned earlier, the 64 pin package for AC '97 sets aside 4 reserved pins for this purpose.

Q14. How are 18 or 20-bit samples handled?

A14. The standard AC '97 DAC and ADC resolutions are defined as 16 bits. 18 or 20 bit resolution implementations are optional. The audio driver for an "enhanced" AC '97 Controller can determine the implemented DAC and ADC resolution after it has been loaded by reading the AC '97 Codec's "Reset Register" which is located at 0x00. If, for example, the driver has determined that the implemented DAC resolution is 16 bits yet the Controller supports 18 or 20 bit sample streams for playback, the Controller

can either dither the sample streams down to 16 bits or pass the stream “as is”. Since all AC-link data time slots carry 20 bits, the non-dithered approach will result in the least significant bits which overrun the DAC width being dropped. For this reason dithering may be an attractive feature for the Controller that supports greater than 16 bit sample streams.

Q15. How are inconsistent or partially valid frames handled (esp. command slots)?

A15. All AC-link data slots (arguments) required for completely specifying an operation within a given audio frame should be treated as a single “atomic” slot. Only the first tag bit of the atomic slot encountered in the frame determines the validity for the entire atomic slot. For example in an audio output frame, if the tag bit for the Command Address Port is valid then the next bit which corresponds to the Command Data Port should be assumed to be valid as well, regardless of the actual state of the tag bit. If the operation was decoded on the Codec side to be a register read operation, then the Command Data Port data would be discarded. If the operation was determined to be a register write operation, it is not unreasonable to assume that an AC '97 Controller that initiates a write operation on the AC-link will always follow the Command Address Port DIRECTLY with its associated Command Data Port within the same frame.

For interoperability sake, and to minimize design complexity, all Command Write and Status Read multi-slot sequences should be treated as single atomic slots.

Q16. What if AC '97 receives an inconsistent frame?

A16. Given the recommended treatment described in the previous question, “inconsistent” frames are precluded by definition

Q17. Should address and data slots always be treated as 'one entity'?

A17. Yes. As recommended above (“atomic” slot).

Q18. Is it possible to have a 'split transaction' in which a given frame has only valid write Address data, and its write data value is specified in a succeeding frame with valid write Data slot only?

A18. Given the recommended treatment described earlier the answer is no. Aside from the added complexity if this were to be allowed it should not be unreasonable to require the AC '97 Controller to ONLY initiate an AC-link transaction when it can be fully specified within the same frame.

Q19. If one of the 'Valid' time slots is missing, should AC '97 just ignore the command or do its best to 'guess' the intent of the companion Controller possibly using surrounding frames' command slot contents?

A19. We did not have split transactions in mind, the 2 slot structure is just for size-sake. As stated earlier these multi-slot command/argument pairs should be treated as “atomic slots” and handled as described earlier.

Q20. Since there's no mention of Status Read Access time or latency, we assume the immediately following frame contains the content for read request in a frame. Or can it be in a later frame?

A20. We are not requiring that the read requests be completed by the immediately following frame. For some functions this may not be possible. Valid return data for a given input frame is indicated by the tag associated with the Status Address Port being valid. As discussed, the combination of the Status Address and Status Data Ports should be treated as single atomic slot. The data returned within the Status Address Port echoes the register address for which the data in Status Data Port corresponds to. AC '97 Controllers should check the return address. While “out of order” reads are not specified, and “in order” reads are

expected to be the norm, there may be cases where it makes sense to return readily available data out of order.

Q21. 'Vendor ID Register' intent. This register is READ-ONLY and is for interoperability to help an AC '97 Controller identifying AC '97 being connected. This can be used as a cue to activate vendor specific functions in their AC '97 Controller (and in AC '97) Is this correct ?

A21. Yes.

Q22. 'Valid Frame' bit logic implementation.[in an AC '97 Controller]. Is it legal to implement the 'Valid Frame' bit fixed "1", and show the validities of each slots with the corresponding valid bits in TAG slot? Or it must strictly be logical OR of all the valid bits in a frame. Put another way, A frame with its 'Valid Frame' bit "1" and none of the valid bits in TAG a legal frame? Please comment.

A22. Valid Frame = 1 is defined to mean there must be at least one valid slot somewhere within the frame. Implementation of the logical OR is required for interoperability.

Q23. Is there any way to support a multi-point AC-link?

A23. AC-link was designed as a point to point interconnect. However, since it only requires 5 pins to implement AC-link on the digital Controller, it may be possible to design a Controller which supports multiple AC-links and manages one or more AC-link target device at a time. This might be attractive for a mobile solution which includes a docking station.

Supporting multiple *active* AC-links may present a rate adaptation challenge if each AC '97 Codec operates off a independent crystal oscillator source.

Q24: The Intel Legacy Audio on PCI proposal may not be flexible enough to preclude conflicts with, for example, older cards (not even related to audio) that have hardwired IRQ and/or DMA resources. Why don't you believe that more flexibility is warranted?

A24: The Intel team agrees that for reasonable scenarios, such as the one listed above, more flexibility is warranted. Given a motherboard audio (BIOS enumerated) solution, it is felt that fixing the legacy I/O would have negligible exposure since even older non-PnP audio cards have jumper blocks to allow a choice of I/O base addresses. BIOS would reserve the fixed audio I/O on boot and other devices would be required to map around these.

On the other hand, DMA and IRQ resources could more reasonably be applied by other applications (other than just audio), and so therefore we do believe that there is exposure in this area.

A revised proposal will be posted on the AC '97 web page which keeps the fixed I/O resource, but recommends 4 choices for IRQ and DMA resources. The updated Legacy Audio on the PCI Bus white paper details an extended "Legacy Control Register" which comprehends this new flexibility.

This updated Intel proposal is supported by the current revision (rev 0.9) of Microsoft's PC 97 Design Guide for motherboard legacy audio implemented on PCI.

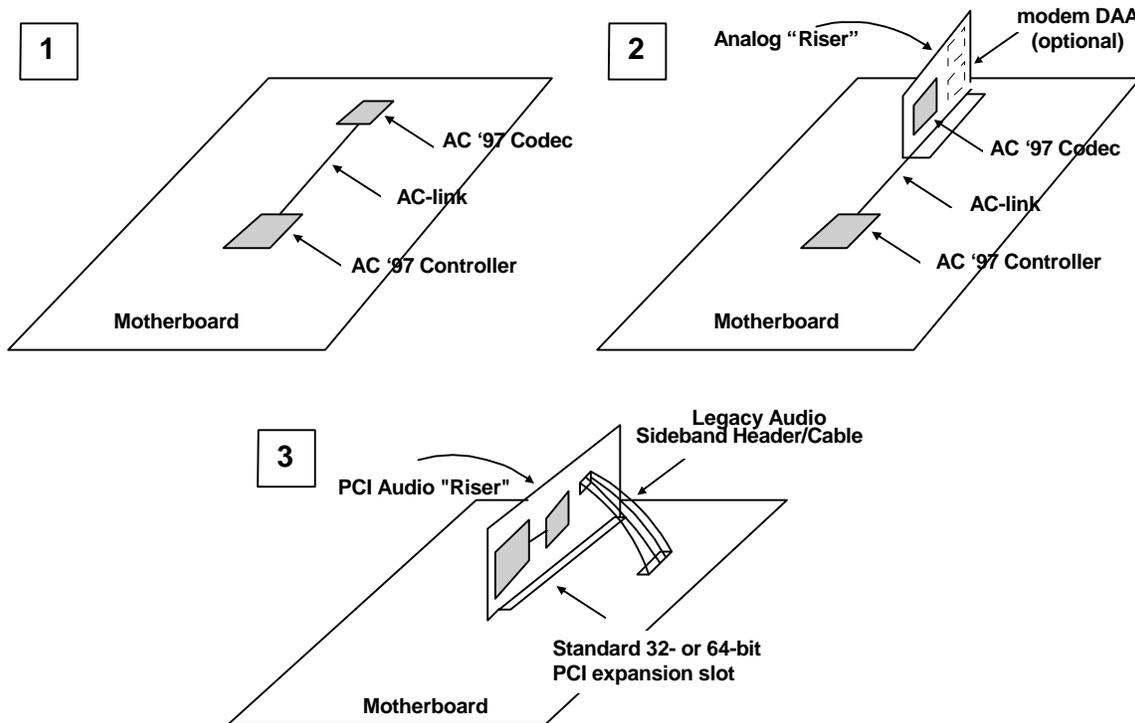
Q25. Does Intel endorse sideband support for modular OEM solutions which support legacy audio devices via PC/PCI or DDMA?

A25. PC/PCI and DDMA hardware mechanisms demand "motherboard aware" implementations due to sideband signaling requirements that cannot be accommodated through the use of either standard ISA or PCI expansion slots. Another reason for this requirement from the software side is the need to have the BIOS enumerate the audio subsystem as a series of system device nodes.

While aftermarket (retail) add-in cards could be problematic, a sideband signaling standard for OEMs and IHVs would enable what is essentially a riser card arrangement for motherboard audio.

Three options for AC '97 Controller and Codec placement are discussed below:

1. Controller down + Codec down (down = on the motherboard)
2. Controller down + "analog riser" with Codec, audio connectors, and optional modem DAA and RJ11
3. Add-in PCI card with Controller, Codec, optional audio/telephony, and/or legacy sideband connector



### Option 1: Fully Motherboard Integrated Solution

The AC '97 Controller and Codec are physically, and logically down on the motherboard.

#### PROs

- Lowest audio/telephony system cost
- Legacy compatibility

#### CONs

- Motherboard attach rate in some cases does not warrant modem down
- FCC certification delays to motherboard intro

IHV's are encouraged to develop scalable, pin compatible AC '97 controllers as well as AC '97 codecs. With an IHV's scalable product family, the OEM can answer the modem down or not business issue by designing one motherboard and scaling up or down based upon the IHV's scalable product offerings.

While this potentially solves both the legacy and audio and audio/telephony scalability issues, the serial delays to OEM product introduction associated with FCC certification remain unresolved.

## **Option 2: AC '97 Codec Riser Solution**

The AC '97 Controller is soldered down on the motherboard, and its AC-link<sup>1</sup> feeds a TBD riser connector for the AC '97 Codec/DAA etc...

### **PROs**

- Legacy compatibility
- Scalability

### **CONs**

- Higher cost than fully motherboard integrated solution

As for option #1 IHVs are encouraged to develop scalable, pin compatible AC '97 controllers as well as AC '97 codecs. With an IHV's scalable product family, the OEM can layout his motherboard for a pin compatible series of scalable controllers, and with a single motherboard can ship a range of products with or without the telephony integration based upon the appropriate controller being matched up with its corresponding Codec riser card.

The OEM can either design their own riser cards, or subcontract the IHV to deliver them to the OEM customer's specifications. In either case the FCC certification process is decoupled from the motherboard design.

## **Option 3: Legacy Header/PCI Bus Add-in/"Riser" Solution**

The OEM provides a "Legacy Header" on the motherboard a that standard form factor PCI add-in card can cable onto with their complementary header. This option brings legacy DMA/IRQ sideband signals over to the standard PCI bus add-in.

With this option the OEM is presented with a maximally scalable platform partitioning, and the IHV can sell their add-in into the retail market segment (without legacy support) as well as the OEM market segment.

In order to enable legacy hardware compatibility the standard form factor PCI bus add-in, when utilizing the legacy header, must be treated as an OEM motherboard subsystem. This OEM targeted product is configured as a riser card conveniently plugged into a standard PCI expansion slot with additional signals provided via the header/cable. The audio subsystem must be enumerated via the motherboard BIOS to enable the legacy compatible hardware.

### **PROs**

- Can be sold into retail and OEM market segments
- Legacy compatibility (OEM only)
- Max. Scalability

### **CONs**

- Legacy compatibility lost in retail versions
- Highest cost option
- Uses a PCI expansion slot

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<sup>1</sup> In addition to other telephony related digital signals, such as ring detect, hook switch control, etc.