



## 8x930Hx UNIVERSAL SERIAL BUS PERIPHERAL CONTROLLER

- **USB Hub with One Upstream, One Internal Downstream, and Three External Downstream Ports**
  - Complete Universal Serial Bus Specification 1.0 Compatibility
  - Serves as both USB Hub and USB Embedded Function (Internal Port)
- **USB Hub**
  - Connectivity Management
  - Downstream Device Connect/Disconnect Detection
  - Power Management, Including Suspend and Resume
  - Bus Fault Detection and Recovery
  - Full and Low Speed Downstream Device Support
- **Output Pin for Port Power Switching**
- **Input Pin for Overcurrent Detection**
- **USB Embedded Function**
  - Supports Isochronous and Non-isochronous Data
- **On-chip USB Transceivers**
- **Serial Bus Interface Engine (SIE)**
  - Packet Decoding/Generation
  - CRC Generation and Checking
  - NRZI Encoding/Decoding and Bit-stuffing
- **Hub FIFO Data Buffers**
  - One Pair of 16-byte Transmit and Receive FIFOs
  - One 1-byte Transmit Register
- **Embedded Function FIFO Data Buffers**
  - Three Pairs of 16-byte Transmit and Receive FIFOs
  - One Pair of Configurable Transmit and Receive FIFOs (1 Kbyte total)
- **Automatic Transmit/Receive FIFO Management**
- **Three USB Interrupt Vectors**
  - Endpoint Done
  - Start of Frame/Hub Endpoint Done
  - Global Suspend/Resume
- **Low Clock Mode**
- **User-selectable Configurations**
  - External Wait State
  - External Address Range
  - Page Mode
- **Real-time Wait Function**
- **256-Kbyte External Code/Data Memory Space**
- **On-chip ROM Options**
  - 0, 8, or 16 Kbytes
- **1024 bytes On-chip Data RAM**
- **Four Input/Output Ports**
- **Standard MCS<sup>®</sup> 51 UART**
- **Power-saving Idle and Powerdown Modes**
- **Register-based MCS 251 Architecture**
- **Code-compatible with MCS 51 and MCS 251 Microcontrollers**
- **12-MHz Crystal Operation**

The 8x930Hx USB peripheral controller is based on the MCS 251 microcontroller. It consists of standard 8XC251Sx peripherals plus a USB module. The USB module provides both USB hub and USB embedded function capabilities. The 8x930Hx supports USB hub functionality, embedded function, suspend/resume modes, isochronous/non-isochronous transfers, and it is fully USB rev 1.0 specification compliant. The USB module contains one internal and three external downstream ports and integrates the USB transceivers, serial bus interface engine (SIE), hub interface unit (HIU), function interface unit (FIU), and transmit/receive FIFOs. The 8x930Hx uses the standard instruction set of the MCS 251 architecture, which is binary code compatible with the MCS 51 architecture.

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1.0 ABOUT THIS DOCUMENT

This data sheet contains advance information about Intel's 8x930Hx Universal Serial Bus peripheral controller, based on the MCS® 251 peripheral controller, which includes a functional overview, mechanical data, targeted electrical specifications (simulated), and bus functional waveforms. A detailed functional description, other than parametric performance, is published in the 8x930Ax, 8x930Hx Universal Serial Bus Micorcontroller User's Manual (272949).

1.2 Electronic Information

We offer a variety of technical and product information through the World Wide Web (see Table 2 for URL) and through FaxBack service which is an on-demand publishing system that sends documents to your fax machine. You can get product announcements, change notifications, product literature, device characteristics, design recommendations, and quality and reliability information 24 hours a day, 7 days a week. Just dial the telephone number and respond to the system prompts.

1.1 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641
1-800-879-4683

Table 1. Related Documentation

Table with 2 columns: Document Title, Order/Contact. Rows include 8x930Ax, 8x930Hx Universal Serial Bus Micorcontroller User's Manual and Universal Serial Bus Specification.

Table 2. Electronic Information

Table with 2 columns: Document Title, Order/Contact. Rows include Intel's World-Wide Web (WWW) Location, Customer Support (US and Canada), FaxBack Service (US and Canada, Europe, worldwide), and Application Bulletin Board Service (up to 14.4-Kbaud line, dedicated 2400-baud line, Europe).

1.3 Product Summary

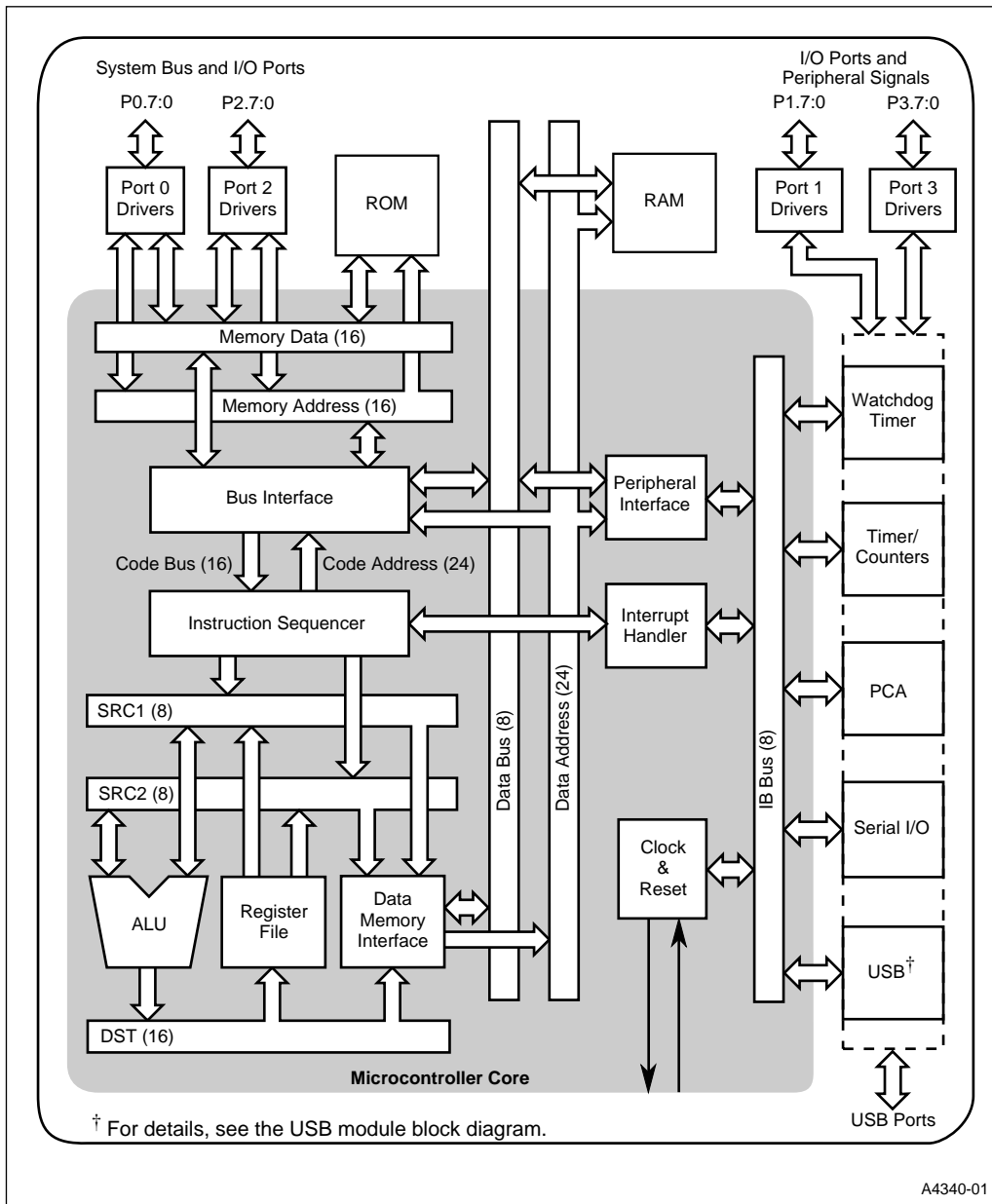


Figure 1. 8x930Hx Block Diagram

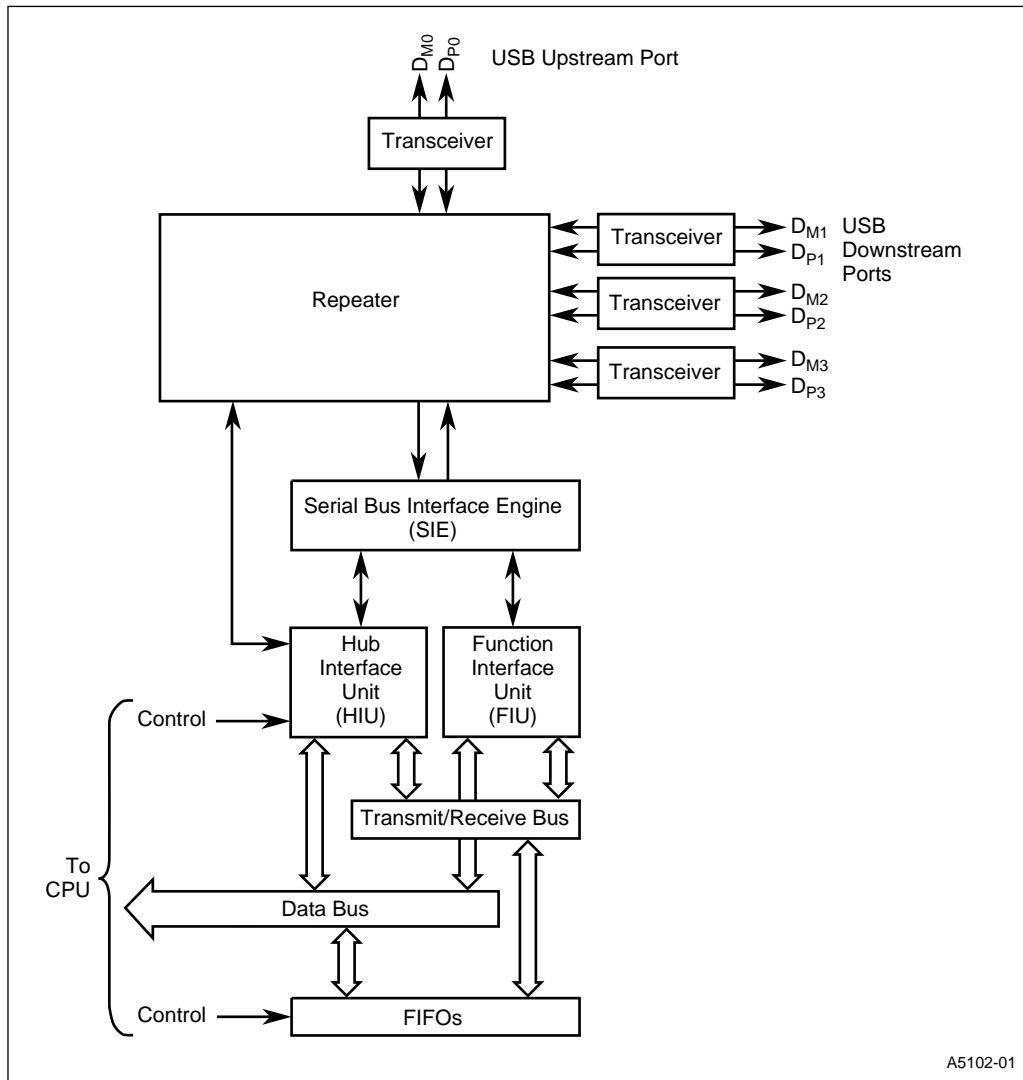


Figure 2. 8x930Hx USB Module Block Diagram



2.0 NOMENCLATURE OVERVIEW

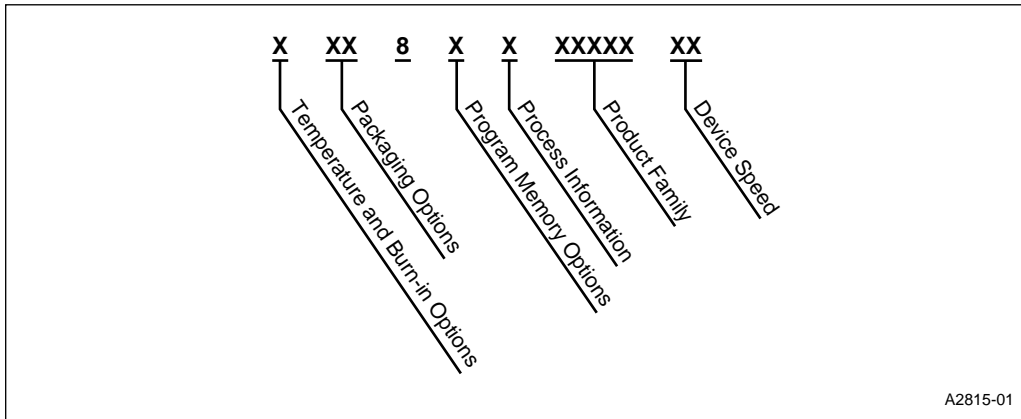


Figure 3. Product Nomenclature

Table 3. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in
Packaging Options	N	Plastic Leaded Chip Carrier (PLCC)
	U	Shrink Dual In-Line Package (SDIP)
Program Memory Options	0	Without ROM
	3	With ROM
Process and Voltage Information	no mark	CHMOS
Product Family	930Hx	Advanced 8-bit microcontroller architecture with on-chip Universal Serial Bus Function peripherals capability
Device Speed	no mark	6 or 12 MHz crystal

Table 4. Proliferation Options

Part Name	ROM Size	RAM Size	Package
N80930HD	0	1024 bytes	68-pin PLCC
N83930HD	8 Kbytes	1024 bytes	68-pin PLCC
N83930HE	16 Kbytes	1024 bytes	68-pin PLCC
U80930HD	0	1024 bytes	68-pin SDIP
U83930HD	8 Kbytes	1024 bytes	68-pin SDIP
U83930HE	16 Kbytes	1024 bytes	68-pin SDIP





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### 3.0 PINOUT

Figure 4 illustrates a diagram of the 8x930Hx PLCC package. Table 5 and Table 7 contain indexes of the pin arrangement. Table 9 contains the signal descriptions for all pins.

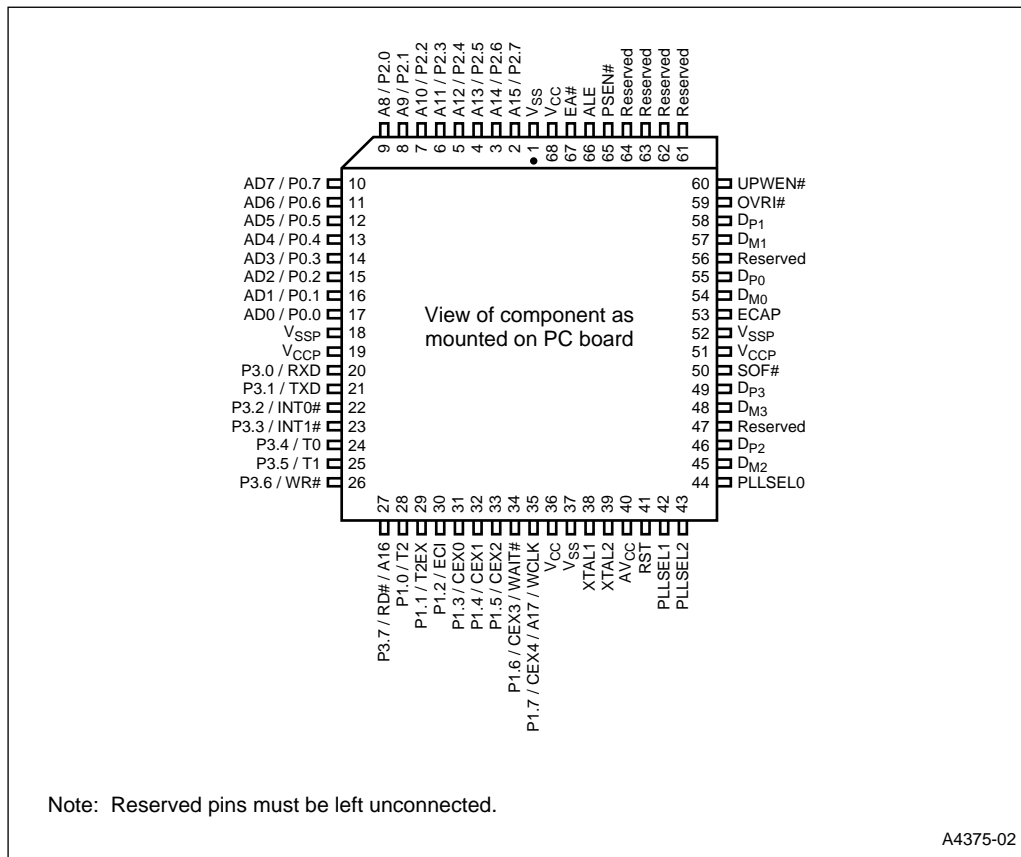


Figure 4. 8x930Hx 68-pin PLCC Package

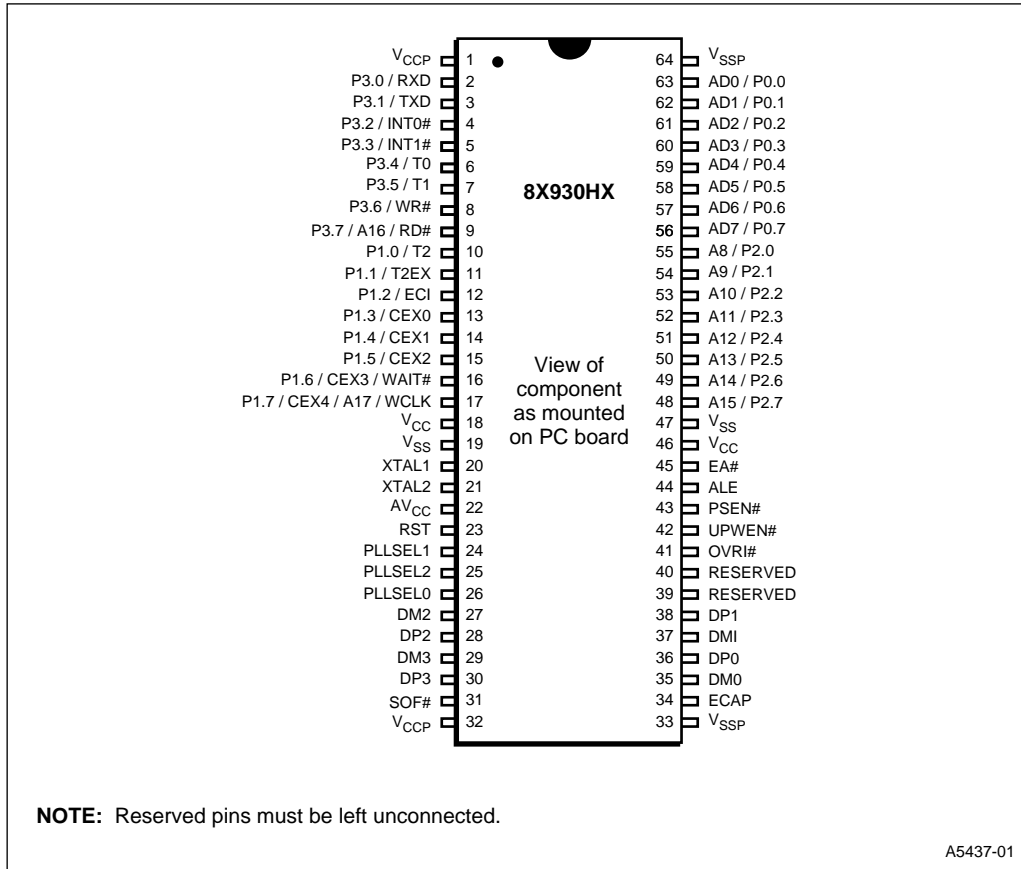


Figure 5. 8x930Hx 64-pin SDIP Package



Table 5. 68-pin PLCC Pin Assignment

Pin	Name	Pin	Name	Pin	Name
1	V <sub>SS</sub>	24	P3.4/T0	47	Reserved
2	A15/P2.7	25	P3.5/T1	48	D <sub>M3</sub>
3	A14/P2.6	26	P3.6/WR#	49	D <sub>P3</sub>
4	A13/P2.5	27	P3.7/RD#/A16	50	SOF#
5	A12/P2.4	28	P1.0/T2	51	V <sub>CCP</sub>
6	A11/P2.3	29	P1.1/T2EX	52	V <sub>SSP</sub>
7	A10/P2.2	30	P1.2/ECI	53	ECAP
8	A9/P2.1	31	P1.3/CEX0	54	D <sub>M0</sub>
9	A8/P2.0	32	P1.4/CEX1	55	D <sub>P0</sub>
10	AD7/P0.7	33	P1.5/CEX2	56	Reserved
11	AD6/P0.6	34	P1.6/CEX3/WAIT#	57	D <sub>M1</sub>
12	AD5/P0.5	35	P1.7/CEX4/A17/WCLK	58	D <sub>P1</sub>
13	AD4/P0.4	36	V <sub>CC</sub>	59	OVRI#
14	AD3/P0.3	37	V <sub>SS</sub>	60	UPWEN#
15	AD2/P0.2	38	XTAL1	61	Reserved
16	AD1/P0.1	39	XTAL2	62	Reserved
17	AD0/P0.0	40	AV <sub>CC</sub>	63	Reserved
18	V <sub>SSP</sub>	41	RST	64	Reserved
19	V <sub>CCP</sub>	42	PLLSEL1	65	PSEN#
20	P3.0/RXD	43	PLLSEL2	66	ALE
21	P3.1/TXD	44	PLLSELO	67	EA#
22	P3.2/INT0#	45	D <sub>M2</sub>	68	V <sub>CC</sub>
23	P3.3/INT1#	46	D <sub>P2</sub>		

Table 6. 64-pin SDIP Pin Assignment

Pin	Name	Pin	Name	Pin	Name
1	V <sub>CCP</sub>	23	RST	45	EA#
2	P3.0/RXD	24	PLLSEL1	46	V <sub>CC</sub>
3	P3.1/TXD	25	PLLSEL2	47	V <sub>SS</sub>
4	P3.2/INT0#	26	PLLSEL0	48	A15/P2.7
5	P3.3/INT1#	27	DM2	49	A14/P2.6
6	P3.4/T0	28	DP2	50	A13/P2.5
7	P3.5/T1	29	DM3	51	A12/P2.4
8	P3.6/WR#	30	DP3	52	A11/P2.3
9	P3.7/A16/RD#	31	SOF#	53	A10/P2.2
10	P1.0/T2	32	V <sub>CCP</sub>	54	A9/P2.1
11	P1.1/T2EX	33	V <sub>SSP</sub>	55	A8/P2.0
12	P1.2/ECI	34	ECAP	56	AD7/P0.7
13	P1.3/CEX0	35	DM0	57	AD6/P0.6
14	P1.4/CEX1	36	DP0	58	AD5/P0.5
15	P1.5/CEX2	37	DM1	59	AD4/P0.4
16	P1.6/CEX3/WAIT#	38	DP1	60	AD3/P0.3
17	P1.7/CEX4/A17/WCLK	39	Reserved	61	AD2/P0.2
18	V <sub>CC</sub>	40	Reserved	62	AD1/P0.1
19	V <sub>SS</sub>	41	OVR1#	63	AD0/P0.0
20	XTAL1	42	UPWEN#	64	V <sub>SSP</sub>
21	XTAL2	43	PSEN#		
22	AVCC	44	ALE		



## 8x930Hx UNIVERSAL SERIAL BUS PERIPHERAL CONTROLLER

Table 7. 68-pin PLCC Signal Assignments Arranged by Functional Category

Address & Data		Input/Output		USB	
Name	Pin	Name	Pin	Name	Pin
AD0/P0.0	17	P1.0/T2	28	PLLSEL0	44
AD1/P0.1	16	P1.1/T2EX	29	PLLSEL1	42
AD2/P0.2	15	P1.2/ECI	30	PLLSEL2	43
AD3/P0.3	14	P1.3/CEX0	31	D <sub>M0</sub>	54
AD4/P0.4	13	P1.4/CEX1	32	D <sub>P0</sub>	55
AD5/P0.5	12	P1.5/CEX2	33	D <sub>M1</sub>	57
AD6/P0.6	11	P1.6/CEX3/WAIT#	34	D <sub>P1</sub>	58
AD7/P0.7	10	P1.7/CEX4/A17/WCLK	35	D <sub>M2</sub>	45
A8/P2.0	9	P3.0/RXD	20	D <sub>P2</sub>	46
A9/P2.1	8	P3.1/TXD	21	D <sub>M3</sub>	48
A10/P2.2	7	P3.2/INT0#	22	D <sub>P3</sub>	49
A11/P2.3	6	P3.3/INT1#	23	SOF#	50
A12/P2.4	5	P3.4/T0	24	ECAP	53
A13/P2.5	4	P3.5/T1	25	OVR!#	59
A14/P2.6	3	P3.6/WR#	26	UPWEN#	60
A15/P2.7	2	P3.7/RD#/A16	27		
P3.7/RD#/A16	27				
P1.7/CEX4/A17/WCLK	35				

Processor Control		Power & Ground		Bus Control & Status	
Name	Pin	Name	Pin	Name	Pin
P3.2/INT0#	22	V <sub>CC</sub>	36, 68	P3.6/WR#	26
P3.3/INT1#	23	V <sub>CCP</sub>	19, 51	P3.7/RD#/A16	27
RST	41	A <sub>V</sub> <sub>CC</sub>	40	PSEN#	65
XTAL1	38	V <sub>SS</sub>	1, 37	ALE	66
XTAL2	39	V <sub>SSP</sub>	18, 52	EA#	67



Table 8. 64-pin SDIP Signal Assignments Arranged by Functional Category

Address & Data		Input/Output		USB	
Name	Pin	Name	Pin	Name	Pin
AD0/P0.0	63	P1.0/T2	10	PLLSEL0	26
AD1/P0.1	62	P1.1/T2EX	11	PLLSEL1	24
AD2/P0.2	61	P1.2/ECI	12	PLLSEL2	25
AD3/P0.3	60	P1.3/CEX0	13	D <sub>M0</sub>	35
AD4/P0.4	59	P1.4/CEX1	14	D <sub>P0</sub>	36
AD5/P0.5	58	P1.5/CEX2	15	D <sub>M1</sub>	37
AD6/P0.6	57	P1.6/CEX3/WAIT#	16	D <sub>P1</sub>	38
AD7/P0.7	56	P1.7/CEX4/A17/WCLK	17	D <sub>M2</sub>	27
A8/P2.0	55	P3.0/RXD	2	D <sub>P2</sub>	28
A9/P2.1	54	P3.1/TXD	3	D <sub>M3</sub>	29
A10/P2.2	53	P3.2/INT0#	4	D <sub>P3</sub>	30
A11/P2.3	52	P3.3/INT1#	5	SOF#	31
A12/P2.4	51	P3.4/T0	6	ECAP	34
A13/P2.5	50	P3.5/T1	7	OVR!#	41
A14/P2.6	49	P3.6/WR#	8	UPWEN#	42
A15/P2.7	48	P3.7/A16/RD#	9		
P3.7/A16/RD#	9				
P1.7/CEX4/A17/WCLK	17				

Processor Control		Power & Ground		Bus Control & Status	
Name	Pin	Name	Pin	Name	Pin
P3.2/INT0#	4	V <sub>CC</sub>	46	P3.6/WR#	8
P3.3/INT1#	5	V <sub>CCP</sub>	32	P3.7/RD#/A16	9
RST	23	AV <sub>CC</sub>	22	PSEN#	43
XTAL1	20	V <sub>SS</sub>	47	ALE	44
XTAL2	21	V <sub>SSP</sub>	64	EA#	45



4.0 SIGNALS

Table 9. Signal Description (Sheet 1 of 4)

Signal Name	Type	Description	Alternate Function
A17	O	<b>Address Line 17.</b> Output to memory as 18th external address bit in extended bus applications. Selected with bits RD1:0 in configuration byte UCONFIG0. See Table 10 and RD#, WR#, and PSEN#.	P1.7/CEX4/WCLK
A16	O	<b>Address Line 16.</b> Output to memory as 17th external address bit in extended bus applications. Selected with bits RD1:0 in configuration byte UCONFIG0. See Table 10 and RD#, WR#, and PSEN#.	RD#
A15:8	O	<b>Address Lines.</b> Upper address lines for external memory. Description is for nonpage mode configuration. For page mode configuration, data (D7:0) is multiplexed with the upper address byte (A15:8).	P2.7:0
AD7:0	I/O	<b>Address/Data Lines.</b> Multiplexed lower address lines and data lines for external memory. Description is for nonpage mode configuration. For page mode configuration, data (D7:0) is multiplexed with the upper address byte (A15:8).	P0.7:0
ALE	O	<b>Address Latch Enable.</b> ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	—
AV <sub>CC</sub>	PWR	<b>Analog V<sub>CC</sub>.</b> A separate V <sub>CC</sub> input for the phase-locked loop circuitry.	—
CEX2:0 CEX3 CEX4	I/O	<b>Programmable Counter Array (PCA) Input/Output Pins.</b> These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.5:3 P1.6/WAIT# P1.7/A17/WCLK
D <sub>M0</sub> , D <sub>P0</sub>	I/O	<b>USB Port 0.</b> D <sub>P0</sub> and D <sub>M0</sub> are the data plus and data minus lines of USB port 0, the upstream differential port. These lines do not have internal pullup resistors. Provide an external 1.5 KΩ pullup resistor at D <sub>P0</sub> to indicate the connection of a fullspeed device.  <b>NOTE:</b> D <sub>P0</sub> low and D <sub>M0</sub> low signals an SE0 (USB reset), causing the 8x930Hx to stay in reset.	—
D <sub>M1</sub> , D <sub>P1</sub> D <sub>M2</sub> , D <sub>P2</sub> D <sub>M3</sub> , D <sub>P3</sub>	I/O	<b>USB Ports 1, 2, 3.</b> D <sub>P1</sub> , D <sub>P2</sub> , D <sub>P3</sub> , D <sub>M1</sub> , D <sub>M2</sub> , and D <sub>M3</sub> , are the data plus and data minus lines of USB ports 1, 2, and 3, the three downstream differential ports. These lines have no internal pulldown resistors. Provide an external 15 KΩ pulldown resistor at each of these pins.	—

Table 9. Signal Description (Sheet 2 of 4)

Signal Name	Type	Description	Alternate Function
EA#	I	<b>External Access.</b> Directs program memory accesses to on-chip or off-chip code memory. When EA# is connected to ground, all program memory accesses are off-chip. When EA# is connected to $V_{CC}$ , program accesses on-chip ROM if the address is within the range of the on-chip ROM; otherwise, the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM, EA# must be connected to ground.	—
ECAP	I	<b>External Capacitor.</b> Connect a 1 $\mu$ F or larger capacitor between this pin and $V_{SS}$ to ensure proper operation of the differential line drivers.	—
ECI	I	<b>PCA External Clock Input.</b> External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	<b>External Interrupts 0 and 1.</b> These inputs set the IE1:0 interrupt flags in the TCON register. Bits IT1:0 in TCON select the triggering method: edge-triggered (high-to-low) or level triggered (active low). INT1:0 also serves as external run control for timer1:0 when selected by GATE1:0# in TCON.	P3.3:2
OVRI#	I	<b>Overcurrent Sense.</b> Senses input to indicate an overcurrent condition for a bus-powered USB device on an external downstream port. Active low.	—
P0.7:0	I/O	<b>Port 0.</b> This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.5:3 P1.6 P1.7	I/O	<b>Port 1.</b> This is an 8-bit, bidirectional I/O port with internal pull-ups.	T2 T2EX ECI CEX2:0 CEX3/WAIT# CEX4/A17/WCLK
P2.7:0	I/O	<b>Port 2.</b> An 8-bit, bidirectional I/O port with internal pull-ups.	A15:8
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	<b>Port 3.</b> An 8-bit, bidirectional I/O port with internal pull-ups.	RXD TXD INT1:0# T1:0 WR# RD#/A16
PLLSEL2:0	I	<b>Phase-locked Loop Select.</b> Three-bit code selects USB data rate (see Table 12 on page 16).	—
PSEN#	O	<b>Program Store Enable.</b> Read signal output. Asserted for the memory address range determined by bits RD1:0 in configuration byte UCONFIG0 (see RD# and Table 10).	—
RD#	O	<b>Read.</b> Read signal output to external data memory. Asserted only for RD1:0 = 11. See configuration byte UCONFIG0. (Also see PSEN# and Table 10).	P3.7/A16





## 8x930Hx UNIVERSAL SERIAL BUS PERIPHERAL CONTROLLER

Table 9. Signal Description (Sheet 3 of 4)

Signal Name	Type	Description	Alternate Function
RST	I	<b>Reset.</b> Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than $V_{IH1}$ is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor; connecting a capacitor between this pin and $V_{CC}$ implements power-on reset.  Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	<b>Receive Serial Data.</b> RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
SOF#	O	<b>Start of Frame.</b> Start of frame pulse. Active low. Asserted for 8 states (see Table 12) when frame timer is locked to USB frame timing and when SOF token or artificial SOF is detected.	—
T1:0	I	<b>Timer 1:0 External Clock Input.</b> When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	<b>Timer 2 Clock Input/Output.</b> For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	<b>Timer 2 External Input.</b> In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	<b>Transmit Serial Data.</b> TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
UPWEN#	O	<b>USB Power Enable.</b> A low signal on this pin applies power to all three external downstream ports.	—
$V_{CC}$	PWR	<b>Supply Voltage.</b> Connect this pin to the +5V supply voltage.	—
$V_{CCP}$	PWR	<b>Supply Voltage for I/O Buffers.</b> Connect this pin to the +5V supply voltage.	—
$V_{SS}$	GND	<b>Circuit Ground.</b> Connect this pin to ground.	—
$V_{SSP}$	GND	<b>Circuit Ground for I/O Buffers.</b> Connect this pin to ground.	—
WAIT#	I	<b>Real-time Wait State Input.</b> The real-time WAIT# input is enabled by writing a logical '1' to the WCON.0 (RTWE) bit at S:A7H. During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal on the port 1.6 input.	P1.6/CEX3
WCLK	O	<b>Wait Clock Output.</b> The real-time WCLK output is driven at port 1.7 (WCLK) by writing a logical '1' to the WCON.1 (RTWCE) bit at S:A7H. When enabled, the WCLK output produces a square wave signal with a period of TCLK.	P1.7/CEX4/A17



Table 9. Signal Description (Sheet 4 of 4)

Signal Name	Type	Description	Alternate Function
WR#	O	<b>Write.</b> Write signal output to external memory (See Table 10).	P3.6
XTAL1	I	<b>Oscillator Amplifier Input.</b> When implementing the on-chip oscillator, connect the external crystal/resonator across XTAL1 and XTAL2. If an external clock source is used, then connect it to this pin.	—
XTAL2	O	<b>Oscillator Amplifier Output.</b> When implementing the on-chip oscillator, connect the external crystal/resonator across XTAL1 and XTAL2. If an external oscillator is used, then leave XTAL2 unconnected.	—

Table 10. Memory Signal Selections (RD1:0) †

RD1:0	A17/P1.7/ CEX4/WCLK	A16/P3.7/RD#	PSEN#	WR#	Features
0 0	A17	A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external address space
0 1	P1.7/CEX4/WCLK	A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external address space
1 0	P1.7/CEX4/WCLK	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	64-Kbyte external address space One additional port pin
1 1	P1.7/CEX4/WCLK	RD# asserted for addresses ≤ 7F:FFFFH	Asserted for addresses ≥ 80:0000H	Asserted only for writes to MCS® 51 microcontroller data memory locations.	Compatible with MCS 51 microcontrollers. Separate 64-Kbyte external program and data memories.

† RD1:0 are bits 3:2 of configuration byte UCONFIG0. Refer to Figure 4-3 on page 4-5 in the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual*.



## 5.0 ADDRESS MAP

Table 11. 8x930Hx Address Map

Internal Address)	Description	Notes
FF:FFFFH FF:4000H	External Memory except the top eight bytes (FF:FFF8H – FF:FFFFH) which are reserved for the configuration array.	1, 2, 3
FF:FFFFH FF:0000H	External memory or on-chip nonvolatile memory (8 Kbytes FF:0000H – FF:1FFFH, 16 Kbytes FF:0000H – FF:3FFFH).	2, 4, 5
FE:FFFFH FE:0000H	External Memory	2
FD:FFFFH 02:0000H	Reserved Addresses	6
01:FFFFH 01:0000H	External Memory	2
00:FFFFH 00:0420H	External Memory	4
00:041FH 00:0080H	On-chip RAM	4
00:007FH 00:0020H	On-chip RAM	7
00:001FH 00:0000H	Storage for R0–R7 of Register File	8, 9

**NOTES:**

1. 18 address lines are bonded out (A15:0, A16:0, or A17:0 selected during chip configuration).
2. Data in this area is accessible by indirect addressing only.
3. Eight addresses at the top of all external memory maps are reserved for current and future device Configuration Byte information.
4. Data is accessible by direct and indirect addressing.
5. Devices reset into internal or external starting locations depending on the state of EA# and configuration byte information. See EA# signal description in Table 5. See also UCONFIG1:0 bit definitions in the *8x930Ax, 8x930Hx Universal Serial Bus Microcontroller User's Manual*.
6. This reserved area returns unspecified values. Software can execute a write to the reserved area, but nothing is actually written.
7. Data is accessible by direct, indirect, and bit addressing.
8. The special function registers (SFRs) and the register file have separate internal address spaces.
9. Data is accessible by direct, indirect, and register addressing.



## 6.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS<sup>†</sup>

Ambient Temperature Under Bias .....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pins to $V_{SS}$ .....	-0.5 V to +6.5 V
$I_{OL}$ per I/O Pin .....	15 mA
Power Dissipation (1) .....	1.5 W

**NOTICE:** This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

### OPERATING CONDITIONS<sup>†</sup>

$T_A$ (Ambient Temperature Under Bias):	
Commercial .....	-0°C to +70°C
$V_{CC} / V_{CCP}$ (Digital Supply Voltage) .....	4.40 V to 5.25 V
$V_{SS} / V_{SSP}$ .....	0 V
$AV_{CC}$ (Analog Supply Voltage) .....	4.40 V to 5.25 V
$F_{OSC}$ .....	12 MHz

**† WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**NOTE:** Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

## 6.1 Operating Frequencies

Table 12. 8x930Hx Operating Frequency

PLLSEL2:0 Pin 43, 42, 44 (1)	XTAL1 Frequency ( $F_{OSC}$ )	USB Rate (2)	Internal Frequency for CPU and Peripherals ( $1/T_{CLK}$ ) (3)	XTAL1 Clocks per State ( $T_{OSC}/state$ ) (5)	Comments
110	12 MHz	12 Mbps (Full Speed)	12 MHz (4)	1	PLL On

#### NOTES:

- Other PLLSELx combinations are not valid.
- The sampling rate is four times the USB rate.
- The AC timing specification (Table 15) defines the following symbol: CPU frequency =  $F_{CLK} = 1/T_{CLK}$ .
- The 8x930Hx CPU and peripheral frequency is 3 MHz (low clock mode) until the LC bit in PCON is cleared by user firmware.
- When the CPU is operating in low clock mode (3 MHz), 1 state equals 4  $T_{OSC}$ .



6.2 DC Characteristics

Table 13. DC Characteristics at Operating Conditions (Sheet 1 of 2)

Symbol	Parameter	Min	Typical <sup>(1)</sup>	Max	Units	Test Conditions
V <sub>IL</sub>	Input Low Voltage (except EA#)	-0.5		0.2 V <sub>CC</sub> - 0.1	V	
V <sub>IL1</sub>	Input Low Voltage (EA#)	0		0.2 V <sub>CC</sub> - 0.3	V	
V <sub>IH</sub>	Input High Voltage (except XTAL1, RST)	0.2 V <sub>CC</sub> + 0.9		V <sub>CC</sub> + 0.5	V	
V <sub>IH1</sub>	Input High Voltage (XTAL1, RST)	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage (port 1, 2, 3)			0.3 0.45 1.0	V	I <sub>OL</sub> = 100 μA <sup>(2) (3)</sup> I <sub>OL</sub> = 1.6 mA I <sub>OL</sub> = 3.5 mA
V <sub>OL1</sub>	Output Low Voltage (port 0, ALE, PSEN#, SOF#)			0.3 0.45 1.0	V	I <sub>OL</sub> = 200 μA <sup>(2) (3)</sup> I <sub>OL</sub> = 3.2 mA I <sub>OL</sub> = 7.0 mA
V <sub>OH</sub>	Output High Voltage (port 1, 2, 3, ALE, PSEN#, SOF#)	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V	I <sub>OH</sub> = -10 μA <sup>(4)</sup> I <sub>OH</sub> = -30 μA I <sub>OH</sub> = -60 μA
V <sub>OH1</sub>	Output High Voltage (port 0 in external address space)	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V	I <sub>OH</sub> = -200 μA <sup>(4)</sup> I <sub>OH</sub> = -3.2 mA I <sub>OH</sub> = -7.0 mA
I <sub>IL</sub>	Logical 0 Input Current (port 1,2,3)			-150	μA	V <sub>IN</sub> = 0.45 V
I <sub>LI</sub>	Input Leakage Current (port 0)			±10	μA	0.45 < V <sub>IN</sub> < V <sub>CC</sub>
I <sub>TL</sub>	Logical 1-to-0 Transition Current (Port 1, 2,3)			-650	μA	V <sub>IN</sub> = 2.0 V
R <sub>RST</sub>	RST Pulldown Resistor	40		225	KΩ	
C <sub>IO</sub>			10		pF	F <sub>OSC</sub> = 12 MHz T <sub>A</sub> = 25°C
I <sub>PD</sub>	Powerdown Current Normal powerdown USB suspend		25 145	75 175	μA	

Table 13. DC Characteristics at Operating Conditions (Sheet 2 of 2)

Symbol	Parameter	Min	Typical <sup>(1)</sup>	Max	Units	Test Conditions
I <sub>DL</sub>	Idle Mode I <sub>CC</sub>			60	mA	Full speed (in low clock mode) PLLSEL2:0 = 110 F <sub>CLK</sub> = 3 MHz
				110		Full speed (not in low clock mode) PLLSEL2:0 = 110 F <sub>CLK</sub> = 12 MHz
I <sub>CC</sub>	Active Current			75	mA	Full speed (in low clock mode) PLLSEL2:0 = 110 F <sub>CLK</sub> = 3 MHz
				170		Full speed (not in low clock mode) PLLSEL2:0 = 110 F <sub>CLK</sub> = 12 MHz

**NOTE:**

- Typical values are obtained using V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C and are not guaranteed.
- Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:  
Maximum I<sub>OH</sub> per port pin: 10 mA  
Maximum I<sub>OL</sub> per 8-bit port:  
Port 0: 26 mA      Ports 1-3: 15 mA  
Maximum Total I<sub>OL</sub> for all output pins: 71 mA  
If I<sub>OL</sub> exceeds the test conditions, then V<sub>OL</sub> may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
- Capacitive loading on ports 0 and 2 causes the V<sub>OH</sub> on ALE and PSEN to drop below the V<sub>CC</sub> specification when the address lines are stabilizing.



### 6.3 Explanation of Timing Symbols

Table 14 defines the timing symbols used in Tables 11 through 14 and the associated timing diagrams. They have the form  $T_{\text{XYY}}$ , where the character pairs represent a signal and its condition. Timing symbols represent the time between two signal / condition points.

**Table 14. AC Timing Symbol Definitions**

Character	Signal(s)
A	Address: A17, A16, A15:8, A7:0
C	Wait Clock (WCLK), External Clock (XTAL1)
D	Data In: D7:0, RXD
L	ALE
Q	Data Out: D7:0, RXD
R	Read: RD#/PSEN#
W	Write: WR#
X	TXD
Y	WAIT#

Character	Condition
H	High
L	Low
V	Valid, Setup
X	No Longer Valid, Hold
Z	Floating (low impedance)

## 6.4 System Bus AC Characteristics

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall times = 10 ns,  $F_{OSC} = 12$  MHz.

Table 15. AC Characteristics at Operating Conditions (Sheet 1 of 2)

Symbol	Parameter	CPU Frequency @ 12 MHz (M, N = 0)	CPU Frequency ( $F_{CLK}$ ) Variable		Units
			Min	Max	
$T_{CLK}$	1/(CPU Frequency)	83.33 (Typical)			ns (1) (2)
$T_{LHLL}$	ALE Pulse Width	34.66	$(0.5+M)T_{CLK} - 7$		ns (4)
$T_{AVLL}$	Address Valid to ALE Low	21.66	$(0.5+M)T_{CLK} - 20$		ns (4)
$T_{LLAX}$	Address Hold after ALE Low	4	4		ns
$T_{RLRH}^{(3)}$	RD# or PSEN# Pulse Width	73.33	$(1+N)T_{CLK} - 10$		ns (5)
$T_{WLWH}$	WR# Pulse Width	71.33	$(1+N)T_{CLK} - 12$		ns (5)
$T_{LLRL}^{(3)}$	ALE Low to RD# or PSEN# Low	5	5		ns
$T_{LHAX}$	ALE High to Address Hold	40.33	$(1+M)T_{CLK} - 43$		ns (4)
$T_{RLDV}^{(3)}$	RD# or PSEN# Low to Valid Data/Instruction In	50.33		$(1+N)T_{CLK} - 33$	ns (5)
$T_{RHDX}^{(3)}$	Data/Instruction. Hold After RD# or PSEN# High	0	0		ns
$T_{RLAZ}^{(3)}$	RD# or PSEN# Low to Address Float	0		0	ns
$T_{RHDZ1}^{(3)}$	Instruct. Float After PSEN# High	10		10	ns
$T_{RHDZ2}^{(3)}$	Data Float After RD# or PSEN# High	83.33		$T_{CLK}$	ns
$T_{RHLH1}^{(3)}$	PSEN# High to ALE High (instruction)	10	10		ns
$T_{RHLH2}^{(3)}$	RD# or PSEN# High to ALE High (data)	83.33	$T_{CLK}$		ns
$T_{WHLH}$	WR# High to ALE High	88.33	$T_{CLK} + 5$		ns
$T_{AVDV1}$	Address (Port 0) Valid to Valid Data/Instruction In	98.66		$(2+M+N)T_{CLK} - 68$	ns (4) (5)

### NOTES:

1. Refer to Table 12 for CPU frequencies versus XTAL1 frequencies.
2. XTAL1 frequency is  $\pm 0.25\%$  for full speed and  $\pm 1.5\%$  for low speed.
3. Specifications for PSEN# are identical to those for RD#.
4.  $M = 0, 1$  is the extended ALE state.
5.  $N = 0, 1, 2, 3$  is the RD#/PSEN#/WR# wait state.





Table 15. AC Characteristics at Operating Conditions (Sheet 2 of 2)

Symbol	Parameter	CPU Frequency @ 12 MHz (M, N = 0)	CPU Frequency (F <sub>CLK</sub> ) Variable		Units
			Min	Max	
T <sub>AVDV2</sub>	Address (Port 2) Valid to Valid Data/Instruction In	118.66		(2+M+N)T <sub>CLK</sub> - 48	ns (4) (5)
T <sub>AVDV3</sub>	Address (Port 2) Valid to Valid Instruction In	23.33		(1+N)T <sub>CLK</sub> - 60	ns <sup>(5)</sup>
T <sub>AVRL</sub> <sup>(3)</sup>	Address Valid to RD# or PSEN# Low	37.33	(1+M)T <sub>CLK</sub> - 46		ns <sup>(4)</sup>
T <sub>AVWL1</sub>	Address (Port 0) Valid to WR# Low	37.33	(1+M)T <sub>CLK</sub> - 46		ns <sup>(4)</sup>
T <sub>AVWL2</sub>	Address (Port 2) Valid to WR# Low	66.33	(1+M)T <sub>CLK</sub> - 17		ns <sup>(4)</sup>
T <sub>WHQX</sub>	Data Hold after WR# High	28.66	0.5 T <sub>CLK</sub> - 13		ns
T <sub>QVWH</sub>	Data Valid to WR# High	68.33	(1+N)T <sub>CLK</sub> - 15		ns <sup>(5)</sup>
T <sub>WHAX</sub>	WR# High to Address Hold	70.33	T <sub>CLK</sub> - 13		ns

**NOTES:**

1. Refer to Table 12 for CPU frequencies versus XTAL1 frequencies.
2. XTAL1 frequency is ± 0.25% for full speed and ± 1.5% for low speed.
3. Specifications for PSEN# are identical to those for RD#.
4. M = 0,1 is the extended ALE state.
5. N = 0,1,2,3 is the RD#/PSEN#/WR# wait state.

6.4.1 SYSTEM BUS TIMING DIAGRAMS

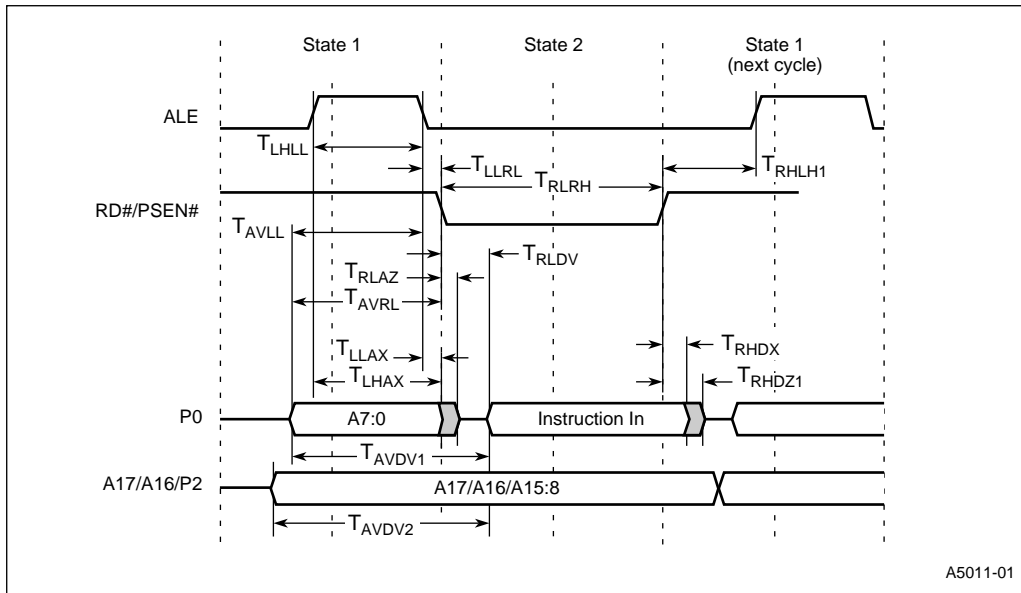


Figure 6. 8x930Hx Code Fetch, Nonpage Mode



8x930Hx UNIVERSAL SERIAL BUS PERIPHERAL CONTROLLER

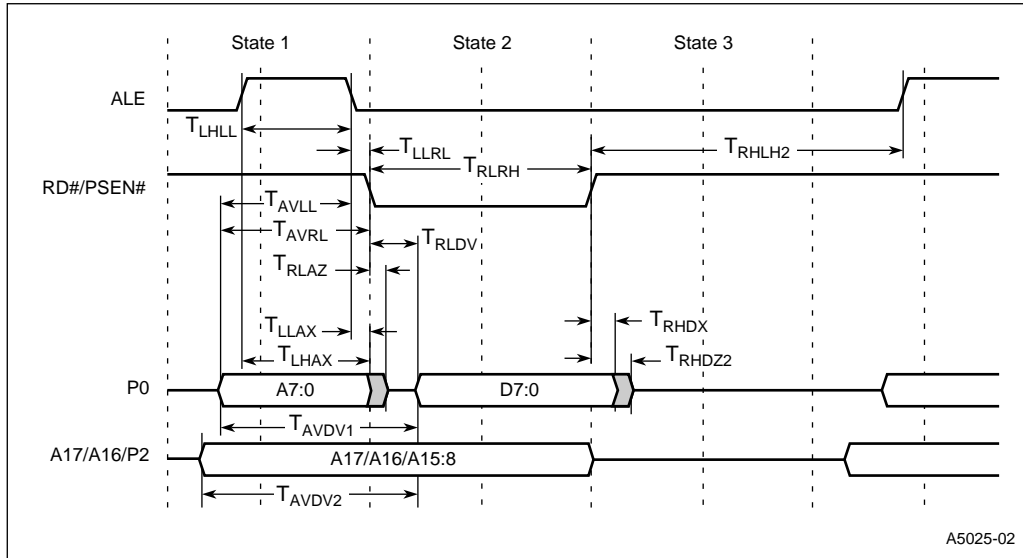


Figure 7. 8x930Hx Data Read, Nonpage Mode

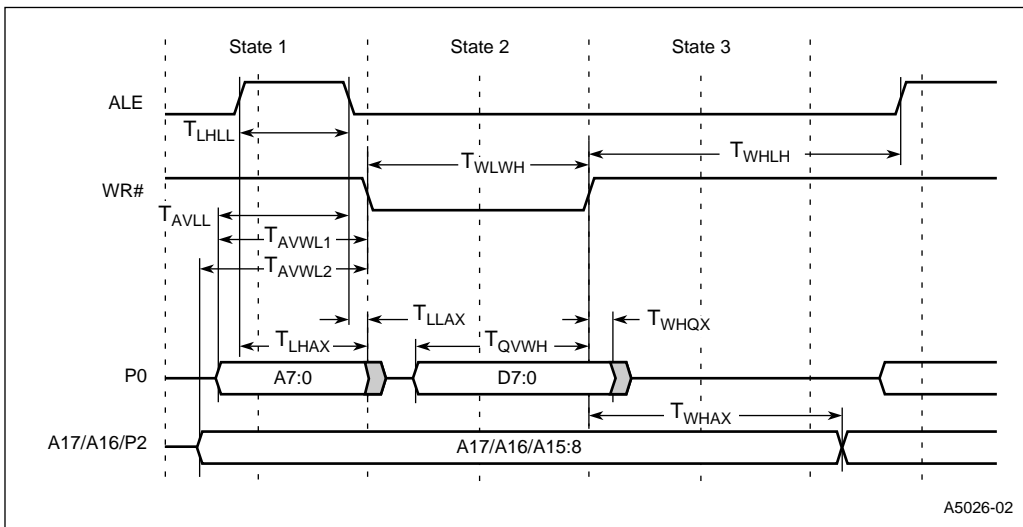


Figure 8. 8x930Hx Data Write, Nonpage Mode

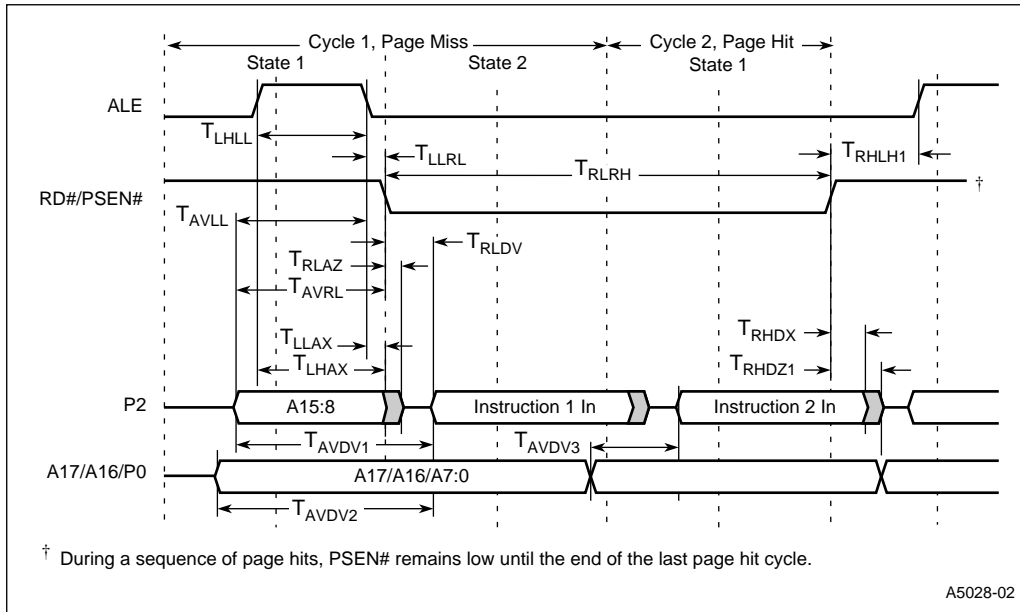


Figure 9. 8x930Hx Code Fetch, Page Mode



### 8x930Hx UNIVERSAL SERIAL BUS PERIPHERAL CONTROLLER

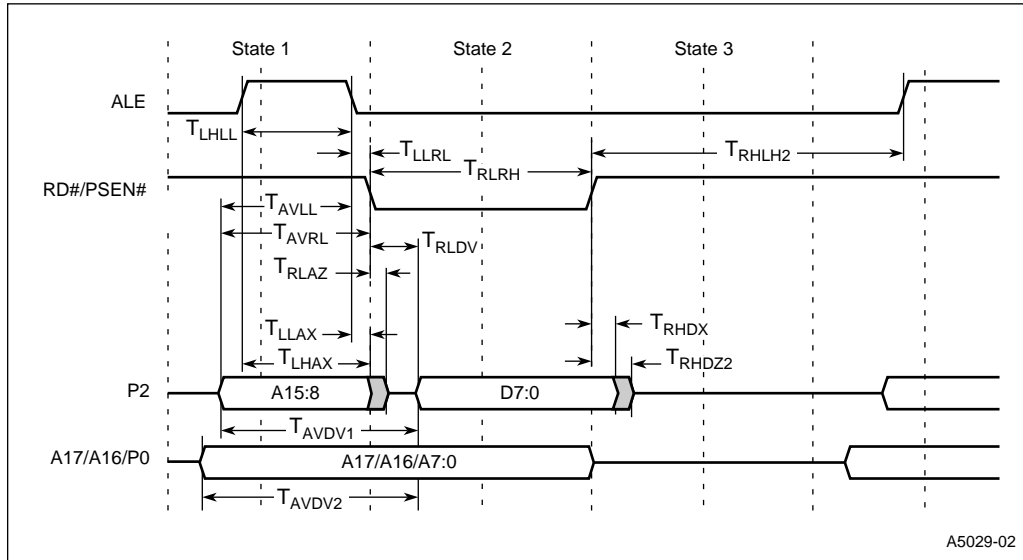


Figure 10. 8x930Hx Data Read, Page Mode

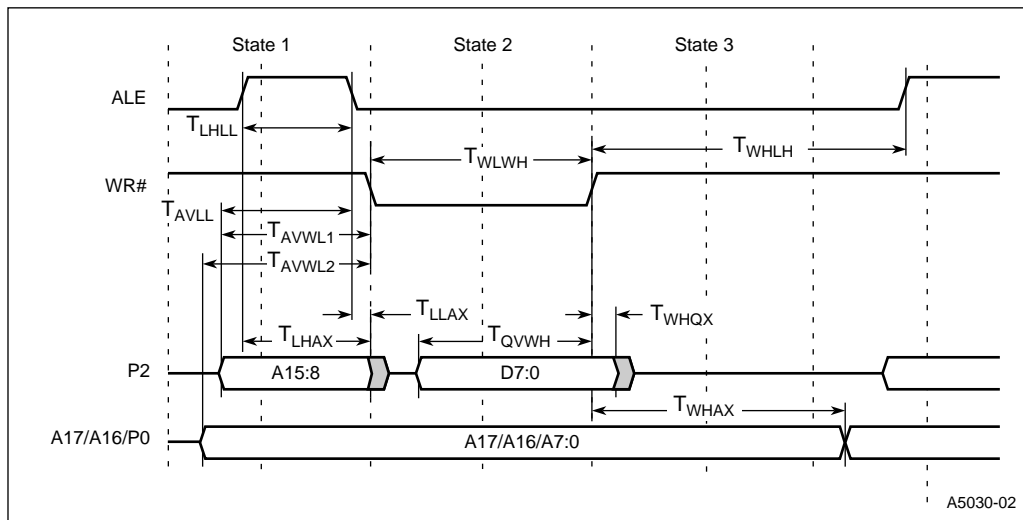


Figure 11. 8x930Hx Data Write, Page Mode

## 6.4.2 REAL-TIME WAIT STATE FUNCTION AC CHARACTERISTICS

Table 16. Real-time Wait State AC Timing Specifications

Symbol	Parameter	F <sub>CLK</sub> Variable <sup>(1)</sup> <sup>(2)</sup>			Units
		Min	Typ	Max	
T <sub>CLYV</sub>	WCLK Low to WAIT# Setup	0		0.5 T <sub>CLK</sub> - 13	ns
T <sub>CLYX</sub>	WAIT# Hold after WCLK Low	(W)T <sub>CLK</sub> + 5		(0.5+W)T <sub>CLK</sub> - 13	ns
T <sub>RLYV</sub> <sup>(2)</sup>	PSEN# or RD# Low to WAIT# Setup	0		0.5 T <sub>CLK</sub> - 13	ns
T <sub>RLYX</sub>	WAIT# Hold after PSEN# or RD# Low	(W)T <sub>CLK</sub> + 5		(0.5+W)T <sub>CLK</sub> - 13	ns
T <sub>WLYV</sub>	WR# Low to WAIT# Setup	0		0.5 T <sub>CLK</sub> - 13	ns
T <sub>WLYX</sub>	WAIT# Hold after WR# Low	(W)T <sub>CLK</sub> + 5		(0.5+W)T <sub>CLK</sub> - 13	ns

**NOTES:**

1. W is the number of real-time wait states (0, 1, 2, ... highest possible number).
2. The real-time wait function has a critical timing for instruction reads. It is not advisable to use this feature for instruction reads during page mode.



6.4.3 REAL-TIME WAIT STATE FUNCTION TIMING DIAGRAMS

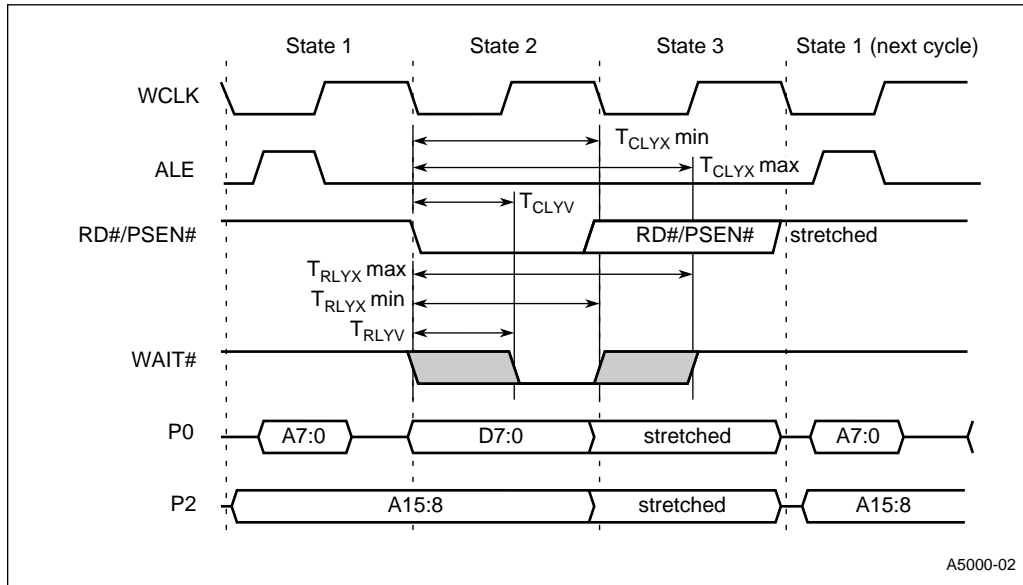


Figure 12. External Code Fetch/Data Read (Nonpage Mode, Real-time Wait State)

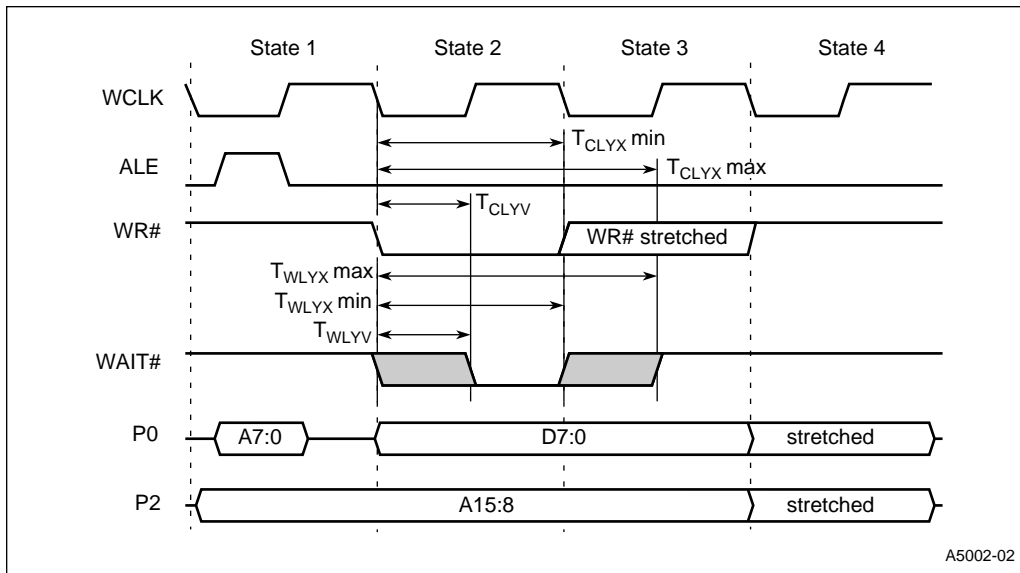


Figure 13. External Data Write (Nonpage Mode, Real-time Wait State)

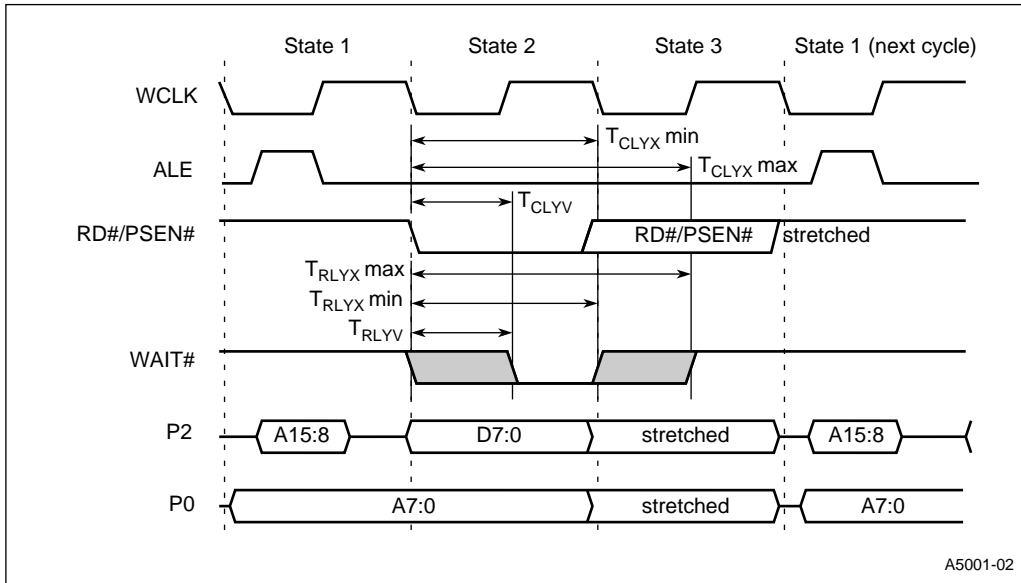


Figure 14. External Data Read (Page Mode, Real-time Wait State)

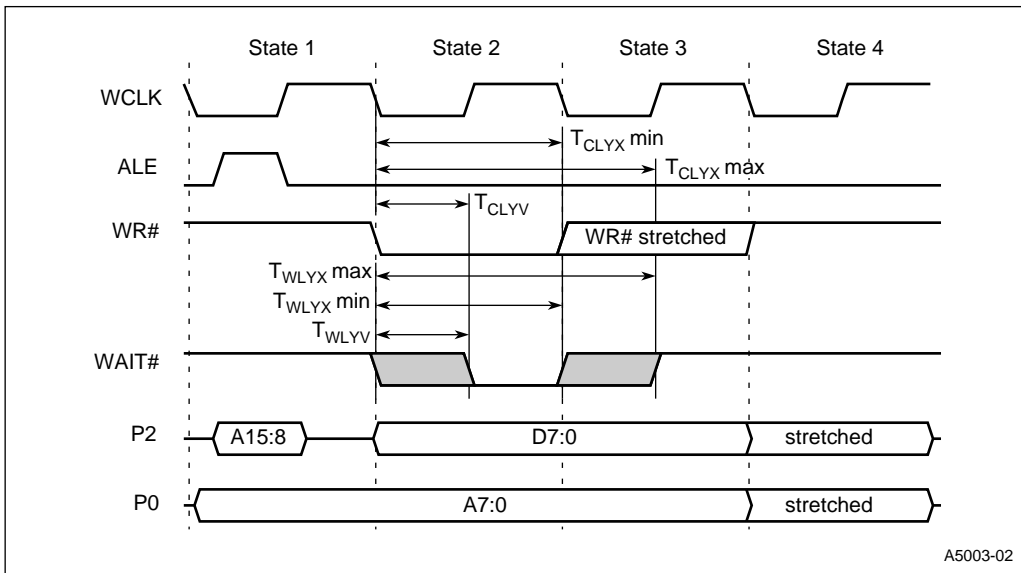


Figure 15. External Data Write (Page Mode, Real-time Wait State)





6.5 AC Characteristics — Synchronous Mode 0

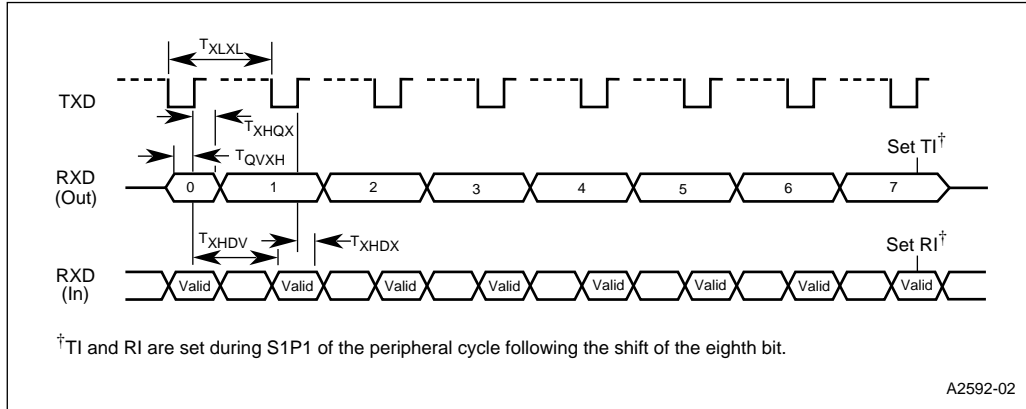


Figure 16. Serial Port Waveform — Synchronous Mode 0

Table 17. Serial Port Timing — Synchronous Mode 0

Symbol	Parameter	Min	Max	Units
$T_{XLXL}$	Serial Port Clock Cycle Time	$6 T_{OSC}$		ns
$T_{QVXH}$	Output Data Setup to Clock Rising Edge	$5 T_{OSC} - 133$		ns
$T_{XHGX}$	Output Data Hold after Clock Rising Edge	$T_{OSC} - 50$		ns
$T_{XHDX}$	Input Data Hold after Clock Rising Edge	0		ns
$T_{XHDV}$	Clock Rising Edge to Input Data Valid		$5 T_{OSC} - 133$	ns

6.6 External Clock Drive

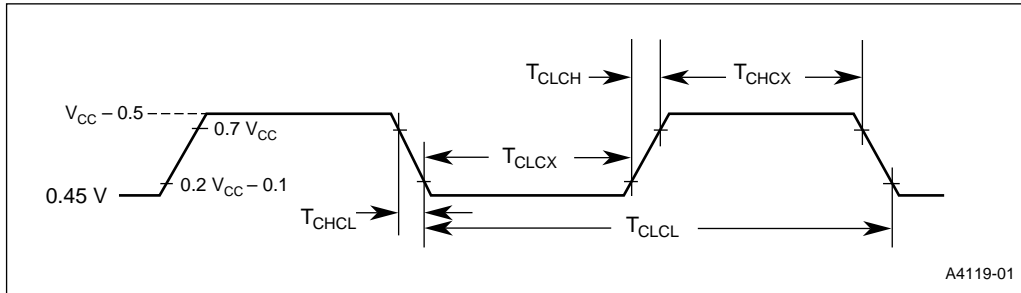


Figure 17. External Clock Drive Waveforms

Table 18. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{OSC}$	Oscillator Frequency ( $F_{OSC}$ )	6	12	MHz
$T_{CHCX}$	High Time	$0.35 T_{OSC}$	$0.65 T_{OSC}$	ns
$T_{CLCX}$	Low Time	$0.35 T_{OSC}$	$0.65 T_{OSC}$	ns
$T_{CLCH}$	Rise Time		10	ns
$T_{CHCL}$	Fall Time		10	ns

### 6.7 Testing Waveforms

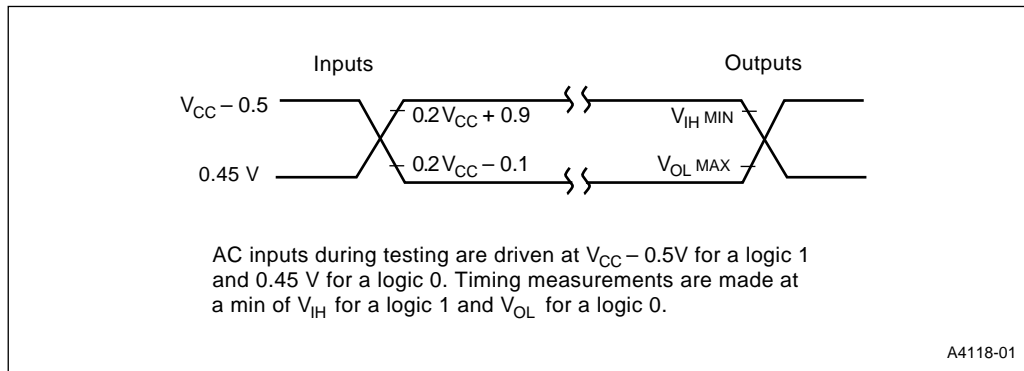


Figure 18. AC Testing Input, Output Waveforms

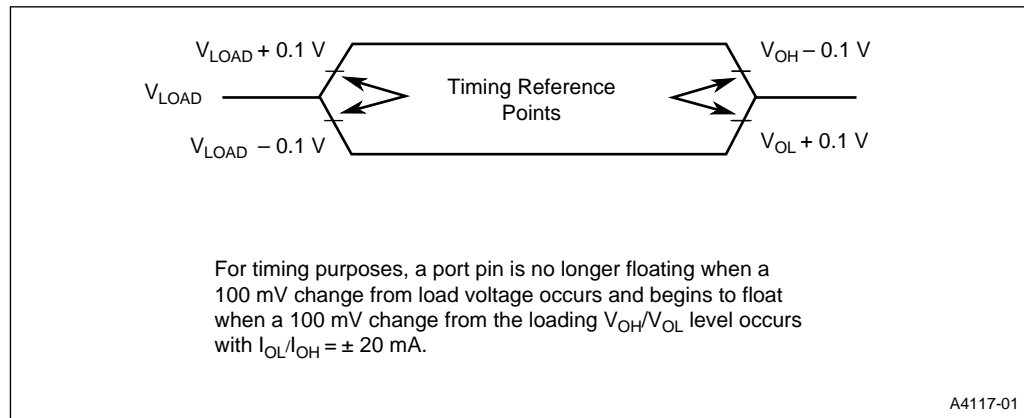


Figure 19. Float Waveforms



## 7.0 THERMAL CHARACTERISTICS

The microcontroller operates over the commercial temperature range from 0°C to 70°C. All thermal impedance data (see Table 19) is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

**Table 19. Thermal Characteristics**

Package Type	$\theta_{JA}$	$\theta_{JC}$
68-pin PLCC	N/A	N/A

## 8.0 DESIGN CONSIDERATIONS

### 8.1 External Bus Timing and Peripheral Timing Affected by PLLSEL2:0 Selection

PLLSEL2 (pin 43), PLLSEL1 (pin 42), and PLLSEL0 (pin 44) determine the 8x930Hx internal CPU operating frequency. See Table 12. Operate the 8x930Hx at full speed by setting PLLSEL2:0 to 110. This provides an internal clock frequency of 12 MHz ( $F_{CLK} = F_{OSC}$ ) and sets the microcontroller state time equal to one oscillator period ( $T_{OSC}$ ).

The CPU operating frequency influences the timing of all on-chip peripherals. Refer to the *8X930Ax, 8X930Hx Universal Serial Bus Microcontroller User's Manual* for peripheral timing formulas (refer to Table 1 on page 1 for ordering information).

### 8.2 Low Clock Mode Frequency

The internal clock  $F_{CLK}$  distributed to the CPU and peripherals is 3 MHz. Peripheral timing and external bus accesses (including instruction fetch and data read/write) are affected. Refer to Table 12 for clock rates.

### 8.3 Setting RXFFRC Bit Clears Only the Oldest Packet in the FIFO

If the receive FIFO is set as a dual packet mode, then it can receive two packets. Setting RXFFRC (in RXCON registers) to indicate FIFO Read Complete will **not** flush the entire FIFO; it will flush only the oldest packet. The read marker will be advanced to the location of the read pointer.

### 8.4 Series Resistor Requirement for Impedance Matching

Per USB rev. 1.0 specification (page 111, section 7.1.1.1), the impedance of the differential driver must be between 29Ω and 44Ω. To match the cable impedance, a series resistor of 27Ω to 33Ω should be connected to each USB line; i.e., on  $D_{P0}$  (pin 55) and on  $D_{M0}$  (pin 54). If the USB line is improperly terminated or not matched, then signal fidelity will suffer. This condition can be seen on the oscilloscopes as excessive overshoot and undershoot. This condition can potentially introduce bit errors.

### 8.5 Pullup Resistor Requirement for 8x930Hx Hub devices

The USB specification requires a pullup resistor to allow the host to identify which devices are low speed and which are full speed in order to communicate at the appropriate data rate. For 8x930Hx hub devices (12 Mbps), use a 1.5KΩ pullup resistor (to 3.0 V – 3.6 V) on the  $D_{P0}$  line.

### 8.6 Powerdown Mode Cannot Be Invoked Before USB Suspend

If the 8x930Hx is put into powerdown mode before receiving a USB suspend signal from the host, then a USB resume will not properly wake up the 8x930Hx from powerdown mode.



## 9.0 8x930Hx ERRATA

The 8x930Hx may contain design defects or errors known as errata. Characterized errata that may cause the 8x930Hx's operational behavior to deviate from published specifications are documented in a specification update (order number 272962). Specification updates can be obtained from your local Intel sales office or from the World Wide Web ([www.intel.com](http://www.intel.com)).

## 10.0 DATASHEET REVISION HISTORY

Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This (-002) revision of the 8x930Hx datasheet replaces earlier product information. The following changes were made in this revision:

1. Added 64-pin SDIP package information.
2. The following DC Characteristics were changed:  $I_{PD}$ ,  $I_{DL}$  and  $I_{CC}$ .
3. The following AC Characteristics were changed: Tavl, Tlax, Twlwh, Tlrl, Tlhax, Trhdz2, Trlh2, Twlh, Tavdv1, Tavdv3, Tavr1, Tawl1 and Tawl2.

