ADVANCE INFORMATION

VS28F016SV, MS28F016SV
16-Mbit (1-Mbit x 16, 2-Mbit x 8) FlashFile™ MEMORY

- **VS28F016SV**
  - **— −40°C to +125°C**
  - **— SE2 Grade**
- **MS28F016SV**
  - **— −55°C to +125°C**
  - **— QML Certified**
  - **— SE1 Grade**
- **SmartVoltage Technology**
  - **— User-Selectable 3.3V or 5V V_{CC}**
  - **— User-Selectable 5V or 12V V_{PP}**
- **Three Voltage/Speed Options**
  - **— 80 ns Access Time, 5.0V ±5%**
  - **— 85 ns Access Time, 5.0V ±10%**
  - **— 120 ns Access Time, 3.3V ±10%**
- **1 Million Erase Cycles per Block Typical**
- **14.3 MB/sec Burst Write Transfer Rate**
- **Configurable x8 or x16 Operation**
- **56-Lead SSOP Plastic Package**
- **Backwards-Compatible with VE28F008, M28F008 and 28F016SA Command Set**
- **Revolutionary Architecture**
  - **— Multiple Command Execution**
  - **— Write During Erase**
  - **— Command Super-Set of the Intel VE28F008, M28F008**
  - **— Page Buffer Write**
- **Multiple Power Savings Modes**
- **Two 256-Byte Page Buffers**
- **State-of-the-Art 0.6 µm ETOX™ IV Flash Technology**

Intel's VS/MS28F016SV, 16-Mbit FlashFile™ Memory is the latest member of Intel's high density, high performance memory family for the Industrial, Special Environment, and Military markets. Its user selectable V_{CC} and V_{PP} (SmartVoltage Technology), innovative capabilities, 100% compatibility with the VE28F008 and M28F008, multiple power savings modes, selective block locking, and very fast read/write performance make it the ideal choice for any applications that need a high density and a wide temperature range memory device. The VS/MS28F016SV is the ideal choice for designers who need to break free from the dependence on slow rotating media or battery backed up memory arrays.

With two product grades (SE1: −55°C to +125°C, and SE2: −40°C to +125°C) available, the VS/MS28F016SV is perfect for the non-PC industries like Telecommunications, Embedded/Industrial, Automotive, Navigation, Wireless Communication, Commercial Aircraft, and all Military programs.

The VS/MS28F016SV's x8/x16 architecture allows for the optimization of the memory to processor interface. The flexible block locking options enable bundling of executable application software in a Resident Flash Array (RFA), PCMCIA Memory or ATA Cards or Memory modules.

The VS/MS28F016SV is offered in a 56-lead SS0P (Shrink Small Outline Package) and is manufactured on Intel's 0.6 µm ETOX™ IV process technology.

December 1995 **Order Number: 271312-002**

VS28F016SV, MS28F016SV FlashFile™ MEMORY

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1.0 INTRODUCTION

The documentation of the Intel VS/MS28F016SV memory device includes this data sheet, a detailed user's manual, and a number of application notes, all of which are referenced at the end of this data sheet.

The data sheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications. The 28F016SA (compatible with VS/MS28F016SV) User's Manual provides complete descriptions of the user modes, system interface examples and detailed descriptions of all principles of operation. It also contains the full list of software algorithm flowcharts, and a brief section on compatibility with the Intel VE28F008 and M28F008.

1.1 Enhanced Features

The VS/MS28F016SV is backwards compatible with the VE28F008 and M28F008 and offers the following enhancements:

- SmartVoltage Technology
  - — Selectable 5.0V or 12.0V V_{PP}
- V_{PP} Level Bit in Block Status Register
- Additional RY/BY# Configuration
  - — Pulse-On-Write/Erase
- Additional Upload Device Information Command Feedback
  - — Device Revision Number
  - — Device Proliferation Code
  - — Device Configuration Code
- x8/x16 Architecture
- Block Locking
- 2 Page Buffers
- Instruction Queuing

1.2 Product Overview

The VS/MS28F016SV is a high-performance, 16-Mbit (16,777,216-bit) block erasable, non-volatile random access memory, organized as either 1 Mword x 16 or 2 Mbyte x 8. The VS/MS28F016SV includes thirty-two 64-KB (65,536 byte) blocks or thirty-two 32-KW (32,768 word) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and result in greater product reliability and ease of use.

The VS/MS28F016SV incorporates SmartVoltage technology, providing V_{CC} operation at both 3.3V and 5.0V and program and erase capability at V_{PP} = 12.0V or 5.0V. Operating at V_{CC} = 3.3V, the VS/MS28F016SV consumes approximately one-half the power consumption at 5.0V V_{CC}, while 5.0V V_{CC} provides highest read performance capability. V_{PP} = 5.0V operation eliminates the need for a separate 12.0V converter, while V_{PP} = 12.0V maximizes write/erase performance. In addition to the flexible program and erase voltages, the dedicated V_{PP} gives complete code protection with $V_{PP} \leq V_{PPLK}$.

Depending on system design specifications, the VS/MS28F016SV is capable of supporting

- — 80 ns access times with a V_{CC} of 5.0V ±5% and loading of 30 pF
- — 85 ns access times with a V_{CC} of 5.0V ±10% and loading of 100 pF
- — 120 ns access times with a V_{CC} of 3.3V ±5% and loading of 50 pF

A 3/5# input pin configures the device's internal circuitry for optimal 3.3V or 5.0V Read/Write operation.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte/Word Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the VE28F008 or M28F008 8-Mbit FlashFile memory.

A super-set of commands has been added to the basic VE28F008 or M28F008 command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Page Buffer Writes to Flash
- Command Queuing Capability
- Automatic Data Writes during Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 6 μsec (12.0V V_{PP}) – a 33% improvement over the VE28F008 or M28F008. A Block Erase operation erases one of the 32 blocks in about 1.0 sec (12.0V V_{PP}), independent of the other blocks, which is about a 65% improvement over the VE28F008 or M28F008.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve one million Block Erase Cycles by providing wear-leveling algorithms and graceful block retirement. These techniques have already been employed in many flash file systems and hard disk drive designs.

The VS/MS28F016SV incorporates two Page Buffers of 256 bytes (128 words) each to allow page data writes. This feature can improve a system write performance by up to 4.8 times over previous flash memory devices, which have no Page Buffers.

All operations are started by a sequence of Write commands to the device. Three Status Registers (described in detail later in this data sheet) and a RY/BY# output pin provide information on the progress of the requested operation.

While the VE28F008 or M28F008 requires an operation to complete before the next operation can be requested, the VS/MS28F016SV allows queuing of the next operation while the memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The VS/MS28F016SV can also perform Write operations to one block of memory while performing Erase of another block.

The VS/MS28F016SV provides selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable O/S or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the VS/MS28F016SV has a master Write Protect pin (WP#) which prevents any modifications to memory blocks whose lock-bits are set.

The VS/MS28F016SV contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the VE28F008 or M28F008 FlashFile memory Status Register. The CSR, when used alone, provides a straightforward upgrade capability to the VS/MS28F016SV from a VE28F008- or M28F008-based design.
- A Global Status Register (GSR) which informs the system of command Queue status, Page Buffer status, and overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for Byte-Wide and Word-Wide modes are shown in Figures 4 and 5.

The VS/MS28F016SV incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

Other configurations of the RY/BY# pin are enabled via special CUI commands and are described in detail in the 16-Mbit Flash Product Family User's Manual.

The VS/MS28F016SV's Upload Device Information command is enhanced compared to the VE28F008 or M28F008, providing access to additional device information. This command uploads the Device Revision Number, Device Proliferation Code and Device Configuration Code. The Device Proliferation Code for the VS/MS28F016SV is 01H, and the Device Configuration Code identifies the current RY/BY# configuration. Section 4.4 documents the exact page buffer address locations for all uploaded information. A subsequent Page Buffer Swap and Page Buffer Read command sequence is necessary to read the correct device information.

The VS/MS28F016SV also incorporates a dual chip-enable function with two input pins, CE_0# and CE_1#. These pins have exactly the same functionality as the regular chip-enable pin, CE#, on the VE28F008 or M28F008. For minimum chip designs, CE_1# may be tied to ground and system logic may use CE_0# as the chip enable input. The VS/MS28F016SV uses the logical combination of these two signals to enable or disable the entire chip. Both CE_0# and CE_1# must be active low to enable the device. If either one becomes inactive, the chip will be disabled. This feature, along with the open drain RY/BY# pin, allows the system designer to reduce the number of control pins used in a large array of 16-Mbit devices.

The BYTE# pin allows either x8 or x16 read/writes to the VS/MS28F016SV. BYTE# at logic low selects 8-bit mode with address A_0 selecting between low byte and high byte. On the other hand, BYTE#

at logic high enables 16-bit operation with address A_1 becoming the lowest order address and address A_0 is not used (don't care). A device block diagram is shown in Figure 1.

The VS/MS28F016SV is specified for a maximum access time of 80 ns (t_{ACC}) at 5.0V operation (4.75V to 5.25V) in either the SE1 or SE2 grades. A corresponding maximum access time of 120 ns at 3.3V (3.15V to 3.45V) is achieved for reduced power consumption applications.

The VS/MS28F016SV incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching). In APS mode, the typical I_{CC} current is 1 mA at 5.0V (0.8 mA at 3.3V).

A deep power-down mode of operation is invoked when the RP# (called PWD# on the VE28F008 or M28F008) pin transitions low. This mode brings the device power consumption to less than 30.0 μA, typically, and provides additional write protection by acting as a device reset pin during power transitions. A reset time of 500 ns (5.0V V_{CC} operation) is required from RP# switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS standby mode of operation is enabled when either CE_0# or CE_1# transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 70 μA at 5V V_{CC}.

2.0 DEVICE PINOUT

The VS/MS28F016SV 56L-SSOP pinout configuration is shown in Figure 2.

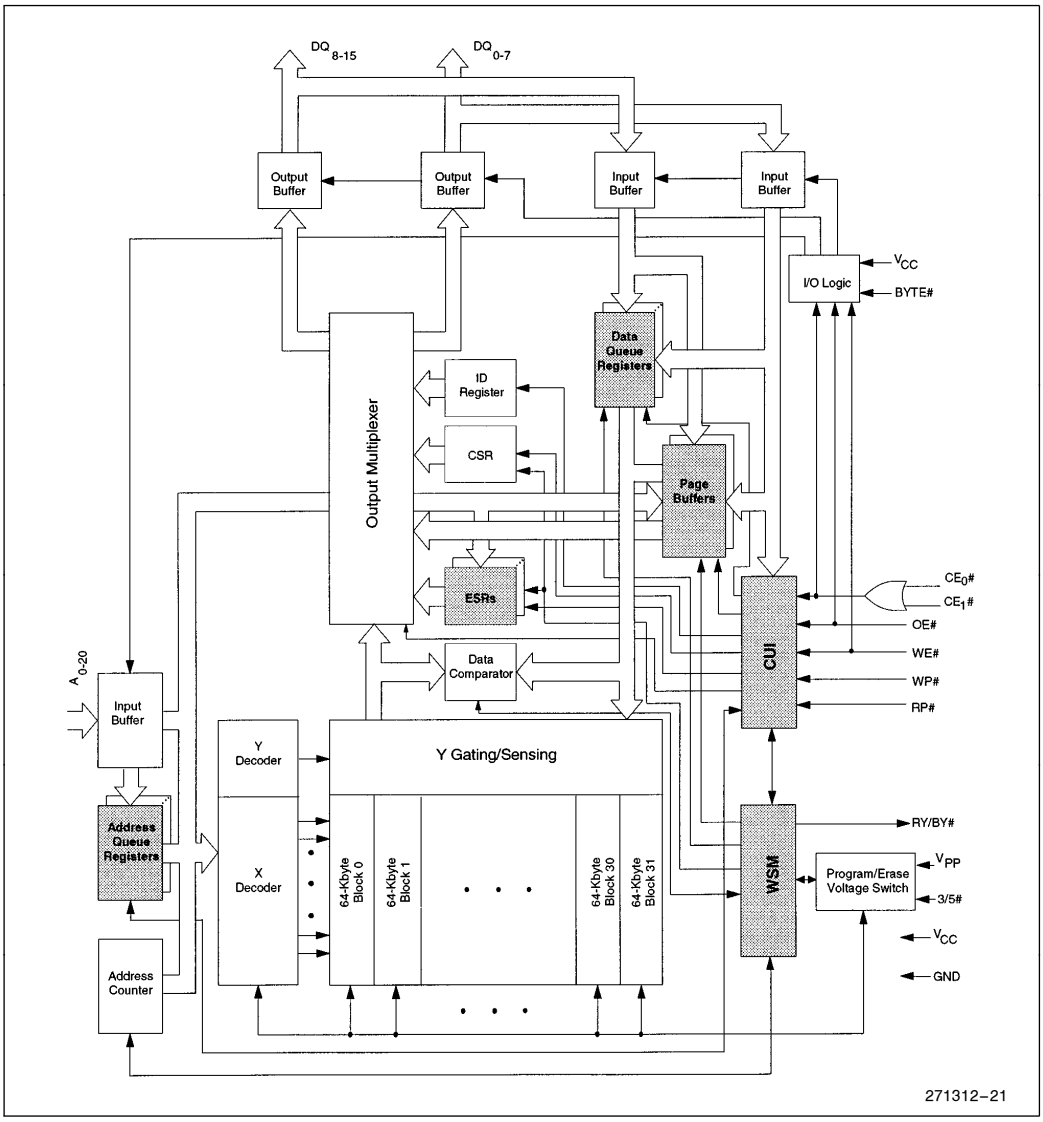


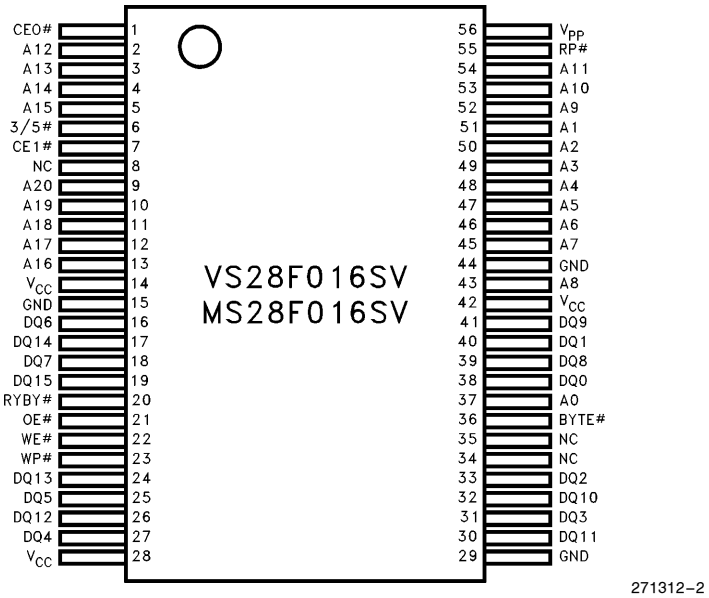
Figure 1. Block Diagram

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (i.e., the A_0 input buffer is turned off when BYTE# is high).
A_1 - A_{15}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 64-Kbyte block. A_{6-15} selects 1 of 1024 rows, and A_{1-5} selects 16 of 512 columns. These addresses are latched during Data Writes.
A_{16} - A_{20}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0 - DQ_7	INPUT/OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8 - DQ_{15}	INPUT/OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 Data-Write operations. Outputs array, buffer or identifier data in the appropriate read mode; not used for Status Register reads. Floated when the chip is de-selected or the outputs are disabled.
CE_0#, CE_1#	INPUT	**CHIP ENABLE INPUTS:** Activate the device's control logic, input buffers, decoders and sense amplifiers. With either CE_0# or CE_1# high, the device is de-selected and power consumption reduces to standby levels upon completion of any current Data-Write or Erase operations. Both CE_0#, CE_1# must be low to select the device. All timing specifications are the same for both signals. Device Selection occurs with the latter falling edge of CE_0# or CE_1#. The first rising edge of CE_0# or CE_1# disables the device.
RP#	INPUT	**RESET/POWER-DOWN:** RP# low places the device in a Deep Power-Down state. All circuits that consume static power, even those circuits enabled in standby mode, are turned off. When returning from Deep Power-Down, a recovery time of t_{PHQV} at 5.0V V_{CC} is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status Registers return to ready (with all status flags cleared). Exit from Deep Power-Down places the device in read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high. **NOTE:** CE_x# overrides OE#, and OE# overrides WE#.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge. Page Buffer addresses are latched on the falling edge of WE#.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# floating indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or erase is suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE_0#, CE_1# are high), except if a RY/BY# Pin Disable command is issued.
WP#	INPUT	**WRITE PROTECT:** Erase blocks can be locked by writing a nonvolatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent data writes or erases. When WP# is high, all blocks can be written or erased regardless of the state ot the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. Address A_0 selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A_0 input buffer. Address A_1, then becomes the lowest order address.
3/5#	INPUT	**3.3/5.0 VOLT SELECT:** 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. **NOTE:** Reading the array with 3/5# high in a 5.0V system could damage the device. Reference the power-up and reset timings (Section 5.7) for 3/5# switching delay to valid data.
V_{PP}	SUPPLY	**WRITE/ERASE POWER SUPPLY (12.0V ±0.6V, 5.0V ±0.5V):** For erasing memory array blocks or writing words/bytes/pages into the flash array. V_{PP} = 5.0V ±0.5V eliminates the need for a 12V converter, while connection to 1 2.0V ±0.6V maximizes Write/Erase Performance. **NOTE:** Successful completion of write and erase attempts is inhibited with V_{PP} at or below 1.5V. Write and erase attempts with V_{PP} between 1.5V and 4.5V, between 5.5V and 11.4V, and above 12.6V produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ±0.45V, 5.0V ±0.5V, 5.0 ±0.25V):** To switch 3.3V to 5.0V (or vice versa), first ramp V_{CC} down to GND, and then power to the new V_{CC} voltage. Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** Lead may be driven or left floating.



24mm x 13.5mm 0.8mm Lead Pitch

Top View

NOTE:
56-Lead SSOP Mechanical Diagrams and dimensions are shown at the end of this data sheet.

Figure 2. SSOP Pinout Configuration

3.0 MEMORY MAPS

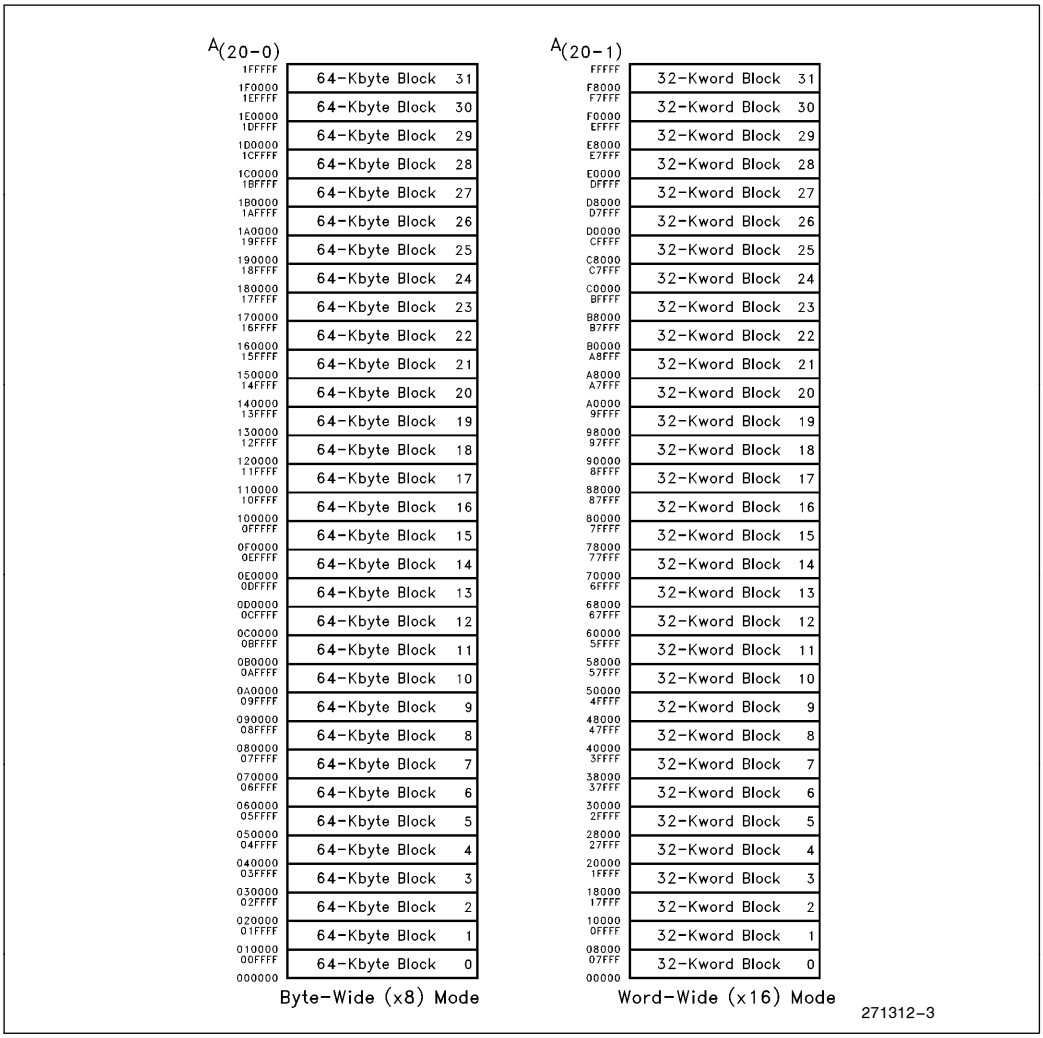


Figure 3. VS/MS28F016SV Memory Maps (Byte-Wide and Word-Wide Modes)

3.1 Extended Status Registers Memory Map

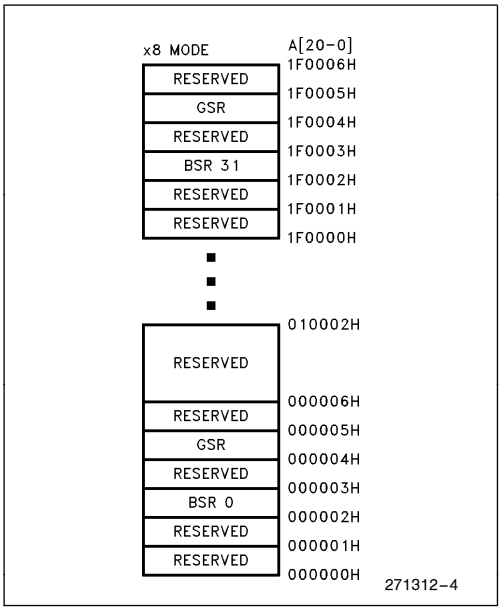


Figure 4. Extended Status Register Memory Map (Byte-Wide Mode)

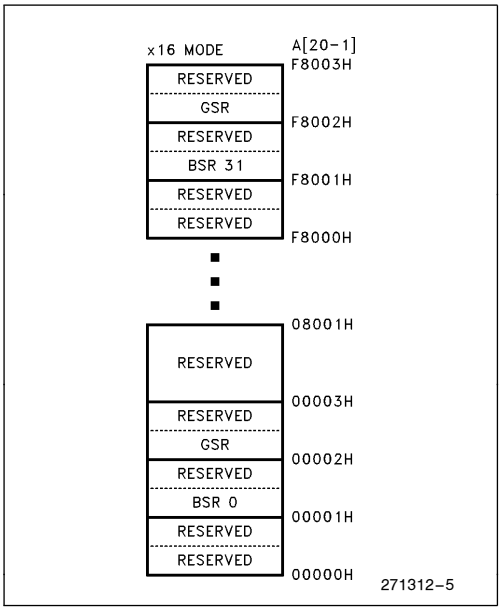


Figure 5. Extended Status Register Memory Map (Word-Wide Mode)

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE_1#	CE_0#	OE#	WE#	A_1	DQ_{0-15}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	0089H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	66A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

4.2 Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE_1#	CE_0#	OE#	WE#	A_0	DQ_{0-7}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	89H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0H	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

NOTES:
1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}.
2. RY/BY# output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode. RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ±0.2V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide device manufacturer codes in x8 and x16 modes respectively. A_0 and A_1 at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for Erase, Data Write, or Lock-Block operations can only be completed successfully when $V_{PP} = V_{PPH1}$or $V_{PP} = V_{PPH2}$.
6. While the WSM is running, RY/BY# in level-mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations. For example, a Status Register read during a Write operation.

4.3 VE28F008 and M28F008 Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data(4)	Oper	Addr	Data(4)
Read Array		Write	X	xxFFH	Read	AA	AD
Intelligent Identiier	1	Write	X	xx90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	xx70H	Read	X	CSRD
Clear Status Register	3	Write	X	xx50H			
Word/Byte Write		Write	X	xx40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	xx10H	Write	WA	WD
Block Erase/Confirm		Write	X	xx20H	Write	BA	xxD0H
Erase Suspend/Resume		Write	X	xxB0H	Write	X	xxD0H

ADDRESS
AA = Array Address
BA = Block Address
IA = Identitier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the Intelligent Identifier command, two Read operations access the manutacturer and device signature codes.
2. The CSR is automatically available after device enters data write, erase, or suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5, BSR.4 and BSR.2 bits. See Status Register definitions.
4. The upper byte of the data bus (DQ_{8-15}) during command writes is a ''Don't Care'' in x16 operation of the device.

4.4 VS/MS28F016SV—Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data[13]	Oper	Addr	Data[13]	Oper	Addr	Data
Read Extended Status Register		1	Write	X	xx71H	Read	RA	GSRD BSRD			
Page Buffer Swap		7	Write	X	xx72H						
Read Page Buffer			Write	X	xx75H	Read	PA	PD			
Single Load to Page Buffer			Write	X	xx74H	Write	PA	PD			
Sequential Load to Page Buffer	x8	4,6,10	Write	X	xxE0H	Write	X	BCL	Write	X	BCH
	x16	4,5,6,10	Write	X	xxE0H	Write	X	WCL	Write	X	WCH
Page Buffer Write to Flash	x8	3,4,9,10	Write	X	xx0CH	Write	A_0	BC(L,H)	Write	WA	BC(H,L)
	x16	4,5,10	Write	X	xx0CH	Write	X	WCL	Write	WA	WCH
Two-Byte Write	x8	3	Write	X	xxFBH	Write	A_0	WD(L,H)	Write	WA	WD(H,L)
Lock Block/ Confirm			Write	X	xx77H	Write	BA	xxD0H			
Upload Status Bits/Confirm		2	Write	X	xx97H	Write	X	xxD0H			
Upload Device Information/ Confirm		11	Write	X	xx99H	Write	X	xxD0H			
Erase All Unlocked Blocks/Confirm			Write	X	xxA7H	Write	X	xxD0H			
RY/BY# Enable to Level-Mode		8	Write	X	xx96H	Write	X	xx01H			
RY/BY# Pulse-On-Write		8	Write	X	xx96H	Write	X	xx02H			
RY/BY# Pulse-On-Erase		8	Write	X	xx96H	Write	X	xx03H			
RY/BY# Disable		8	Write	X	xx96H	Write	X	xx04H			
RY/BY# Pulse-On-Write/Erase		8	Write	X	xx96H	Write	X	xx05H			
Sleep		12	Write	X	xxF0H						
Abort			Write	X	xx80H						

ADDRESS
BA = Block Address
PA = Page Butter Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
PD = Page Buffer Data
BSRD = BSR Data
GSRD = GSR Data

WC (L,H) = Word Count (Low, High)
BC (L,H) = Byte Count (Low, High)
WD (L,H) = Write Data (Low, High)

NOTES:
1. RA can be the GSR address or any BSR address. See Figures 4 and 5 for Extended Status Register memory maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. A_0 is automatically complemented to load second byte of data. BYTE# must be at V_{IL}. A_0 value determines which WD/BC is supplied first: A_0 = 0 looks at the WDL/BCL, A_0 = 1 looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-byte (128-word) Page Buffer size, and to avoid writing the Page Buffer contents to more than one 256-byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In x16 mode, only the lower byte DQ_{0-7} is used for WCL and WCH. The upper byte DQ_{8-15} is a don't care.
6. PA and PD (whose count is given in cycles 2 and 3) are supplied starting in the fourth cycle, which is not shown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure RY/BY# output to one of two pulse-modes or enable and disable the RY/BY# function.
9. Write address, WA, is the Destination address in the flash array which must match the Source address in the Page Buffer. Refer to the 16-Mbit Flash Product Family User's Manual.
10. BCL = 00H corresponds to a byte count of 1. Similarly, WCL = 00H corresponds to a word count of 1.
11. After writing the Upload Device Information command and the Confirm command, the following information is output at Page Buffer addresses specified below:

Address	Information
06H, 07H (Byte Mode)	Device Revision Number
03H (Word Mode)	Device Revision Number
1EH (Byte Mode)	Device Configuration Code
0FH (DQ_{0-7}) (Word Mode)	Device Configuration Code
1FH (Byte Mode)	Device Proliferation Code (01H)
0FH (DQ_{8-15}) (Word Mode)	Device Proliferation Code (01H)

A page buffer swap followed by a page buffer read sequence is necessary to access this information. The contents of all other Page Buffer locations, after the Upload Device Information command is written, are reserved for future implementation by Intel Corporation. See Section 4.8 for a description of the Device Configuration Code. This code also corresponds to data written to the 28F016SV after writing the RY/BY# Reconfiguration command.
12. To ensure that the 28F0165V's power consumption during Sleep Mode reaches the deep power-down current level, the system also needs to de-select the chip by taking either or both CE_0# or CE_1# high.
13. The upper byte of the data bus (DQ_{8-15}) during command wntes is a Don't Care in x16 operation of the device.

4.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS
- 1 = Ready
- 0 = Busy

CSR.6 = ERASE-SUSPEND STATUS
- 1 = Erase Suspended
- 0 = Erase In Progress/Completed

CSR.5 = ERASE STATUS
- 1 = Error In Block Erasure
- 0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS
- 1 = Error in Data Write
- 0 = Data Write Successful

CSR.3 = V_{PP} STATUS
- 1 = V_{PP} Error Detect, Operation Abort
- 0 = V_{PP} OK

CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use; mask them out when polling the CSR.

NOTES:

RY/BY# output or WSMS bit must be checked to determine completion of an operation (Erase, Erase Suspend, or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

If DWS and ES are set to ‘‘1’’ during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}’s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPLK}(max) and V_{PPH1}(min) and between V_{PPH1}(max) and V_{PPH2}(min) and above V_{PPH_2}(max).

4.6 Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

	NOTES:
GSR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (Block Lock, Suspend, any RY/BY# reconfiguration, Upload Status Bits, Erase or Data Write) before the appropriate Status bit (OSS or DOS) is checked for success.
GSR.6 = OPERATION SUSPEND STATUS 1 = Operation Suspended 0 = Operation in Progress/Completed	
GSR.5 = DEVICE OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running	
GSR.4 = DEVICE SLEEP STATUS 1 = Device in Sleep 0 = Device Not in Sleep	
MATRIX 5/4	
0 0 = Operation Successful or Currently Running	If operation currently running, then GSR.7 = 0.
0 1 = Device in Sleep mode or Pending Sleep	If device pending sleep, then GSR.7 = 0.
1 0 = Operation Unsuccessful	
1 1 = Operation Unsuccessful or Aborted	Operation aborted: Unsuccessful due to Abort command.
GSR.3 = QUEUE STATUS 1 = Queue Full 0 = Queue Available	
GSR.2 = PAGE BUFFER AVAILABLE STATUS 1 = One or Two Page Buffers Available 0 = No Page Buffer Available	The device contains two Page Buffers.
GSR.1 = PAGE BUFFER STATUS 1 = Selected Page Buffer Ready 0 = Selected Page Buffer Busy	Selected Page Buffer is currently busy with WSM operation
GSR.0 = PAGE BUFFER SELECT STATUS 1 = Page Buffer 1 Selected 0 = Page Buffer 0 Selected	

NOTE:
1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

4.7 Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	VPPL	R
7	6	5	4	3	2	1	0

	NOTES:
BSR.7 = BLOCK STATUS 1 = Ready 0 = Busy	[1] RY/BY# output or BS bit must be checked to determine completion of an operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bits (BOS, BLS) is checked for success.
BSR.6 = BLOCK LOCK STATUS 1 = Block Unlocked for Write/Erase 0 = Block Locked for Write/Erase	
BSR.5 = BLOCK OPERATION STATUS 1 = Operation Unsuccessful 0 = Operation Successful or Currently Running	
BSR.4 = BLOCK OPERATION ABORT STATUS 1 = Operation Aborted 0 = Operation Not Aborted	The BOAS bit will not be set until BSR.7 = 1.
MATRIX 5/4 0 0 = Operation Successful or Currently Running 0 1 = Not a Valid Combination 1 0 = Operation Unsuccessful 1 1 = Operation Aborted	Operation halted via Abort command.
BSR.3 = QUEUE STATUS 1 = Queue Full 0 = Queue Available	
BSR.2 = V_{PP} STATUS 1 = V_{PP} Error Detect, Operation Abort 0 = V_{PP} OK	
BSR.1 = V_{PP} LEVEL 1 = V_{PP} Detected at 5.0V ±10% 0 = V_{PP} Detected at 12.0V ±5%	BSR.1 is not guaranteed to report accurate feedback between the V_{PPH1} and V_{PPH2} voltage ranges. Writes and erases with V_{PP} between V_{PPLK}(max) and V_{PPH1} (min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max) produce spurious results and should not be attempted. BSR.1 was a RESERVED bit on the 28F016SA.
BSR.0 = RESERVED FOR FUTURE ENHANCEMENTS This bit is reserved for future use; mask it out when polling the BSRs.	

NOTE:
1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

4.8 Device Configuration Code

R	R	R	R	R	RB2	RB1	RB0
7	6	5	4	3	2	1	0

DCC.2-DCC.0 = RY/BY# CONFIGURATION (RB2-RB0)
- 001 = Level Mode (Default)
- 010 = Pulse-On-Write
- 011 = Pulse-On-Erase
- 100 = RY/BY# Disabled
- 101 = Pulse-On-Write/Erase

DCC.7-DCC.3 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use; mask them out when reading the Device Configuration Code. Set these bits to ''0'' when writing the desired RY/BY# configuration to the device.

NOTES:
Undocumented combinations of RB2-RB0 are reserved by Intel Corporation for future implementations and should not be used.

5.0 ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

5.1 Absolute Maximum Ratings*

Temperature Under Bias
—SE1 . . . . . −55°C to +125°C
—SE2 . . . . . −40°C to +125°C

Storage Temperature . . . . . −65° to +125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3V ±0.15V Systems(4)

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
T_{CSE2}	Operating Temperature, SE2		−40	+125	°C	
T_{CSE1}	Operating Temperature, SE1		−55	+125	°C	
V_{CC}	V_{CC} with Respect to GND	1	−0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	1,2	−0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	1,5	−0.5	V_{CC} +0.5	V	
I	Current into any Non-Supply Pin	5		±30	mA	
I_{OUT}	Output Short Circuit Current	3		100	mA	

V_{CC} = 5.0V ±0.5V, V_{CC} = 5.0V ±0.25V Systems(4, 5)

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
T_{CSE2}	Operating Temperature, SE2		−40	+125	°C	
T_{CSE1}	Operating Temperature, SE1		−55	+125	°C	
V_{CC}	V_{CC} with Respect to GND	1	−0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	1,2	−0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	1,5	−2.0	7.0	V	
I	Current into any Non-Supply Pin	5		±30	mA	
I_{OUT}	Output Short Circuit Current	3		100	mA	

NOTES:
1. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.
5. This specification also applies to pin marked "NC".
6. 5% V_{CC} specifications refer to the VS/MS28F016SV-80 in its high speed test configuration.

5.2 Capacitance

For a 3.3V ±0.15V System:

Sym	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = 25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = 25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1,2		50	pF	For V_{CC} = 3.3V ±0.15V
	Equivalent Load Timing Circuit			2.5	ns	50Ω transmission line delay

For a 5.0V System:

Sym	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A=25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = 25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1,2		100	pF	For V_{CC} = 5.0V ±0.5V
				30	pF	For V_{CC} = 5.0V ±0.25V
	Equivalent Testing Load Circuit for V_{CC} ±10%			2.5	ns	25Ω transmission line delay
	Equivalent Testing Load Circuit for V_{CC} ±5%			2.5	ns	85Ω transmission line delay

NOTES:
1. Sampled, not 100% tested. Guaranteed by design.
2. To obtain iBIS models for the VS/MS28F016SV, please contact your local Intel/Distribution Sales Office.

5.3 Timing Nomenclature

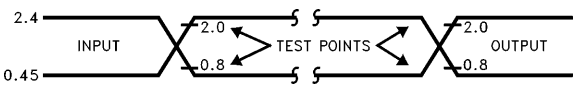
All 3.3V system timings are measured from where signals cross 1.5V.

For 5.0V systems use the standard JEDEC cross point definitions.

Each timing parameter consists of 5 characters. Some common examples are defined as follows:

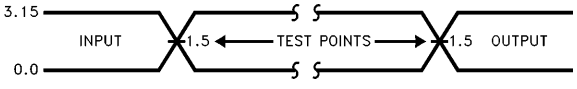
t_{CE}	t_{ELQV} time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)
t_{OE}	t_{GLQV} time(t) from OE # (G) going low (L) to the outputs (Q) becoming valid (V)
t_{ACC}	t_{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
t_{AS}	t_{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)
t_{DH}	t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but not Necessarily Valid
F	BYTE# (Byte Enable)	Z	High Impedance
G	OE# (Output Enable)		
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready Busy)		
V	Any Voltage Level		
Y	3/5# Pin		
5V	V_{CC} at 4.5V Minimum		
3V	V_{CC} at 3.15V Minimum		



AC test inputs are driven at V_{OH} (2.4 VTTL) for a Logic "1" and V_{OL} (0.45 VTTL) for a Logic "0." Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

Figure 6. Transient Input/Output Reference Waveform for V_{CC} = 5.0V ±10% (Standard Testing Configuration)



AC test inputs are driven at 3.15V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

Figure 7. Transient Input/Output Reference Waveform (V_{CC} = 3.3V ±0.15V) High Speed Reference Waveform (V_{CC} = 5.0V ±5%)

NOTE:
1. Testing characteristics for VS/MS28F016SV-085 (Standard Testing Configuration) and VS/MS28F016SV-100.

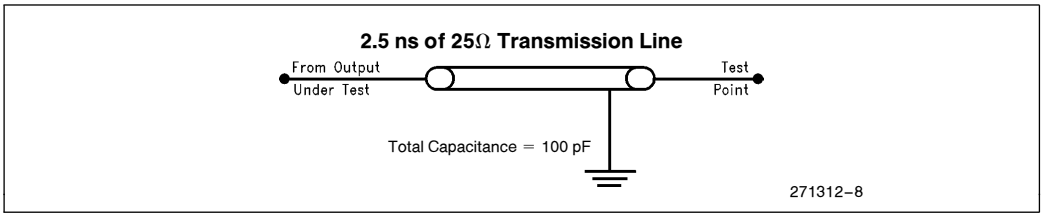


Figure 8. Transient Equivalent Testing Load Circuit (V_{CC} = 5.0V ±10%)

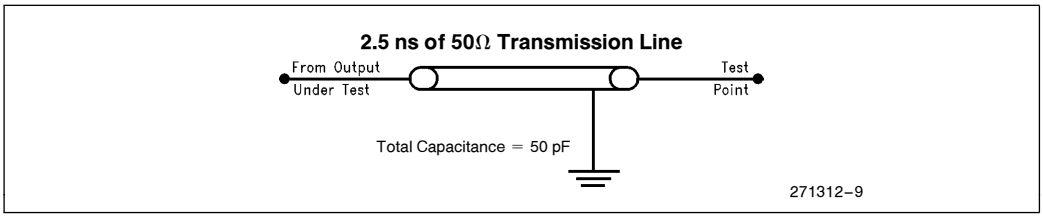


Figure 9. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3V ±0.15V)

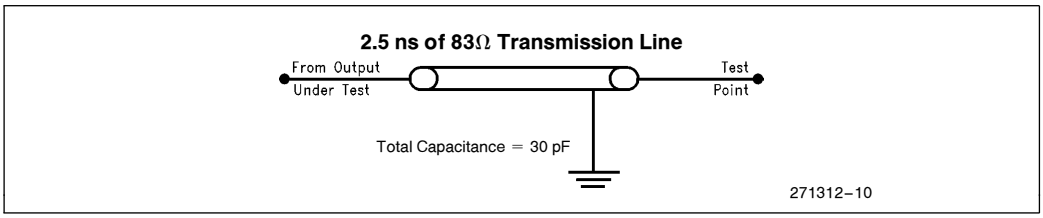


Figure 10. High Speed Transient Equivalent Testing Load Circuit (V_{CC} = 5.0V ±5%)

5.4 DC Characteristics

V_{CC} = 3.3V ±0.15V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Load Current	1		±1	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1		±10	µA	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,5		130	µA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ±0.2V BYTE#, WP#, 3/5# = V_{CC} ±0.2V or GND ±0.2V
				4	mA	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		50	µA	RP# = GND ±0.2V BYTE# = V_{CC} ±0.2V or GND ±0.2V
$I_{CCR}1$	V_{CC} Read Current	1,4,5		60	mA	V_{CC} = V_{CC} Max CMOS: CE_0#, CE_1# = GND ±0.2V BYTE# = GND ±0.2V or V_{CC} ±0.2V Inputs = GND ±0.2V or V_{CC} ±0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH} INPUTS = V_{IL} or V_{IH}, f = 8 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current	1,4,5,6		40	mA	V_{CC} = V_{CC} Max CMOS: CE_0#, CE_1# = GND ±0.2V BYTE# = GND ±0.2V or V_{CC} ±0.2V Inputs = GND ±0.2V or V_{CC} ±0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH} INPUTS = V_{IL} or V_{IH}, f = 4 MHz, I_{OUT} = 0 mA

5.4 DC Characteristics (Continued)

V_{CC} = 3.3V ±0.3V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
I_{CCW}	V_{CC} Write Current	1,6		12	mA	Word/Byte Write in Progress V_{PP} = 12.0V ±5%
				17	mA	Word/Byte Write in Progress V_{PP} = 5.0V ±10%
I_{CCE}	V_{CC} Block Erase Current	1,6		12	mA	Block Erase in Progress V_{PP} = 12.0V ±5%
				17	mA	Block Erase in Progress V_{PP} = 5.0V ±10%
I_{CCES}	V_{CC} Erase Suspend Current	1,2		6	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPS} I_{PPR}	V_{PP} Standby/Read Current	1		±100	µA	$V_{PP} \leq V_{CC}$
				200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		50	µA	RP# = GND ±0.2V
I_{PPW}	V_{PP} Write Current	1		15	mA	V_{PP} = 12.0V ±5% Word/Byte Write in Progress
				25	mA	V_{PP} = 5.0V ±10% Word/Byte Write in Progress
I_{PPE}	V_{PP} Erase Current	1		10	mA	V_{PP} = 12.0V ±5% Block Erase in Progress
				20	mA	V_{PP} = 5.0V ±10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		200	µA	V_{PP} = V_{PPH1} or V_{PPH2}, Block Erase Suspended
V_{IL}	Input Low Voltage		−0.3	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = V_{CC} Min and I_{OL} = 4 mA

5.4 DC Characteristics (Continued)

$V_{CC} = 3.3V \pm 0.15V$, $T_{CSE2} = -40°C$ to $+125°C$, $T_{CSE1} = -55°C$ to $+125°C$

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
$V_{OH}1$	Output High Voltage		2.4		V	$I_{OH} = -2.0$ mA $V_{CC} = V_{CC}$ Min
$V_{OH}2$			$V_{CC} - 0.2$		V	$I_{OH} = -100\ \mu A$ $V_{CC} = V_{CC}$ Min
V_{PPLK}	V_{PP} Erase/Write Lock Voltage	3	0.0	1.8	V	
V_{PPH1}	V_{PP} during Write/Erase Operations	3	4.5	5.5	V	
V_{PPH2}	V_{PP} during Write/Erase Operations	3	11.4	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		1.8		V	

NOTES:
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block Erases, Word/Byte Writes and Lock Block operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min) and above V_{PPH2}(max).
4. Automatic Power Savings (APS) reduces I_{CCR} to less than 3 mA in static operation.
5. CMOS Inputs are either $V_{CC} \pm 0.2V$ or GND $\pm 0.2V$. TTL Inputs are either V_{IL} or V_{IH}.
6. Sampled, but not 100% tested. Guaranteed by design.

5.5 DC Characteristics

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Load Current	1		±1	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1		±10	µA	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,5		130	µA	V_{CC} = V_{CC} Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP# = V_{CC} ± 0.2V or GND ±0.2V
				4	mA	V_{CC} = V_{CC} Max CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		50	µA	RP# = GND ±0.2V BYTE# = V_{CC} ±0.2V or GND ±0.2V
$I_{CCR}1$	V_{CC} Read Current	1,4,5		135	mA	V_{CC} = V_{CC} Max, CMOS:CE_0#, CE_1# = GND ± 0.2V BYTE# = GND ±0.2V or V_{CC} ±0.2V Inputs = GND ±0.2V or V_{CC} ±0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH}, f = 10 MHz, I_{OUT} = 0 mA
$I_{CCR}2$	V_{CC} Read Current	1,4,5,6		90	mA	V_{CC} = V_{CC} Max, CMOS:CE_0#, CE_1# = GND ± 0.2V BYTE# = GND ±0.2V or V_{CC} ±0.2V Inputs = GND ±0.2V or V_{CC} ±0.2V TTL: CE_0#, CE_1# = V_{IL}, BYTE# = V_{IL} or V_{IH}, Inputs = V_{IL} or V_{IH}, f = 5 MHz, I_{OUT} = 0 mA

5.5 DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
I_{CCW}	V_{CC} Write Current	1,6		35	mA	Word/Byte in Progress V_{PP} = 12.0V ±5%
				40	mA	Word/Byte in Progress V_{PP} = 5.0V ±10%
I_{CCE}	V_{CC} Block Erase Current	1,6		25	mA	Block Erase in Progress V_{PP} = 12.0V ±5%
				30	mA	Block Erase in Progress V_{PP} = 5.0V ±10%
I_{CCES}	V_{CC} Erase Suspend Current	1,2		10	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPS} I_{PPR}	V_{PP} Standby/Read Current	1		±100	µA	$V_{PP} \leq V_{CC}$
				200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		50	µA	RP# = GND ±0.2V
I_{PPW}	V_{PP} Write Current	1,6		12	mA	V_{PP} = 12.0V ±5% Word/Byte Write in Progress
				22	mA	V_{PP} = 5.0V ±10% Word/Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current	1,6		10	mA	V_{PP} = 12.0V ±5% Block Erase in Progress
				20	mA	V_{PP} = 5.0V ±10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		200	µA	V_{PP} = V_{PPH1} or V_{PPH2}, Block Erase Suspended
V_{IL}	Input Low Voltage	6	−0.5	0.8	V	
V_{IH}	Input High Voltage	6	2.0	V_{CC} +0.5	V	

5.5 DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, 5.0V ± 0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Min	Max	Units	Test Conditions
V_{OL}	Output Low Voltage	6		0.45	V	V_{CC} = V_{CC} Min I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage	6	0.85 V_{CC}		V	I_{OH} = −2.5 mA V_{CC} = V_{CC} Min
$V_{OH}2$		6	V_{CC} −0.4			I_{OH} = −100 µA V_{CC} = V_{CC} Min
V_{PPLK}	V_{PP} Write/Erase Lock Voltage	3,6	0.0	1.8	V	
V_{PPH1}	V_{PP} during Write/Erase Operations		4.5	5.5	V	
V_{PPH2}	V_{PP} during Write/Erase Operations		11.4	12.6	V	
V_{LKO}	V_{CC} Write/Erase Lock Voltage		1.8		V	

NOTES:
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of $I_{CCES}$and I_{CCR}.
3. Block Erases, Word/Byte Writes and Lock Block operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min) and above V_{PPH2}(max).
4. Automatic Power Saving (APS) reduces I_{CCR} to less than 1 mA in Static operation.
5. CMOS Inputs are either V_{CC} ±0.2V or GND ±0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. Sampled, not 100% tested. Guaranteed by design.

5.6 AC Characteristics—Read Only Operations[1]

V_{CC} = 3.3V ±0.15V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions					Units
Sym	Parameter	Notes	Min	Max	
t_{AVAV}	Read Cycle Time		120		ns
t_{AVQV}	Address to Output Delay (T_{ACC})			120	ns
t_{ELQV}	CE# to Output Delay (T_{CE})	2,7		120	ns
t_{PHQV}	RP# High to Output Delay			620	ns
t_{GLQV}	OE# to Output Delay (T_{OE})	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3,7	0		ns
t_{EHQZ}	CE# to Output in High Z	3,7		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		30	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3,7	0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		120	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3,7		5	ns

Extended Status Register Reads

Sym	Parameter	Notes	Min	Max	Units
t_{AVEL}	Address Setup to CE# Going Low	3,7,8,9	0		ns
t_{AVGL}	Address Setup to OE# Going Low	3,7,9	0		ns

5.6 AC Characteristics—Read Only Operations[1] (Continued)

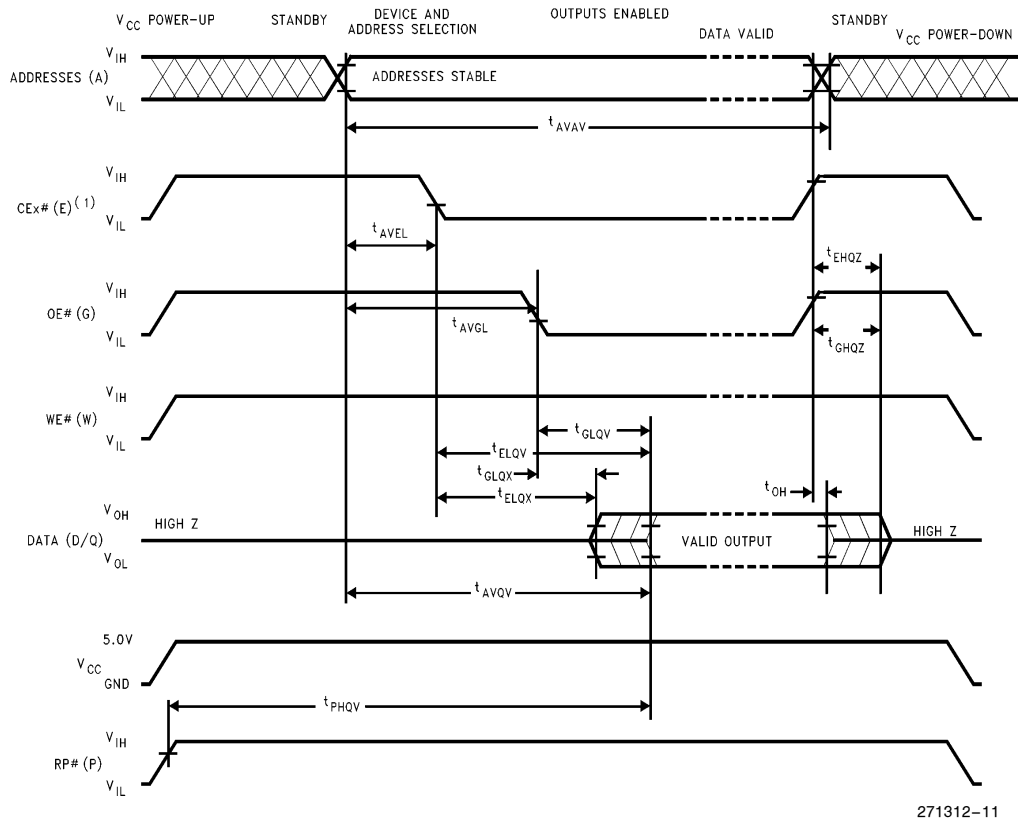
V_{CC} = 5.0V ±0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 30 pF
V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 100 pF

Versions[4]			VS/MS28F016SV-85 V_{CC} ±5%[5]		VS/MS28F016SV-85 V_{CC} ±10%[6]		VS/MS28F016SV-100 V_{CC} ± 10%		Unit
Sym	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	Read Cycle Time		80		85		100		ns
t_{AVQV}	Address to Output Delay (T_{ACC})			80		85		100	ns
t_{ELQV}	CE# to Output Delay (T_{CE})	2		80		85		100	ns
t_{PHQV}	RP# to Output Delay			400		480		480	ns
t_{GLQV}	OE# to Output Delay (T_{OE})	2		30		35		40	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	CE# to Output in High Z	3		25		30		35	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		0		ns
t_{GHQZ}	OE# to Output in High Z	3		25		30		35	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		80		85		100	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		25		30		35	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5		5		5	ns

Extended Status Register Reads

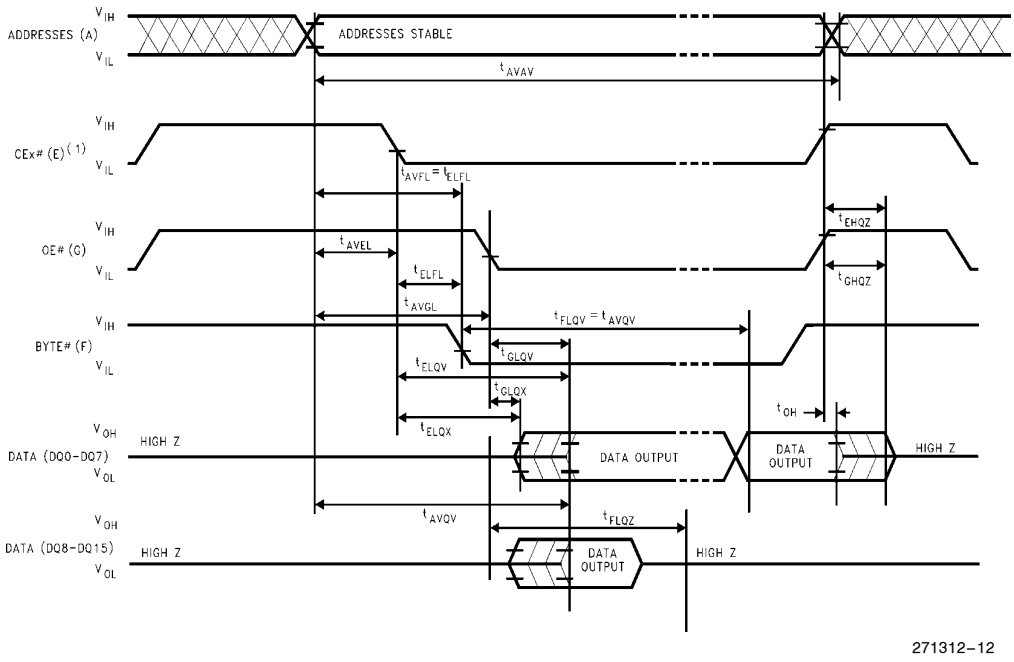
Sym	Parameter	Notes	Min	Max	Min	Max	Min	Max	Unit
t_{AVEL}	Address Setup to CE# Going Low	3,7,8,9	0		0		0		ns
t_{AVGL}	Address Setup to OE# Going Low	3,7,9	0		0		0		ns

NOTES:
1. See AC Input/Output Reference Waveforms for timing measurements, Figures 6 and 7.
2. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE#, without impacting t_{ELQV}.
3. Sampled, not 100% tested. Guaranteed by design.
4. Device speeds are defined as:
   80/85, 100 ns at V_{CC} = 5.0V equivalent to
   120 ns at V_{CC} = 3.3V
5. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
6. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.
7. CE_x# is defined as the latter of CE_0# or CE_1# going low, or the f.
8. This timing parameter is used to latch the correct BSR data onto the outputs.
9. The address setup requirement for Extended Status Register reads must only be met referenced to the falling edge of the last control signal to become active (CE_0#, CE_1#, or OE#). For example, if CE_0# or CE_1# are activated prior to OE# for an Extended Status Register read, specification t_{AVGL} must be met. On the other hand, if either CE_0# or CE_1# (or both) are activated after OE#, specification t_{AVEL} must be referenced.



NOTE:
CEx# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 11. Read Timing Waveforms



NOTE:
CEx# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 12. BYTE# Timing Waveforms

5.7 Power-Up and Reset Timings

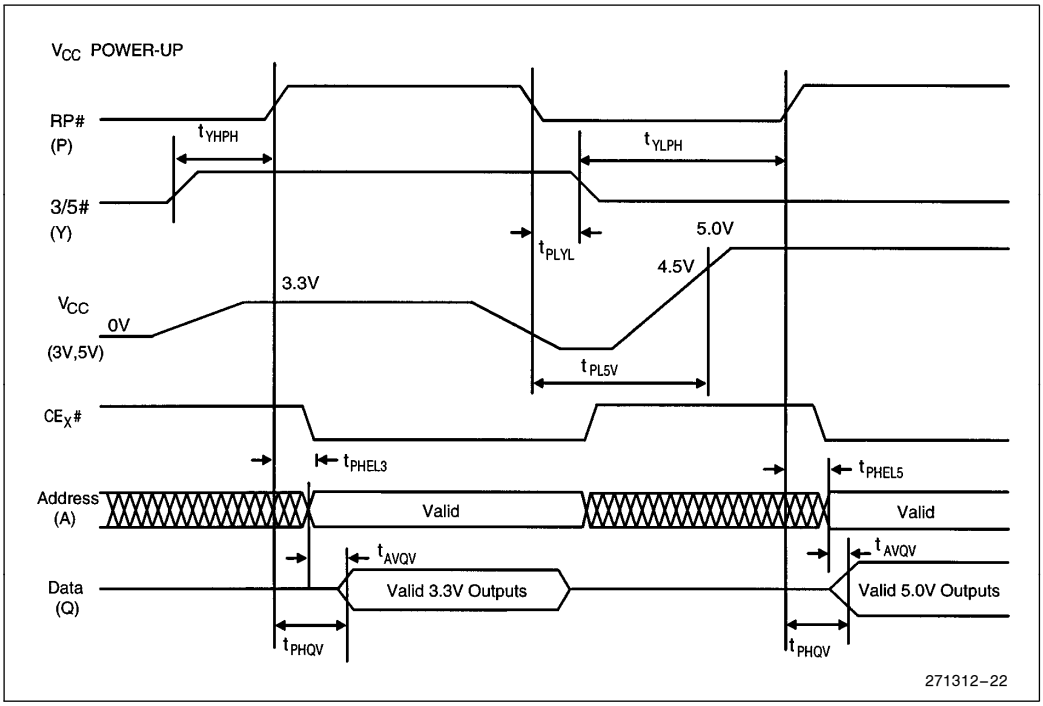


Figure 13. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Notes	Min	Max	Unit
t_{PLYL} t_{PLYH}	RP# Low to 3/5# Low (High)		0		μs
t_{YLPH} t_{YHPH}	3/5# Low (High) to RP# High	1	2		μs
t_{PL5V} t_{PL3V}	RP# Low to V_{CC} at 4.5V minimum (to V_{CC} at 3.0V min or 3.6V max)	2	0		μs
t_{PHEL3}	RP# High to CE# Low (3.3V V_{CC})	1	405		ns
t_{PHEL5}	RP# High to CE# Low (5V V_{CC})	1	330		ns
t_{AVQV}	Address Valid to Data Valid for V_{CC} = 5V ±10%	3		70	ns
t_{PHQV}	RP# High to Data Valid for V_{CC} = 5V ±10%	3		400	ns

NOTES:
CE_0#, CE_1# and OE# are switched low after Power-Up.
1. The t_{YLPH} and/or t_{YHPH} times must be strictly followed to guarantee all other read and write specifications for the VS/MS28F016SV.
2. The power supply may start to switch concurrently with RP# going low.
3. The address access time and RP# high to data valid time are shown for 5.0V V_{CC} operation of the 28F016SV-085 (Standard Test Configuration). Refer to the AC Chracteristics—Read Only Operations for 3.3V V_{CC} and 5.0V V_{CC} (High Speed Test Configuration) values.

5.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

V_{CC} = 3.3V ±0.15V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions					Unit
Sym	Parameter	Notes	Min	Max	
t_{AVAV}	Write Cycle Time		120		ns
t_{VPWH}(1,2)	V_{PP} Setup to WE# Going High	3	100		ns
t_{PHEL}	RP# Setup to CE# Going Low	3,7	480		ns
t_{ELWL}	CE# Setup to WE# Going Low	3,7	10		ns
t_{AVWH}	Address Setup to WE# Going High	2,6	75		ns
t_{DVWH}	Data Setup to WE# Going High	2,6	75		ns
t_{WLWH}	WE# Pulse Width		75		ns
t_{WHDX}	Data Hold from WE# High	2	10		ns
t_{WHAX}	Address Hold from WE# High	2	10		ns
t_{WHEH}	CE# Hold from WE# High	3,7	10		ns
t_{WHWL}	WE# Pulse Width High		45		ns
t_{GHWL}	Read Recovery before Write	3	0		ns
t_{WHRL}	WE# High to RY/BY# Going Low	3		100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	3	480		ns
t_{WHGL}	Write Recovery before Read		95		ns
t_{QVVL}(1,2)	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0		µs
t_{WHQV}(1)	Duration of Word/Byte Write Operation	3,4,5,11	5		µs
t_{WHQV}(2)	Duration of Block Erase Operation	3,4	0.3	10	sec

5.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

(Continued)

V_{CC} = 5.0V ±0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 30 pF
V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 100 pF

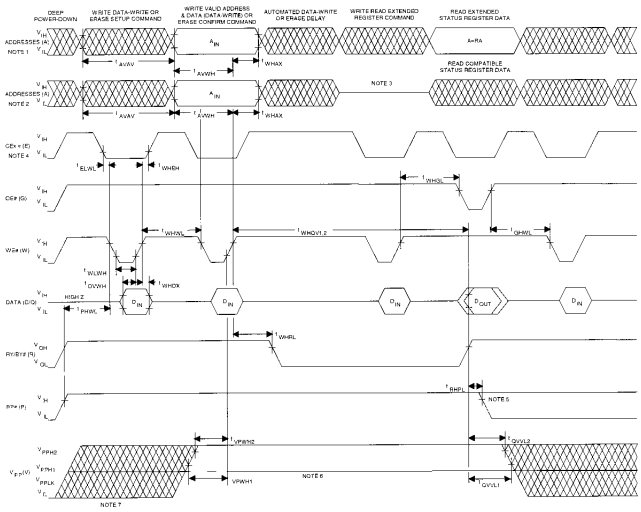
Versions			VS/MS28F016SV-85 V_{CC} ±5%		VS/MS28F016SV-85 V_{CC} ±10%		VS/MS28F016SV-100 V_{CC} ±10%		Unit
Sym	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	Write Cycle Time		80		85		100		ns
t_{VPWH}(1) t_{VPWH}(2)	V_{PP} Setup to WE# Going High	3	100		100		100		ns
t_{PHEL}	RP# Setup to CE# Going Low	3,7	480		480		480		ns
t_{ELWL}	CE# Setup to WE# Going Low	3,7	0		0		0		ns
t_{AVWH}	Address Setup to WE# Going High	2,6	50		50		50		ns
t_{DVWH}	Data Setup to WE# Going High	2,6	50		50		50		ns
t_{WLWH}	WE# Pulse Width		50		60		70		ns
t_{WHDX}	Data Hold from WE# High	2	10		10		10		ns
t_{WHAX}	Address Hold from WE# High	2	10		10		10		ns
t_{WHEH}	CE# Hold from WE# High	3,7	10		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		30		ns
t_{GHWL}	Read Recovery before Write	3	0		0		0		ns
t_{WHRL}	WE# High to RY/BY# Going Low	3		100		100		100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY # High	3	0		0		0		ns

5.8 AC Characteristics for WE#—Controlled Command Write Operations(1)

V_{CC} = 5.0V ±0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 30 pF
V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 100 pF
(Continued)

Versions			VS/MS28F016SV-85 V_{CC} ±5%		VS/MS28F016SV-85 V_{CC} ±10%		VS/MS28F016SV-100 V_{CC} ±10%		Unit
Sym	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PHWL}	RP# High Recovery to WE# Going Low	3	1		1		1		µs
t_{WHGL}	Write Recovery before Read		60		65		70		ns
t_{QVVL}(1) t_{QVVL}(2)	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0		0		0		µs
t_{WHQV}(1)	Duration of Word/Byte Write Operation	3,4,5,11	4.5		4.5		4.5		µs
t_{WHQV}(2)	Duration of Block Erase Operation	3,4	0.3	10	0.3	10	0.3	10	sec

NOTES:
1. Read timings during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, not 100% tested. Guaranteed by design.
4. Write/Erase durations are measured to valid Status Register (CSR) Data. V_{PP} = 12.0V ±0.6V
5. Word/Byte Write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all Command Write operations.
7. CE_x# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
8. Device speeds are defined as:
   80/85, 100 ns at V_{CC} = 5.0V equivalent to
   120 ns at V_{CC} = 3.3V
9. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
10. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.
11. The TBD information will be available in a technical paper. Please contact Intel's Application Hotline or your local sales office for more information.



271312–23

NOTES:
1. This address string depicts data write/erase cycles with corresponding verification via ESRD.
2. This address string depicts data write/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data write/erase operations.
4. CEx# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.
6. V_{PP} voltage during write/erase operations valid at both 12.0V and 5.0V.
7. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

Figure 14. AC Waveforms for Command Write Operations

5.9 AC Characteristics for CE# —Controlled Command Write Operations(1)

V_{CC} = 3.3V ±0.15V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions					Unit
Sym	Parameter	Notes	Min	Max	
t_{AVAV}	Write Cycle Time		120		ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480		ns
t_{VPEH}(1,2)	V_{PP} Setup to CE# Going High	3,7	100		ns
t_{WLEL}	WE# Setup to CE# Going Low	3,7	0		ns
t_{AVEH}	Address Setup to CE# Going High	2,6,7	75		ns
t_{DVEH}	Data Setup to CE# Going High	2,6,7	75		ns
t_{ELEH}	CE# Pulse Width	7	75		ns
t_{EHDX}	Data Hold from CE# High	2,7	10		ns
t_{EHAX}	Address Hold from CE# High	2,7	10		ns
t_{EHWH}	WE# hold from CE# High	3	10		ns
t_{EHEL}	CE# Pulse Width High	7	45		ns
t_{GHEL}	Read Recovery before Write	3	0		ns
t_{EHRL}	CE# High to RY/BY# Going Low	3,7		100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	3,7	480		ns
t_{EHGL}	Write Recovery before Read		95		ns
t_{QVVL}(1,2)	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0		µs
t_{EHQV}(1)	Duration of Word/Byte Write Operation	3,4,5,11	5		µs
t_{EHQV}(2)	Duration of Block Erase Operation	4	0.3	10	sec

5.9 AC Characteristics for CE#—Controlled Command Write Operations(1)

(Continued)
V_{CC} = 5.0V ±0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 30 pF
V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 100 pF

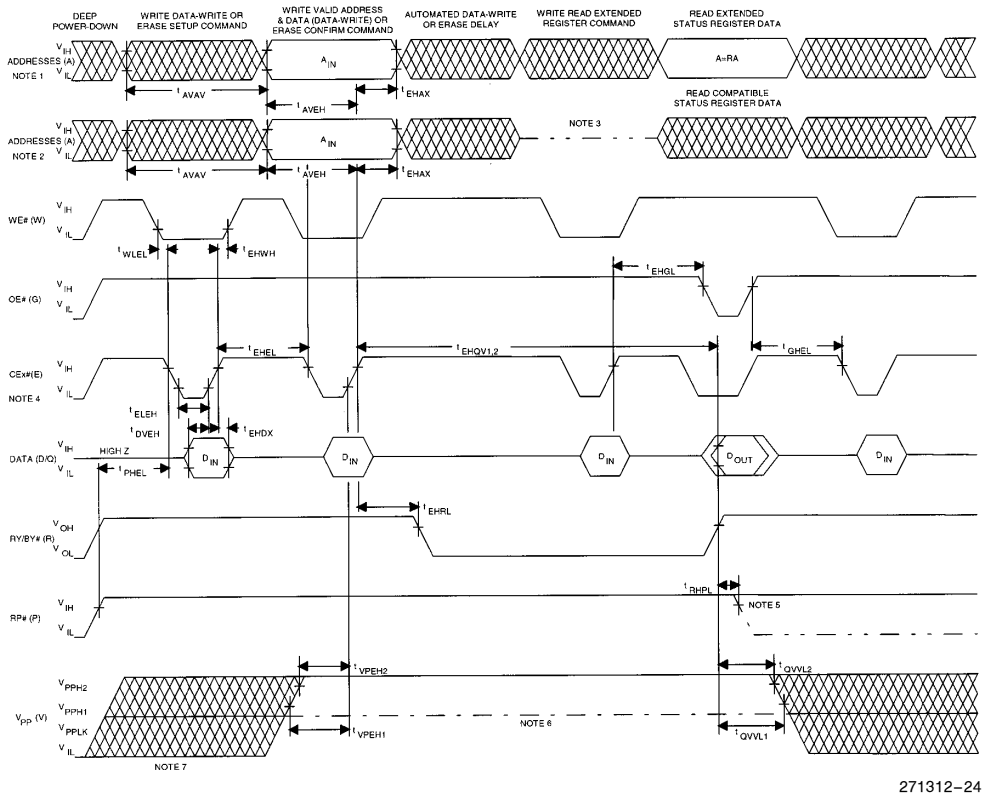
Versions(4)			VS/MS28F016SV-85		VS/MS28F016SV-85		VS/MS28F016SV-100		Unit
			V_{CC} ±5%		V_{CC} ±10%		V_{CC} ±10%		
Sym	Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		80		85		100		ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480		480		480		ns
t_{VPEH}(1,2)	V_{PP} Setup to CE# Going High	3,7	100		100		100		ns
t_{WLEL}	WE# Setup to CE# Going Low	3,7	0		0		0		ns
t_{AVEH}	Address Setup to CE# Going High	2,6,7	50		50		50		ns
t_{DVEH}	Data Setup to CE# Going High	2,6,7	50		50		50		ns
t_{ELEH}	CE# Pulse Width	7	50		60		70		ns
t_{EHDX}	Data Hold from CE# High	2,7	10		10		10		ns
t_{EHAX}	Address Hold from CE# High	2,7	10		10		10		ns
t_{EHWH}	WE Hold from CE# High	3,7	10		10		10		ns
t_{EHEL}	CE# Pulse Width High	7	30		30		30		ns
t_{GHEL}	Read Recovery before Write	3	0		0		0		ns
t_{EHRL}	CE# High to RY/BY# Going Low	3,7		100		100		100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0		0		0		ns

5.9 AC Characteristics for CE#—Controlled Command Write Operations(1)

V_{CC} = 5.0V ±0.25V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 30 pF
V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 100 pF
(Continued)

Versions(4)			VS/MS28F016SV-85		VS/MS28F016SV-85		VS/MS28F016SV-100		Unit
			V_{CC} ±5%		V_{CC} ±10%		V_{CC} ±10%		
Sym	Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{PHEL}	RP# High Recovery to CE# Going Low	3,7	1		1		1		µs
t_{EHGL}	Write Recovery before Read		60		65		70		ns
t_{QVVL}(1,2)	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data at RY/BY# High	3	0		0		0		µs
t_{EHQV}(1)	Duration of Word/Byte Write Operation	3,4,5,11	4.5		4.5		4.5		µs
t_{EHQV}(2)	Duration of Block Erase Operation	3,4	0.3	10	0.3	10	0.3	10	sec

NOTES:
1. Read timings during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, not 100% tested. Guaranteed by design.
4. Write/erase durations are measured to valid Status Data. V_{PP} = 12.0V ± 0.6V.
5. Word/Byte Write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all command write operations.
7. CE_x# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
8. Device speeds are defined as:
   80/85, 100 ns at V_{CC} = 5.0V equivalent to
   120 ns at V_{CC} = 3.3V
9. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
10. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.
11. The TBD information will be available in a technical paper. Please contact Intel's Application Hotline or your local sales office for more information.



NOTES:
1. This address string depicts data-write/erase cycles with corresponding verification via ESRD.
2. This address string depicts data-write/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data write/erase operations.
4. CEx# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above Read and Write cycles.
6. V_{PP} voltage during Write/Erase operations valid at both 12.0V and 5.0V.
7. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

Figure 15. Alternate AC Waveforms for Command Write Operations

5.10 AC Characteristics for WE#—Controlled Page Buffer Write Operations[1]

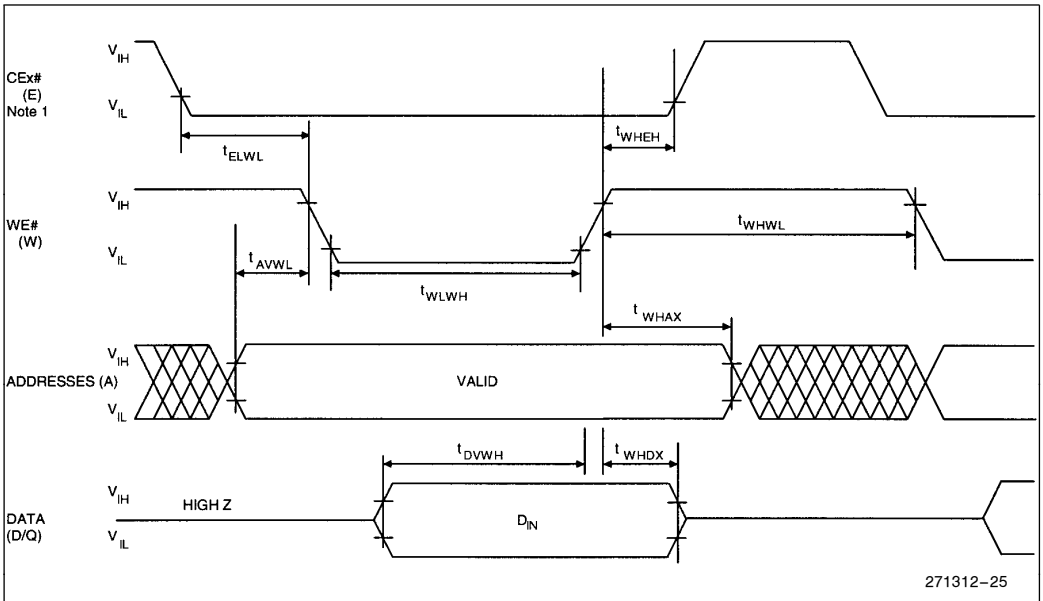
V_{CC} = 3.3V ±0.3V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions			28F016SV-120			Unit
Sym	Parameter	Notes	Min	Typ	Max	
t_{AVWL}	Address Setup to WE# Going Low	2	25			ns

V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions[3]		V_{CC} ±5%	28F016SV-080[4]						Unit
		V_{CC} ±10%	28F016SV-080[5]			28F016SV-085[5]			
Sym	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	
t_{AVWL}	Address Setup to WE# Going Low	2	15			15			ns

NOTES:
1. All other specifications for WE#—Controlled Write Operations can be found in section 5.8.
2. Address must be valid during the entire WE# low pulse.
3. Device speeds are defined as:
   80/85, 100 ns at V_{CC} = 5.0V equivalent to
   120 ns at V_{CC} = 3.3V
4. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
5. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.



NOTE:
1. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 16. WE#—Controlled Page Buffer Write Timing Waveforms (Loading Data to the Tape Buffer)

5.11 AC Characteristics for CE#—Controlled Page Buffer Write Operations(1)

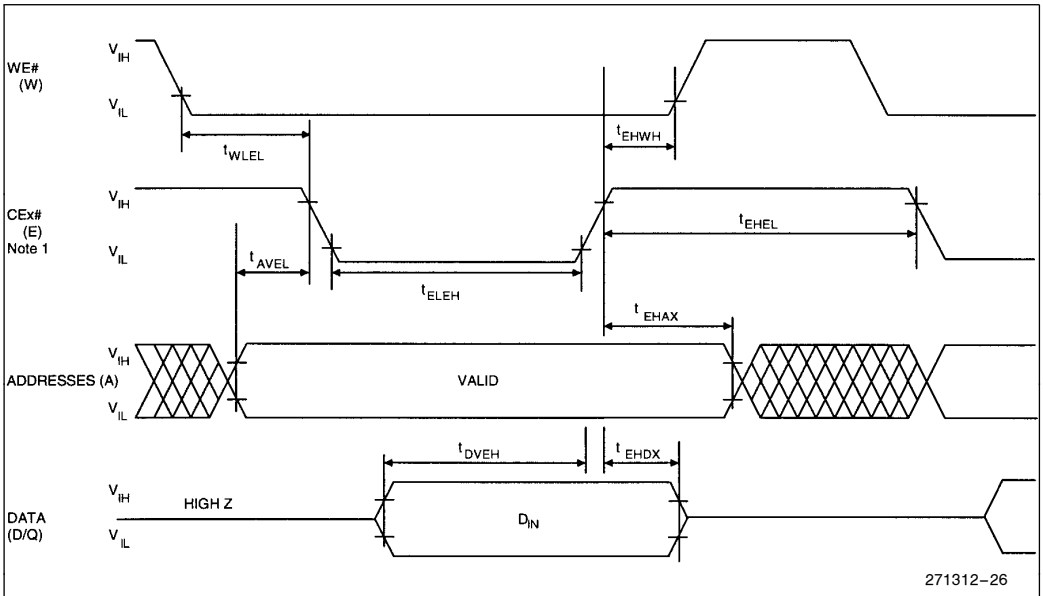
V_{CC} = 3.3V ±0.3V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions			28F016SV-120			Unit
Sym	Parameter	Notes	Min	Typ	Max	
t_{AVEL}	Address Setup to CE# Going Low	2, 3	25			ns

V_{CC} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C, Load = 50 pF

Versions(4)		V_{CC} ±5%	28F016SV-080(5)						Unit
		V_{CC} ±10%	28F016SV-080(6)			28F016SV-085(6)			
Sym	Parameter	Notes	Min	Typ	Max	Min	Typ	Max	
t_{AVEL}	Address Setup to CE# Going Low	2, 3	15			15			ns

NOTES:
1. All other specifications for CE#—Controlled Write Operations can be found in section 5.9.
2. Address must be valid during the entire CE# low pulse.
3. CEx# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
4. Device speeds are defined as:
   80/85, 100 ns at V_{CC} = 5.0V equivalent to
   120 ns at V_{CC} = 3.3V
5. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
6. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.



NOTE:
1. CEx# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

Figure 17. Controller Page Buffer Write Timing Waveforms (Loading Data to the Page Buffer)

5.12 Erase and Word/Byte Write Performance[3,5]

V_{CC} = 3.3V ±0.15V, V_{PP} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Typ[1]	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	8	µs	
	Page Buffer Word Write Time	2,6,7	16	µs	
$t_{WHRH}1A$	Byte Write Time	2,7	29	µs	
$t_{WHRH}1B$	Word Write Time	2,7	35	µs	
t_{WHRH}[2]	Block Write Time	2,7	1.9	sec	Byte Write Mode
t_{WHRH}[3]	Block Write Time	2,7	1.2	sec	Word Write Mode
	Block Erase Time	2,7	1.4	sec	
	Full Chip Erase Time	2,7	44.8	sec	
	Erase Suspend Latency Time to Read	4	12	µs	
	Auto Erase Suspend Latency Time to Write		15	µs	

V_{CC} = 3.3V ±0.15V, V_{PP} = 12.0V ±0.6V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Typ[1]	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	2.2	µs	
	Page Buffer Word Write Time	2,6,7	4.4	µs	
t_{WHRH}[1]	Word/Byte Write Time	2,7	9	µs	
t_{WHRH}[2]	Block Write Time	2,7	0.6	sec	Byte Write Mode
t_{WHRH}[3]	Block Write Time	2,7	0.3	sec	Word Write Mode
	Block Erase Time	2	0.8	sec	
	Full Chip Erase Time	2,7	25.6	sec	
	Erase Suspend Latency Time to Read	4	9	µs	
	Auto Erase Suspend Latency Time to Write		12	µs	

5.12 Erase and Word/Byte Write Performance[3,5] (Continued)

V_{CC} = 5.0V, V_{PP} = 5.0V ±0.5V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Typ[1]	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	8	µs	
	Page Buffer Word Write Time	2,6,7	16	µs	
$t_{WHRH}1A$	Byte Write Time	2,7	20	µs	
$t_{WHRH}1B$	Word Write Time	2,7	25	µs	
t_{WHRH}[2]	Block Write Time	2,7	1.4	sec	Byte Write Mode
t_{WHRH}[3]	Block Write Time	2,7	0.85	sec	Word Write Mode
	Block Erase Time	2,7	1.0	sec	
	Full Chip Erase Time	2,7	32.0	sec	
	Erase Suspend Latency Time to Read	4	9	µs	
	Auto Erase Suspend Latency Time to Write		12	µs	

V_{CC} = 5.0V ± 0.5V, V_{PP} = 12.0V ±0.6V, T_{CSE2} = −40°C to +125°C, T_{CSE1} = −55°C to +125°C

Sym	Parameter	Notes	Typ[1]	Units	Test Conditions
	Page Buffer Byte Write Time	2,6,7	2.1	µs	
	Page Buffer Word Write Time	2,6,7	4.1	µs	
t_{WHRH}[1]	Word/Byte Write Time	2,7	6	µs	
t_{WHRH}[2]	Block Write Time	2,7	0.4	sec	Byte Write Mode
t_{WHRH}[3]	Block Write Time	2,7	0.2	sec	Word Write Mode
	Block Erase Time	2	0.6	sec	
	Full Chip Erase Time	2,7	19.2	sec	
	Erase Suspend Latency Time to Read	4	7	µs	
	Auto Erase Suspend Latency Time to Write		10	µs	

NOTES:
1. 25°C, and normal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Specification applies to interrupt latency for single block erase. Suspend latency for erase all unlocked blocks operation extends the maximum latency time to 270 µs.
5. Sampled, but not 100% tested. Guaranteed by design.
6. Assumes using the full Page Buffer to Write to Flash (256 bytes or 128 words).

6.0 MECHANICAL SPECIFICATIONS

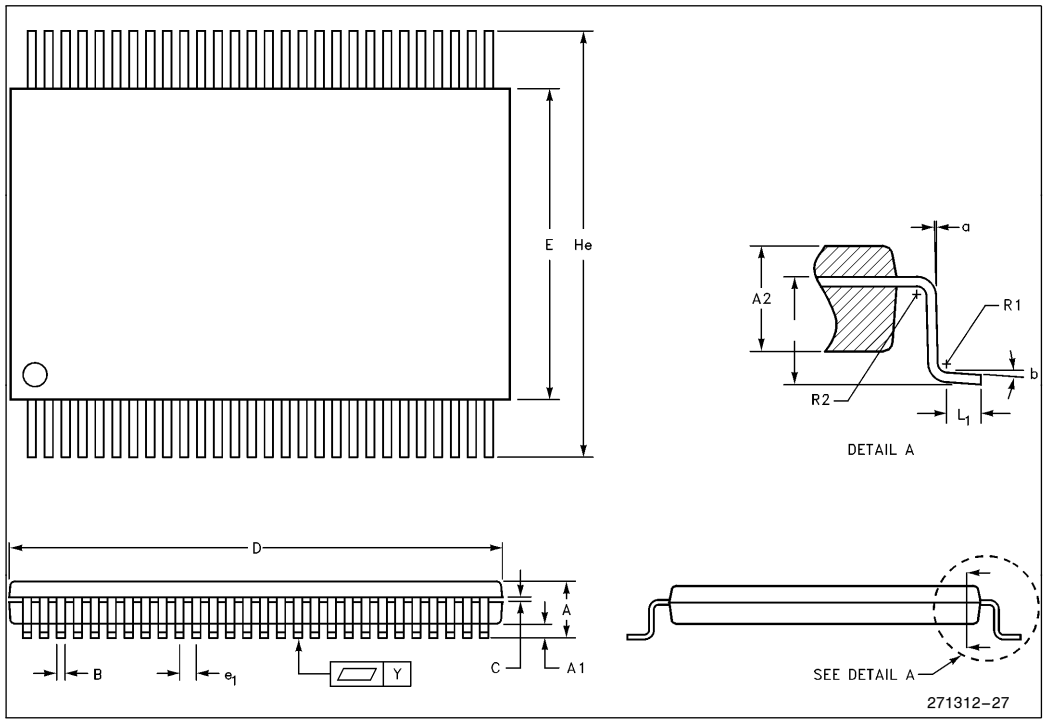


Figure 18. Mechanical Specifications of the VS/MS28F0165V 56-Lead SSOP Package

Family: Shrink Small Out-Line Package				
Symbol	Millimeters			Notes
	Minimum	Nominal	Maximum	
A		1.80	1.90	
A1	0.47	0.52	0.57	
A2	1.18	1.28	1.38	
B	0.25	0.30	0.40	
C	0.13	0.15	0.20	
D	23.40	23.70	24.00	
E	13.10	13.30	13.50	
e_1		0.80		
H_e	15.70	16.00	16.30	
N		56		
L_1	0.45	0.50	0.55	
Y			0.10	
a	2°	3°	4°	
b	3°	4°	5°	
R1	0.45	0.20	0.25	
R2	0.15	0.20	0.25	

DEVICE NOMENCLATURE

V	S	2	8	F	0	1	6	S	V	—	8	5
M	S	2	8	F	0	1	6	S	V	—	8	5

V = SE2
M = SE1

S = SSOP

SV = SmartVoltage Technology

Access Speed

Depending on system design specifcations, the VS/MS28F016SV-85 is capable of supporting

— 85 ns access time with a V_{CC} of 5.0V ±10% and loading of 100 pF

— 100 ns access time with a V_{CC} of 5.0V ±10% and loading of 100 pF

ADDITIONAL INFORMATION

Order Number	Document/Tool
297372	16-Mbit Flash Product Family User's Manual
292163	AP-610 ''Flash Memory In-System Code and Data Update Techinques''
292144	AP-393 ''28F016SV Compatibility with 28F016SA''
292127	AP-378 ''System Optimization Using the Enhanced Features of the 28F016SA''
292126	AP-377 ''16-Mbit Flash Product Family Software Drivers, 28F016SA/ 28F016SV/28F016XS/28F016XD''
292124	AP-387 ''Upgrade Considerations from the 28F008SA to the 28F016SA''
292123	AP-374 ''Flash Memory Write Protection Techniques''
292092	AP-357 ''Power Supply Solutions for Flash Memory''
292165	AB-62 ''Compiling Optimized Code for Embedded Flash RAM Memories''
294016	ER-33 ''ETOX™ Flash Memory Technology—Insight to Intel's Fourth Generation Process Innovation''
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	Flash Cycling Utility
Contact Intel/Distribution Sales Office	28F016SV iBIS Models
Contact Intel/Distribution Sales Office	28F016SV VHDL/Verilog Models
Contact Intel/Distribution Sales Office	28F016SV Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016SV Orcad and ViewLogic Schematic Symbols

DATA SHEET REVISION HISTORY

Number	Description
001	Original Version

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