PRELIMINARY

Pentium® PROCESSORS AT iCOMP® INDEX 735\90, 610\75 MHz WITH VOLTAGE REDUCTION TECHNOLOGY

SmartDie™ Product Specification

- **Compatible with Large Software Base**
  - **MS-DOS*, Windows*, OS/2*, UNIX***
- **32-Bit CPU with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **Two Pipelined Integer Units Are Capable of Two Instructions Per Clock**
  - **Pipelined Floating Point Unit**
- **Separate Code and Data Caches**
  - **8 Kbyte Code, 8 Kbyte Writeback Data**
  - **MESI Cache Protocol**
- **Advanced Design Features**
  - **Branch Prediction**
  - **Virtual Mode Extensions**
- **Low Voltage BiCMOS Silicon Technology**
- **4 Mbyte Pages for Increased TLB Hit Rate**
- **IEEE 1149.1 Boundary Scan**
- **Internal Error Detection Features**
- **SL Enhanced Power Management Features**
  - **System Management Mode**
  - **Clock Control**
- **Voltage Reduction Technology**
  - **2.9V V_{CC} for Core Supply**
  - **3.3V V_{CC} for I/O Buffer Supply**
- **Fractional Bus Operation**
  - **75 MHz Core / 50 MHz Bus**
  - **90 MHz Core / 60 MHz Bus**
- **Intel SmartDie Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C to 105°C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet/Book (Order No. 242557) for additional product information and specifications not found in this document.

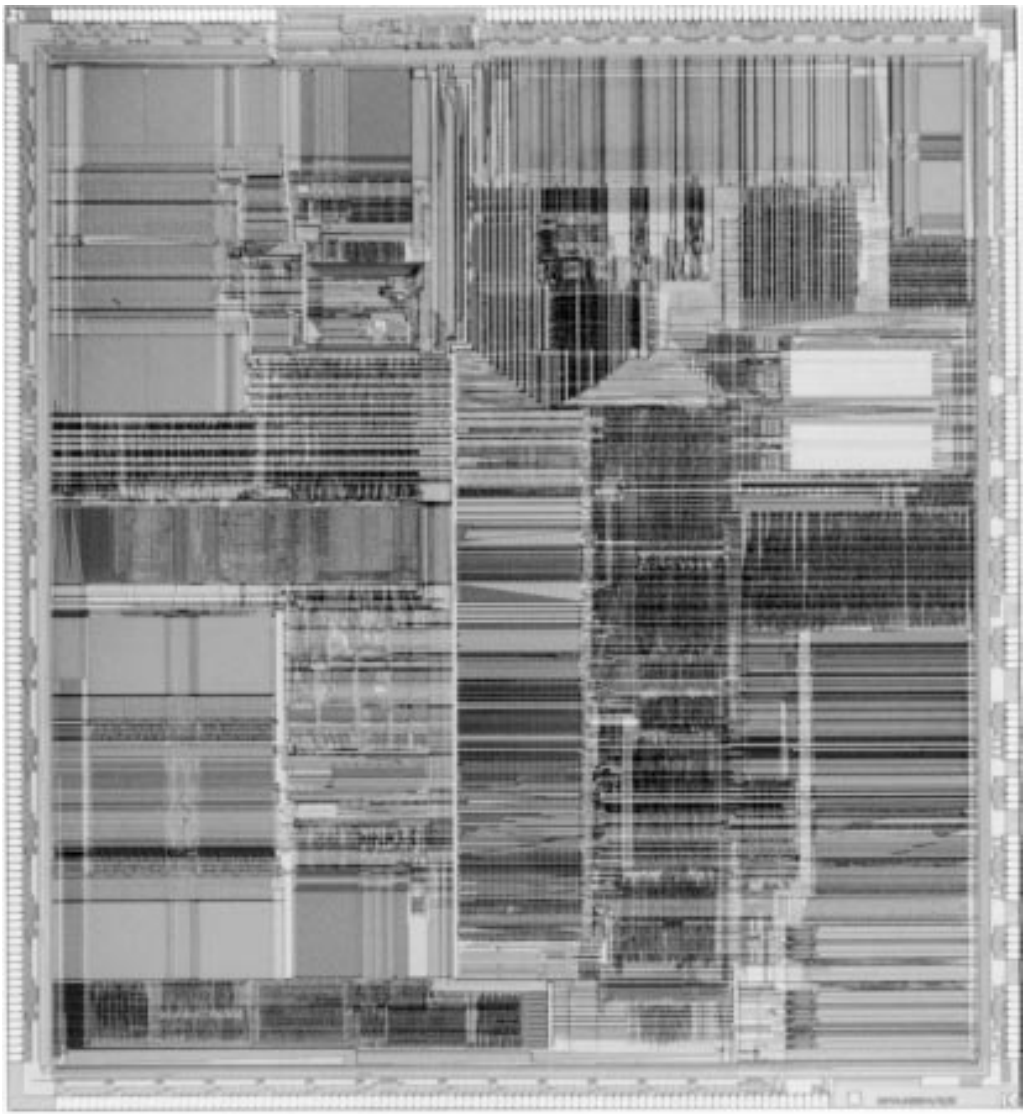
The Pentium processor is fully compatible with the entire installed base of applications for DOS, Windows*, OS/2*, and UNIX*, and all other software that runs on any earlier Intel 8086 family product. The Pentium processor's superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor with voltage reduction has 3.3 million transistors. It is built on Intel's advanced low voltage BiCMOS silicon technology, and has full SL Enhanced power management features, including System Management Mode (SMM) and clock control. The additional SL Enhanced features, 2.9V core operation along with 3.3V I/O buffer operation, and the availability of a SmartDie product version, which are not available in the Pentium processor (510\60, 567\66), make the SmartDie product Pentium processor with voltage reduction technology ideal for enabling mobile Pentium processor designs.

November 1995 **Order Number: 272751-002**

Pentium® PROCESSORS AT iCOMP® INDEX 735/90, 610/ 75 MHz WITH VOLTAGE REDUCTION TECHNOLOGY

SmartDie™ Product Specification

CONTENTS



272751–3

Figure 1. Pentium® Processor Die Photo

1.0 DIE SPECIFICATIONS

The plot and the die photo on the opposite page indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name 80P54LM appears on Pentium processor die.

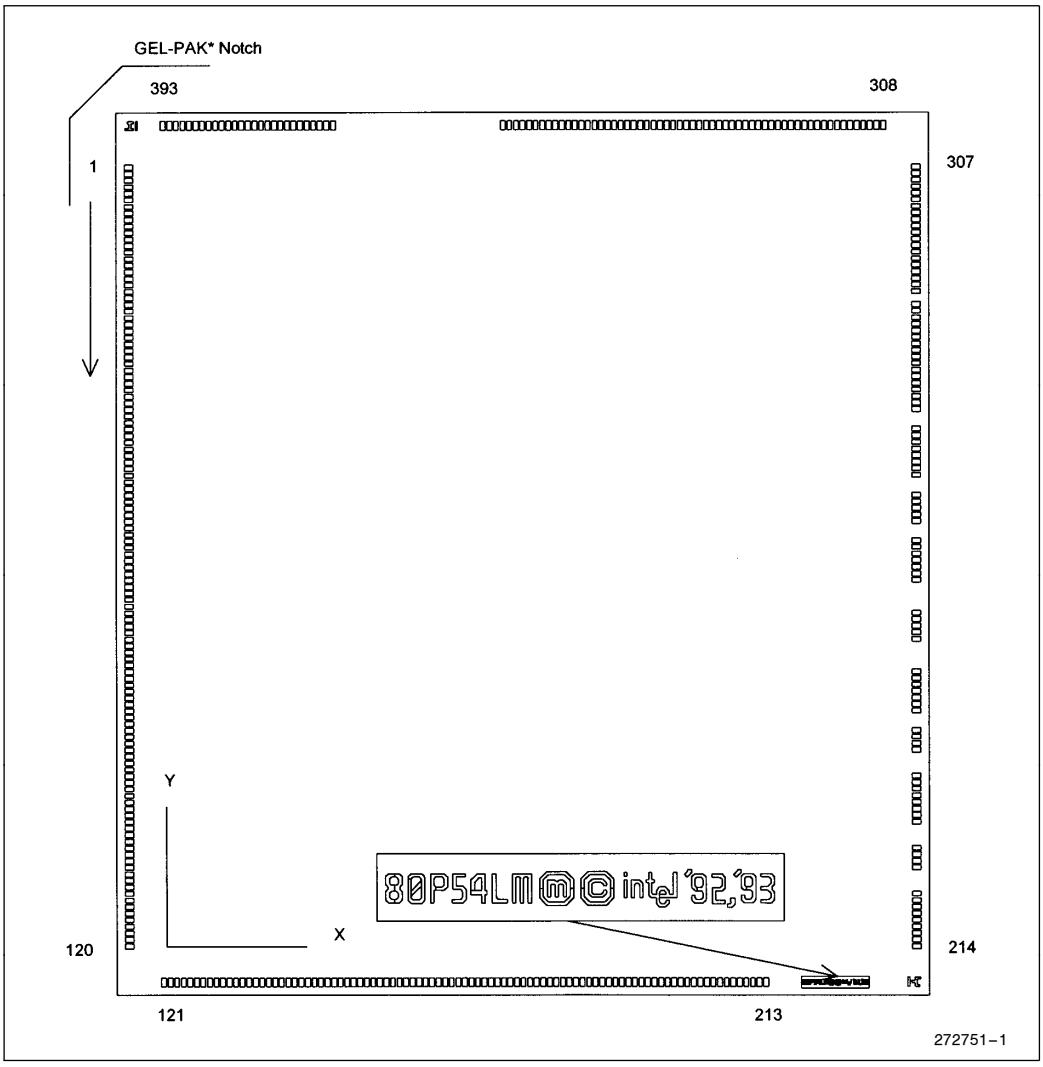


Figure 2. Pentium® Processor Die/Bond Pad Layout

1.1 Pad Description

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 1 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
001	D/C#	−224.8	221.0	−5710	5614
002	PWT	−224.8	217.3	−5710	5519
003	PCD	−224.8	213.6	−5710	5424
004	V_{CC}_3.3	−224.8	209.8	−5710	5329
005	V_{SS}	−224.8	206.1	−5710	5234
006	N.C.	−224.8	202.3	−5710	5139
007	LOCK#	−224.8	198.6	−5710	5044
008	V_{SS}	−224.8	194.9	−5710	4949
009	V_{CC}_2.9	−224.8	191.1	−5710	4854
010	V_{CC}_2.9	−224.8	187.4	−5710	4759
011	V_{SS}	−224.8	183.6	−5710	4664
012	V_{CC}_3.3	−224.8	179.9	−5710	4569
013	V_{SS}	−224.8	176.2	−5710	4474
014	AP	−224.8	172.4	−5710	4379
015	V_{SS}	−224.8	168.7	−5710	4284
016	V_{CC}_2.9	−224.8	164.9	−5710	4189
017	V_{CC}_2.9	−224.8	161.2	−5710	4094
018	V_{SS}	−224.8	157.5	−5710	3999
019	HLDA	−224.8	153.7	−5710	3904
020	BREQ	−224.8	150.0	−5710	3809
021	V_{CC}_3.3	−224.8	146.2	−5710	3714
022	V_{SS}	−224.8	142.5	−5710	3619
023	APCHK#	−224.8	138.8	−5710	3524
024	PCHK#	−224.8	135.0	−5710	3429
025	PRDY	−224.8	131.3	−5710	3334
026	SMIACT#	−224.8	127.5	−5710	3239
027	V_{SS}	−224.8	123.8	−5710	3144
028	V_{CC}_2.9	−224.8	120.1	−5710	3049
029	V_{CC}_2.9	−224.8	116.3	−5710	2954
030	V_{SS}	−224.8	112.6	−5710	2859
031	N.C.	−224.8	108.8	−5710	2764
032	V_{CC}_3.3	−224.8	105.1	−5710	2669
033	V_{SS}	−224.8	101.4	−5710	2574
034	N.C.	−224.8	97.6	−5710	2479
035	N.C.	−224.8	93.9	−5710	2384

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 2 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
036	N.C.	−224.8	90.1	−5710	2289
037	HOLD	−224.8	86.4	−5710	2194
038	WB/WT#	−224.8	82.6	−5710	2099
039	V_{SS}	−224.8	78.9	−5710	2004
040	V_{CC}_2.9	−224.8	75.2	−5710	1909
041	V_{CC}_2.9	−224.8	71.4	−5710	1814
042	V_{SS}	−224.8	67.7	−5710	1719
043	NA#	−224.8	63.9	−5710	1624
044	BOFF#	−224.8	60.2	−5710	1529
045	BRDY#	−224.8	56.5	−5710	1434
046	N.C.	−224.8	52.7	−5710	1339
047	V_{SS}	−224.8	49.0	−5710	1244
048	V_{CC}_2.9	−224.8	45.2	−5710	1149
049	V_{CC}_2.9	−224.8	41.5	−5710	1054
050	V_{SS}	−224.8	37.8	−5710	959
051	KEN#	−224.8	34.0	−5710	864
052	AHOLD	−224.8	30.3	−5710	769
053	INV	−224.8	26.5	−5710	674
054	EWBE#	−224.8	22.8	−5710	579
055	V_{SS}	−224.8	19.1	−5710	484
056	V_{CC}_2.9	−224.8	15.3	−5710	389
057	V_{CC}_2.9	−224.8	11.6	−5710	294
058	V_{SS}	−224.8	7.8	−5710	199
059	V_{CC}_3.3	−224.8	4.1	−5710	104
060	V_{SS}	−224.8	0.4	−5710	9
061	CACHE#	−224.8	−3.4	−5710	−86
062	M/IO#	−224.8	−7.1	−5710	−181
063	V_{CC}_3.3	−224.8	−10.9	−5710	−276
064	V_{SS}	−224.8	−14.6	−5710	−371
065	BP3	−224.8	−18.3	−5710	−466
066	BP2	−224.8	−22.1	−5710	−561
067	PM1/BP1	−224.8	−25.8	−5710	−656
068	PM0/BP0	−224.8	−29.6	−5710	−751
069	FERR#	−224.8	−33.3	−5710	−846
070	V_{SS}	−224.8	−37.0	−5710	−941
071	V_{CC}_2.9	−224.8	−40.8	−5710	−1036
072	V_{CC}_2.9	−224.8	−44.5	−5710	−1131

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 3 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
073	V_{SS}	−224.8	−48.3	−5710	−1226
074	IERR#	−224.8	−52.0	−5710	−1321
075	V_{CC}_3.3	−224.8	−55.7	−5710	−1416
076	V_{SS}	−224.8	−59.5	−5710	−1511
077	DP7	−224.8	−63.2	−5710	−1606
078	D63	−224.8	−67.0	−5710	−1701
079	D62	−224.8	−70.7	−5710	−1796
080	D61	−224.8	−74.4	−5710	−1891
081	V_{SS}	−224.8	−78.2	−5710	−1986
082	V_{CC}_2.9	−224.8	−81.9	−5710	−2081
083	V_{CC}_2.9	−224.8	−85.7	−5710	−2176
084	V_{SS}	−224.8	−89.4	−5710	−2271
085	V_{CC}_3.3	−224.8	−93.1	−5710	−2366
086	V_{SS}	−224.8	−96.9	−5710	−2461
087	D60	−224.8	−100.6	−5710	−2556
088	D59	−224.8	−104.4	−5710	−2651
089	D58	−224.8	−108.1	−5710	−2746
090	D57	−224.8	−111.8	−5710	−2841
091	V_{SS}	−224.8	−115.6	−5710	−2936
092	V_{CC}_2.9	−224.8	−119.3	−5710	−3031
093	V_{CC}_2.9	−224.8	−123.1	−5710	−3126
094	V_{SS}	−224.8	−126.8	−5710	−3221
095	V_{CC}_3.3	−224.8	−130.5	−5710	−3316
096	V_{SS}	−224.8	−134.3	−5710	−3411
097	D56	−224.8	−138.0	−5710	−3506
098	DP6	−224.8	−141.8	−5710	−3601
099	D55	−224.8	−145.5	−5710	−3696
100	D54	−224.8	−149.2	−5710	−3791
101	V_{SS}	−224.8	−153.0	−5710	−3886
102	V_{CC}_2.9	−224.8	−156.7	−5710	−3981
103	V_{CC}_2.9	−224.8	−160.5	−5710	−4076
104	V_{SS}	−224.8	−164.2	−5710	−4171
105	V_{CC}_3.3	−224.8	−167.9	−5710	−4266
106	V_{SS}	−224.8	−171.7	−5710	−4361
107	D53	−224.8	−175.4	−5710	−4456
108	D52	−224.8	−179.2	−5710	−4551
109	D51	−224.8	−182.9	−5710	−4646

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 4 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
110	D50	−224.8	−186.6	−5710	−4741
111	V_{SS}	−224.8	−190.4	−5710	−4836
112	V_{CC}_2.9	−224.8	−194.1	−5710	−4931
113	V_{CC}_2.9	−224.8	−197.9	−5710	−5026
114	V_{SS}	−224.8	−201.6	−5710	−5121
115	V_{CC}_3.3	−224.8	−205.3	−5710	−5216
116	V_{SS}	−224.8	−209.1	−5710	−5311
117	D49	−224.8	−212.8	−5710	−5406
118	D48	−224.8	−216.6	−5710	−5501
119	DP5	−224.8	−220.3	−5710	−5596
120	D47	−224.8	−224.0	−5710	−5691
121	V_{CC}_3.3	−205.3	−244.8	−5214	−6217
122	V_{SS}	−201.5	−244.8	−5119	−6217
123	D46	−197.8	−244.8	−5024	−6217
124	D45	−194.1	−244.8	−4929	−6217
125	D44	−190.3	−244.8	−4834	−6217
126	D43	−186.6	−244.8	−4739	−6217
127	V_{CC}_3.3	−182.8	−244.8	−4644	−6217
128	V_{SS}	−179.1	−244.8	−4549	−6217
129	D42	−175.4	−244.8	−4454	−6217
130	D41	−171.6	−244.8	−4359	−6217
131	D40	−167.9	−244.8	−4264	−6217
132	DP4	−164.1	−244.8	−4169	−6217
133	V_{CC}_3.3	−160.4	−244.8	−4074	−6217
134	V_{SS}	−156.7	−244.8	−3979	−6217
135	D39	−152.9	−244.8	−3884	−6217
136	D38	−149.2	−244.8	−3789	−6217
137	D37	−145.4	−244.8	−3694	−6217
138	D36	−141.7	−244.8	−3599	−6217
139	V_{CC}_3.3	−138.0	−244.8	−3504	−6217
140	V_{SS}	−134.2	−244.8	−3409	−6217
141	D35	−130.5	−244.8	−3314	−6217
142	D34	−126.7	−244.8	−3219	−6217
143	D33	−123.0	−244.8	−3124	−6217
144	D32	−119.3	−244.8	−3029	−6217
145	V_{CC}_3.3	−115.5	−244.8	−2934	−6217
146	V_{SS}	−111.8	−244.8	−2839	−6217

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 5 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
147	DP3	−108.0	−244.8	−2744	−6217
148	D31	−104.3	−244.8	−2649	−6217
149	D30	−100.6	−244.8	−2554	−6217
150	D29	−96.8	−244.8	−2459	−6217
151	V_{CC}_3.3	−93.1	−244.8	−2364	−6217
152	V_{SS}	−89.3	−244.8	−2269	−6217
153	D28	−85.6	−244.8	−2174	−6217
154	D27	−81.9	−244.8	−2079	−6217
155	D26	−78.1	−244.8	−1984	−6217
156	D25	−74.4	−244.8	−1889	−6217
157	V_{CC}_3.3	−70.6	−244.8	−1794	−6217
158	V_{SS}	−66.9	−244.8	−1699	−6217
159	V_{SS}	−63.2	−244.8	−1604	−6217
160	V_{CC}_2.9	−59.4	−244.8	−1509	−6217
161	V_{CC}_2.9	−55.7	−244.8	−1414	−6217
162	V_{SS}	−51.9	−244.8	−1319	−6217
163	D24	−48.2	−244.8	−1224	−6217
164	DP2	−44.5	−244.8	−1129	−6217
165	D23	−40.7	−244.8	−1034	−6217
166	D22	−37.0	−244.8	−939	−6217
167	V_{CC}_3.3	−33.2	−244.8	−844	−6217
168	V_{SS}	−29.5	−244.8	−749	−6217
169	D21	−25.8	−244.8	−654	−6217
170	D20	−22.0	−244.8	−559	−6217
171	D19	−18.3	−244.8	−464	−6217
172	D18	−14.5	−244.8	−369	−6217
173	V_{CC}_3.3	−10.8	−244.8	−274	−6217
174	V_{SS}	−7.1	−244.8	−179	−6217
175	D17	−3.3	−244.8	−84	−6217
176	D16	0.4	−244.8	11	−6217
177	DP1	4.2	−244.8	106	−6217
178	D15	7.9	−244.8	201	−6217
179	V_{CC}_3.3	11.6	−244.8	296	−6217
180	V_{SS}	15.4	−244.8	391	−6217
181	D14	19.1	−244.8	486	−6217
182	D13	22.9	−244.8	581	−6217
183	D12	26.6	−244.8	676	−6217

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 6 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
184	D11	30.3	−244.8	771	−6217
185	V_{CC}_3.3	34.1	−244.8	866	−6217
186	V_{SS}	37.8	−244.8	961	−6217
187	D10	41.6	−244.8	1056	−6217
188	D9	45.3	−244.8	1151	−6217
189	D8	49.0	−244.8	1246	−6217
190	DP0	52.8	−244.8	1341	−6217
191	V_{CC}_3.3	56.5	−244.8	1436	−6217
192	V_{SS}	60.3	−244.8	1531	−6217
193	D7	64.0	−244.8	1626	−6217
194	D6	67.7	−244.8	1721	−6217
195	D5	71.5	−244.8	1816	−6217
196	D4	75.2	−244.8	1911	−6217
197	V_{CC}_3.3	79.0	−244.8	2006	−6217
198	V_{SS}	82.7	−244.8	2101	−6217
199	D3	86.4	−244.8	2196	−6217
200	D2	90.2	−244.8	2291	−6217
201	D1	93.9	−244.8	2386	−6217
202	D0	97.7	−244.8	2481	−6217
203	V_{SS}	101.4	−244.8	2576	−6217
204	V_{CC}_2.9	105.2	−244.8	2671	−6217
205	V_{CC}_2.9	108.9	−244.8	2766	−6217
206	V_{SS}	112.6	−244.8	2861	−6217
207	N.C.	116.4	−244.8	2956	−6217
208	N.C.	120.1	−244.8	3051	−6217
209	N.C.	123.9	−244.8	3146	−6217
210	N.C.	127.6	−244.8	3241	−6217
211	V_{CC}_3.3	131.3	−244.8	3336	−6217
212	V_{SS}	135.1	−244.8	3431	−6217
213	V_{CC}_3.3	138.8	−244.8	3526	−6217
214	TCK	224.8	−224.0	5710	−5691
215	TDO	224.8	−220.3	5710	−5596
216	TDI	224.8	−216.6	5710	−5501
217	TMS	224.8	−212.8	5710	−5406
218	V_{SS}	224.8	−209.1	5710	−5311
219	V_{CC}_2.9	224.8	−205.3	5710	−5216
220	V_{CC}_2.9	224.8	−201.6	5710	−5121

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 7 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (= .001 inch)		Microns	
		X	Y	X	Y
221	V_{SS}	224.8	−197.9	5710	−5026
222	TRST#	224.8	−194.1	5710	−4931
223	V_{SS}	224.8	−179.2	5710	−4551
224	V_{CC}_2.9	224.8	−175.4	5710	−4456
225	V_{CC}_2.9	224.8	−171.7	5710	−4361
226	V_{SS}	224.8	−167.9	5710	−4266
227	N.C.	224.8	−153.0	5710	−3886
228	V_{CC}_3.3	224.8	−149.2	5710	−3791
229	V_{SS}	224.8	−145.5	5710	−3696
230	V_{CC}_2.9	224.8	−141.8	5710	−3601
231	V_{CC}_2.9	224.8	−138.0	5710	−3506
232	V_{SS}	224.8	−134.3	5710	−3411
233	N.C.	224.8	−130.5	5710	−3316
234	N.C.	224.8	−126.8	5710	−3221
235	V_{SS}	224.8	−111.8	5710	−2841
236	V_{CC}_2.9	224.8	−108.1	5710	−2746
237	V_{CC}_2.9	224.8	−104.4	5710	−2651
238	V_{SS}	224.8	−100.6	5710	−2556
239	V_{SS}	224.8	−89.4	5710	−2271
240	V_{SS}	224.8	−85.7	5710	−2176
241	V_{SS}	224.8	−81.9	5710	−2081
242	V_{SS}	224.8	−78.2	5710	−1986
243	V_{CC}_2.9	224.8	−74.4	5710	−1891
244	V_{CC}_2.9	224.8	−70.7	5710	−1796
245	V_{SS}	224.8	−67.0	5710	−1701
246	N.C.	224.8	−48.3	5710	−1226
247	V_{SS}	224.8	−44.5	5710	−1131
248	V_{CC}_2.9	224.8	−40.8	5710	−1036
249	V_{CC}_2.9	224.8	−37.0	5710	−941
250	V_{SS}	224.8	−33.3	5710	−846
251	V_{CC}_3.3	224.8	−14.6	5710	−371
252	V_{SS}	224.8	−10.9	5710	−276
253	V_{CC}_2.9	224.8	−7.1	5710	−181
254	V_{CC}_2.9	224.8	−3.4	5710	−86
255	V_{SS}	224.8	0.4	5710	9
256	N.C.	224.8	4.1	5710	104
257	STPCLK#	224.8	7.8	5710	199

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 8 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
258	N.C.	224.8	19.1	5710	484
259	V_{SS}	224.8	22.8	5710	579
260	V_{CC}_2.9	224.8	26.5	5710	674
261	V_{CC}_2.9	224.8	30.3	5710	769
262	V_{SS}	224.8	34.0	5710	864
263	N.C.	224.8	45.2	5710	1149
264	N.C.	224.8	49.0	5710	1244
265	BF	224.8	52.7	5710	1339
266	V_{SS}	224.8	56.5	5710	1434
267	V_{CC}_2.9	224.8	60.2	5710	1529
268	V_{CC}_2.9	224.8	63.9	5710	1624
269	V_{SS}	224.8	67.7	5710	1719
270	V_{SS}	224.8	71.4	5710	1814
271	N.C.	224.8	82.6	5710	2099
272	V_{SS}	224.8	86.4	5710	2194
273	V_{CC}_2.9	224.8	90.1	5710	2289
274	V_{CC}_2.9	224.8	93.9	5710	2384
275	V_{SS}	224.8	97.6	5710	2479
276	N.C.	224.8	101.4	5710	2574
277	PEN#	224.8	105.1	5710	2669
278	INIT	224.8	108.8	5710	2764
279	IGNNE#	224.8	112.6	5710	2859
280	V_{SS}	224.8	116.3	5710	2954
281	V_{CC}_2.9	224.8	120.1	5710	3049
282	V_{CC}_2.9	224.8	123.8	5710	3144
283	V_{SS}	224.8	127.5	5710	3239
284	SMI#	224.8	131.3	5710	3334
285	INTR	224.8	135.0	5710	3429
286	R/S#	224.8	138.8	5710	3524
287	NMI	224.8	142.5	5710	3619
288	N.C.	224.8	150.0	5710	3809
289	A21	224.8	153.7	5710	3904
290	A22	224.8	157.5	5710	3999
291	A23	224.8	161.2	5710	4094
292	V_{SS}	224.8	164.9	5710	4189
293	V_{CC}_3.3	224.8	168.7	5710	4284
294	A24	224.8	172.4	5710	4379

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 9 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
295	A25	224.8	176.2	5710	4474
296	A26	224.8	179.9	5710	4569
297	A27	224.8	183.6	5710	4664
298	V_{SS}	224.8	187.4	5710	4759
299	V_{CC}_3.3	224.8	191.1	5710	4854
300	A28	224.8	194.9	5710	4949
301	A29	224.8	198.6	5710	5044
302	A30	224.8	202.3	5710	5139
303	A31	224.8	206.1	5710	5234
304	V_{SS}	224.8	209.8	5710	5329
305	V_{CC}_3.3	224.8	213.6	5710	5424
306	V_{CC}_2.9	224.8	217.3	5710	5519
307	V_{SS}	224.8	221.0	5710	5614
308	A3	206.2	244.8	5238	6217
309	V_{SS}	202.5	244.8	5143	6217
310	V_{CC}_3.3	198.8	244.8	5048	6217
311	A4	195.0	244.8	4953	6217
312	A5	191.3	244.8	4858	6217
313	V_{SS}	187.5	244.8	4763	6217
314	V_{CC}_3.3	183.8	244.8	4668	6217
315	A6	180.1	244.8	4573	6217
316	A7	176.3	244.8	4478	6217
317	V_{SS}	172.6	244.8	4383	6217
318	V_{CC}_3.3	168.8	244.8	4288	6217
319	A8	165.1	244.8	4193	6217
320	V_{SS}	161.4	244.8	4098	6217
321	V_{CC}_2.9	157.6	244.8	4003	6217
322	V_{CC}_2.9	153.9	244.8	3908	6217
323	V_{SS}	150.1	244.8	3813	6217
324	A9	146.4	244.8	3718	6217
325	V_{SS}	142.6	244.8	3623	6217
326	V_{CC}_3.3	138.9	244.8	3528	6217
327	A10	135.2	244.8	3433	6217
328	A11	131.4	244.8	3338	6217
329	V_{SS}	127.7	244.8	3243	6217
330	V_{CC}_3.3	123.9	244.8	3148	6217
331	A12	120.2	244.8	3053	6217

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 10 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
332	V_{SS}	116.5	244.8	2958	6217
333	V_{CC}_2.9	112.7	244.8	2863	6217
334	V_{CC}_2.9	109.0	244.8	2768	6217
335	V_{SS}	105.2	244.8	2673	6217
336	A13	101.5	244.8	2578	6217
337	V_{SS}	97.8	244.8	2483	6217
338	V_{CC}_3.3	94.0	244.8	2388	6217
339	A14	90.3	244.8	2293	6217
340	V_{SS}	86.5	244.8	2198	6217
341	V_{CC}_2.9	82.8	244.8	2103	6217
342	V_{CC}_2.9	79.1	244.8	2008	6217
343	V_{SS}	75.3	244.8	1913	6217
344	A15	71.6	244.8	1818	6217
345	V_{SS}	67.8	244.8	1723	6217
346	V_{CC}_3.3	64.1	244.8	1628	6217
347	A16	60.4	244.8	1533	6217
348	A17	56.6	244.8	1438	6217
349	V_{SS}	52.9	244.8	1343	6217
350	V_{CC}_3.3	49.1	244.8	1248	6217
351	A18	45.4	244.8	1153	6217
352	V_{SS}	41.7	244.8	1058	6217
353	V_{CC}_2.9	37.9	244.8	963	6217
354	V_{CC}_2.9	34.2	244.8	868	6217
355	V_{SS}	30.4	244.8	773	6217
356	A19	26.7	244.8	678	6217
357	V_{SS}	23.0	244.8	583	6217
358	V_{CC}_3.3	19.2	244.8	488	6217
359	A20	15.5	244.8	393	6217
360	V_{SS}	11.7	244.8	298	6217
361	V_{CC}_2.9	8.0	244.8	203	6217
362	V_{CC}_2.9	4.3	244.8	108	6217
363	V_{SS}	0.5	244.8	13	6217
364	V_{CC}_2.9	−3.2	244.8	−82	6217
365	V_{SS}	−7.0	244.8	−177	6217
366	RESET	−10.7	244.8	−272	6217
367	N.C.	−108.0	244.8	−2744	6217
368	CLK	−111.8	244.8	−2839	6217

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 11 of 11)

PAD #	SIGNAL	Pad Center			
		Mils (=.001 inch)		Microns	
		X	Y	X	Y
369	SCYC	−115.5	244.8	−2934	6217
370	V_{SS}	−119.3	244.8	−3029	6217
371	V_{CC}_3.3	−123.0	244.8	−3124	6217
372	BE7#	−126.7	244.8	−3219	6217
373	BE6#	−130.5	244.8	−3314	6217
374	BE5#	−134.2	244.8	−3409	6217
375	BE4#	−138.0	244.8	−3504	6217
376	V_{SS}	−141.7	244.8	−3599	6217
377	V_{CC}_3.3	−145.4	244.8	−3694	6217
378	BE3#	−149.2	244.8	−3789	6217
379	BE2#	−152.9	244.8	−3884	6217
380	BE1#	−156.7	244.8	−3979	6217
381	BE0#	−160.4	244.8	−4074	6217
382	A20M#	−164.1	244.8	−4169	6217
383	FLUSH#	−167.9	244.8	−4264	6217
384	BUSCHK#	−171.6	244.8	−4359	6217
385	W/R#	−175.4	244.8	−4454	6217
386	V_{SS}	−179.1	244.8	−4549	6217
387	V_{CC}_3.3	−182.8	244.8	−4644	6217
388	HIT#	−186.6	244.8	−4739	6217
389	HITM#	−190.3	244.8	−4834	6217
390	V_{SS}	−194.1	244.8	−4929	6217
391	V_{CC}_3.3	−197.8	244.8	−5024	6217
392	ADS#	−201.5	244.8	−5119	6217
393	EADS#	−205.3	244.8	−5214	6217

NOTES:
1. N.C. signifies No Connect. These pads must not be connected.
2. The symbol '#' is used at the end of the signal to denote an active low signal.
3. X-Y pad coordinates represent bond pad centers and are relative to the center of the die.
4. Boundary Scan (JTAG) is implemented through the following pads:
   214 (TCK). 215 (TDO), 216 (TDI), 217 (TMS), 222 (TRST).

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs*. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:
GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines Pentium processor physical specifications.

Table 2. Pentium® Processor Physical Specifications

Die Revision:	A-1
Post-Saw Die Dimensions:	Mils: X = 463 ± 0.5, Y = 503 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	Pads may not be evenly pitched. Minimum pitch is: 95 microns (3.7 mils)
Pad Passivation Opening Size:	Mils: 2.8 x 5.0 (single pads) Microns: 71 x 128 (single pads)
Bond Pad Metallization: (outermost layer first)	14,000 Angstroms Al (0.5% Cu), 1000 Angstroms Ti, 365 Angstroms TiN
Pads per Die:	393
Die Backside Material: (outermost layer first)	1600 Angstroms Gold, 150 Angstroms Chrome
Passivation: (outermost layer first)	6.13 microns polyimide, 0.45 microns nitride
Intel Fabrication Process:	BiCMOS (min. feature size 0.6 microns)

3.2 DC Specifications

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature . . . . . 0°C to +70°C
Junction Temperature Under Bias . . . −65°C to +110°C
3V Supply Voltage wrt. V_{SS} . . . . . −0.5V to +4.6V
2.9V Supply Voltage wrt. V_{SS} . . . . . −0.5V to +4.1V
3V Only Buffer DC Input Voltage . −0.5V to V_{CC3} +0.5V; not to exceed 4.6V(1)
5V Safe Buffer DC Input Voltage . . . . −0.5V to +6.5V(2)

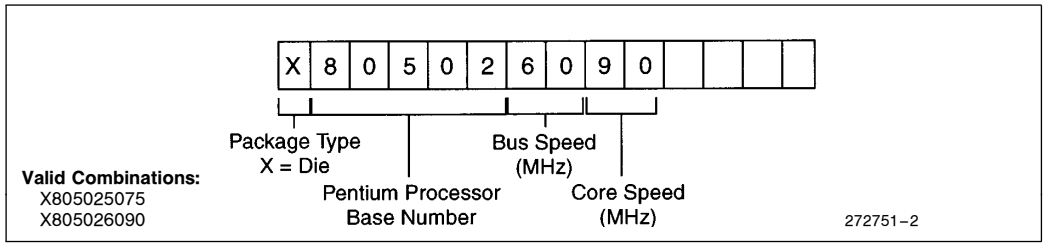
WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS*

V_{CC3} (I/O Supply Voltage) . . . . . 3.3V ± 165 mV
V_{CC2} (Core Supply Voltage) . . . . . 2.9V ± 165 mV
T_J (Junction Temperature Under Bias) . . 0°C to 105°C(3)
Core Operating Frequency . . . . . 75, 90 MHz (50, 60 MHz Bus)
Substrate Bias . . . . . Drive V_{SS}

NOTES:
1. Applies to all Pentium processors with Voltage Reduction Technology inputs except CLK.
2. Applies to CLK.
3. Average die surface temperature.

4.0 DEVICE NOMENCLATURE



Valid Combinations:
X805025075
X805026090

5.0 REFERENCE INFORMATION

Document Title	Order #
Pentium® Processors at iComp® Index 735/90, 610/75 MHz with Voltage Reduction Technology	242557
Pentium® Processors and Related Products	241732
AP-479 Pentium® Processor Clock Design (Application Note)	241574
AP-480 Pentium® Processor Thermal Design Guidelines (Application Note)	241575

6.0 REVISION HISTORY

Revision	Date	Description
−001	7/95	Initial Release
−002	10/95	Pads 228, 239, 240, 241—Signal names modified.