PRELIMINARY

28F008SAC 8-MBIT (1-MBIT X 8) FlashFile™ MEMORY DEVICE

SmartDie™ Product Specification

- **Same Function as 28F008SA-120**
  - **— New Reduced Die Size**
- **High-Density Symmetrically-Blocked Architecture**
  - **— Sixteen 64-Kbyte Blocks**
- **Extended Cycling Capability**
  - **— 100,000 Block Erase Cycles**
  - **— 1.6 Million Block Erase Cycles per Device**
- **Automated Byte Write and Block Erase**
  - **— Command User Interface**
  - **— Status Register**
- **System Performance Enhancements**
  - **— RY/BY# Status Output**
  - **— Erase Suspend Capability**
- **Deep Power-Down Mode**
  - **— 0.20 µA I_{CC} Typical**
- **Very High-Performance Read**
  - **— 120 ns Maximum Access Time**
- **SRAM-Compatible Write Interface**
- **Hardware Data Protection Feature**
  - **— Erase/Write Lockout during Power Transitions**
- **ETOX™ IV Nonvolatile Flash Technology**
  - **— 12 V Byte Write/Block Erase**
- **Intel SmartDie™ Product**
  - **— Full AC/DC Testing at Die Level**
  - **— 0°C to +80°C (Junction) Temperature Range**
  - **— Available only in 120 ns Access Time**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in "DEVICE NOMENCLATURE" on page 7. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet on a specific product. Please refer to the standard package datsheet (order number 290429) for product information and specifications not found in this document.

March 1996 **Order Number: 272817-001**

28F008SAC 8-Mbit (1-Mbit x 8) FlashFile™ Memory Device

SmartDie™ Product Specification

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1.0 DIE SPECIFICATIONS

The die photo below and the plot on page 2 indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name “28F008SA” appears on the die. Table 1 describes the bond pad number and pad center data for each signal.

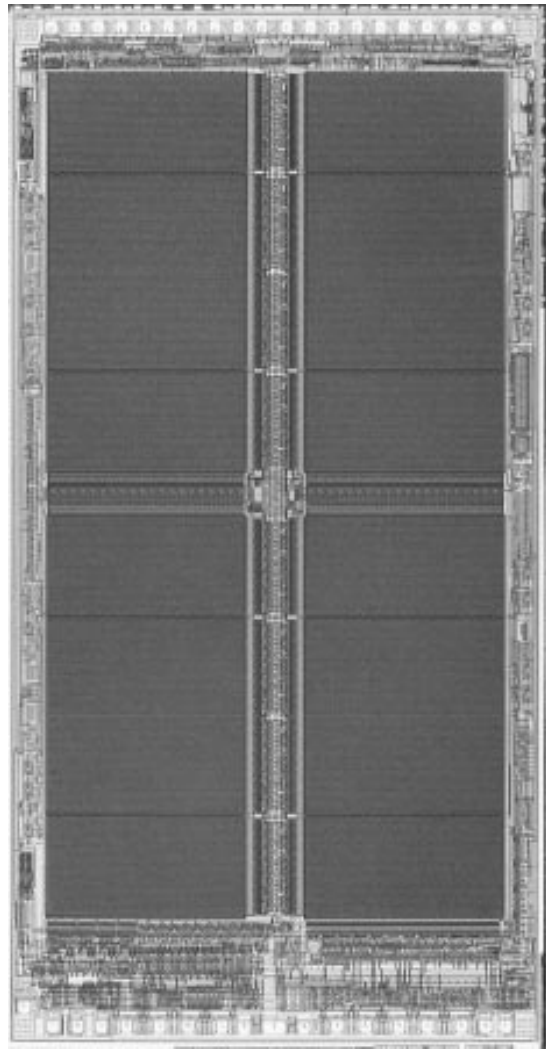

Figure 1. 28F008SAC 8-Mbit FlashFile™ Memory Die Photo

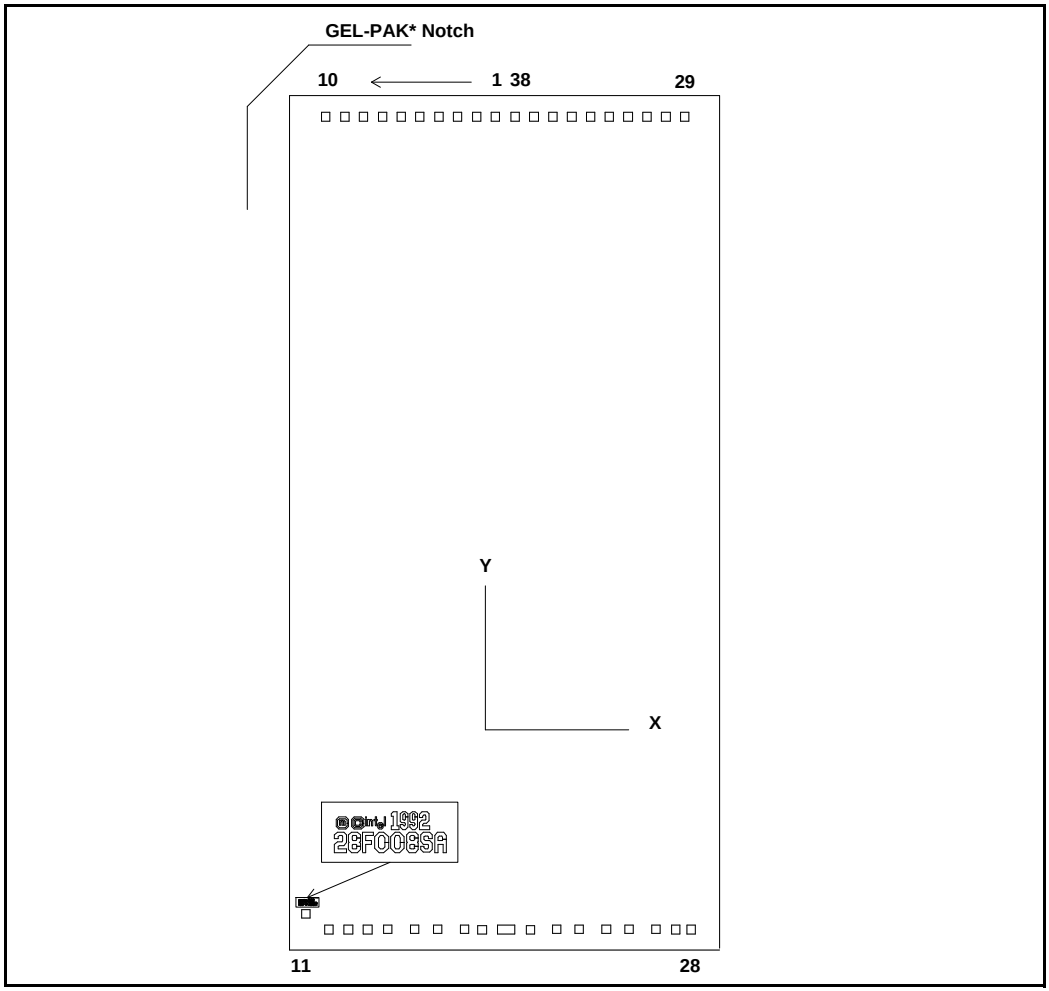

Figure 2. 28F008SAC 8-Mbit FlashFile™ Memory Die/Bond Pad Layout

Table 1. 28F008SAC 8-Mbit FlashFile™ Memory Bond Pad Center Data (Sheet 1 of 2)

PAD#	SIGNAL[2]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
001	V_{PP}	-5.2	198.1	-133	5031
002	PWD#	-14.5	198.1	-367	5031
003	A11	-23.7	198.1	-601	5031
004	A10	-32.9	198.1	-835	5031
005	A9	-42.1	198.1	-1069	5031
006	A8	-51.3	198.1	-1302	5031
007	A7	-60.5	198.1	-1536	5031
008	A6	-69.7	198.1	-1770	5031
009	A5	-78.9	198.1	-2004	5031
010	A4	-88.1	198.1	-2238	5031
011	A3	-97.8	-189.6	-2483	-4817
012	A2	-86.5	-197.1	-2198	-5006
013	A1	-77.0	-197.1	-1956	-5006
014	A0	-67.7	-197.1	-1719	-5006
015	DQ0	-57.8	-196.9	-1469	-5002
016	DQ1	-44.7	-196.9	-1135	-5002
017	DQ2	-33.6	-196.9	-853	-5002
018	DQ3	-20.4	-196.9	-518	-5002
019	V_{SS}	-11.7	-197.3	-298	-5011
020[3]	V_{SS}	0.1	-197.2	2	-5008
021	V_{CC}	11.9	-197.3	302	-5011
022	DQ4	24.7	-196.9	627	-5002
023	DQ5	35.8	-196.9	910	-5002
024	DQ6	49.0	-196.9	1244	-5002
025	DQ7	60.1	-196.9	1526	-5002
026	RY/BY#	73.3	-196.9	1861	-5002
027	OE#	82.9	-197.1	2105	-5006
028	WE#	90.4	-197.1	2297	-5006
029	A19	87.2	198.1	2215	5031
030	A18	78.0	198.1	1982	5031
031	A17	68.8	198.1	1748	5031
032	A16	59.6	198.1	1514	5031

Table 1. 28F008SAC 8-Mbit FlashFile™ Memory Bond Pad Center Data (Sheet 2 of 2)

PAD#	SIGNAL[2]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
033	A15	50.4	198.1	1280	5031
034	A14	41.2	198.1	1046	5031
035	A13	32.0	198.1	813	5031
036	A12	22.8	198.1	579	5031
037	CE#	13.6	198.1	345	5031
038	V_{CC}	4.4	198.1	111	5031

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. The symbol "#" is used to denote active low signals.
3. Double wide bond pad.

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:

GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Handling Requirements

There are two key areas of concern for the 28F008SAC:

- Avoid exposing Flash devices to ultraviolet light. Exposure to UV light erases data in the memory array and erases the device-specific control information stored on-chip.
- Do not expose the 28F008SAC to temperatures above 350°C for more than 10 minutes. Exposure above this time/temperature envelope may cause damage to the device reference cells.

3.2 Physical Specifications

Substrate Bias Condition: Isolate. Chip self-biases (to V_{SS}). Alternative is to drive V_{SS}. Table 2 defines 28F008SAC 8-Mbit (1-Mbit x 8) FlashFile™ Memory Device physical specifications.

Table 2. 28F008SAC 8-Mbit FlashFile™ Memory Physical Specifications

Die Revision:	G-0
Post-Saw Die Dimensions:	Mils: X = 211 ± 0.5, Y = 413 ± 0.5 See Figure 2 for X, Y orientation.
Die Thickness:	17 ± 1.0 mils
Minimum Pad Pitch:	Pads may not be evenly pitched. Minimum pitch is: 193 microns (7.6 mils)
Pad Passivation Opening Size:	Mils: 4.1 x 4.1 (Single pads) Microns: 105 x 105 (Single pads) Mils: 4.1 x 8.3 (Double pads) Microns: 105 x 210 (Double pads)
Bond Pad Metallization: (outermost layer first)	9000 Angstroms Aluminum (0.5% Copper), 1000 Angstroms Titanium, 4000 Angstroms Aluminum (0.5% Copper), 450 Angstroms Tin, 300 Angstroms Titanium
Pads per Die:	38
Die Backside Material: (outermost layer first)	Polished bare silicon
Passivation: (outermost layer first)	2.3 Microns B-Pyrox, 1.5 Microns Oxynitride
Intel Fabrication Process:	ETOX™ IV (min. feature size 0.6 microns)
Substrate Bias Condition:	Float (Self-biasing to V_{SS}). Alternative is to drive V_{SS}.

3.3 DC Specifications

ABSOLUTE MAXIMUM RATINGS†

GEL-PAK Storage Temperature ..... 0°C to +70°C
Junction Temperature Under Bias ..... See Note
Voltage on Any Pin
(Except V_{CC} and V_{PP}) wrt V_{SS} ..... See Note
Supply Voltage V_{CC} wrt V_{SS} ..... See Note
Program Voltage V_{PP} wrt V_{SS}
during Block Erase/Byte Write ..... See Note

Note: For absolute maximum rating values, refer to the *28F008SA 8-Mbit (1-Mbit x 8) FlashFile™ Memory* datasheet, Order No. 290429.

OPERATING CONDITIONS†

T_J (Junction Temperature Under Bias) ..... 0° to 80°C
V_{CC} Supply Voltage (10%) ..... 4.50 to 5.50 V

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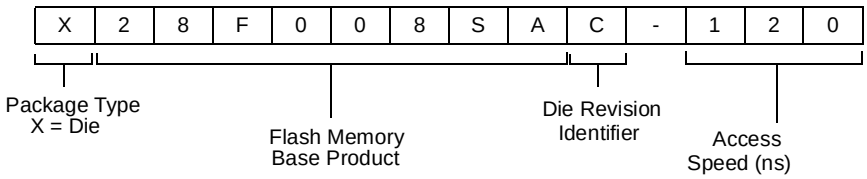
†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



VALID COMBINATION:
X28F008SAC-120

5.0 REFERENCE INFORMATION

Document Title	Order #
28F008SA 8-Mbit (1-Mbit x 8) FlashFile™ Memory datasheet	290429
AP-359, 28F008SA Hardware Interfacing application note	292094
AP-360, 28F008SA Software Drivers application note	292095
AP-364, 28F008SA Automation and Algorithms application note	292099
ER-27, The Intel 28F008SA Flash Memory engineering report	294011

6.0 REVISION HISTORY

Revision	Date	Description
001	3/96	Initial Release