PRELIMINARY

28F008SA 8-MBIT (1-MBIT x 8) FLASH MEMORY

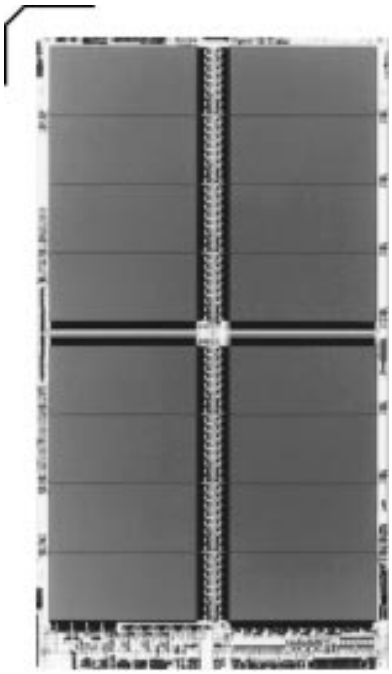
SmartDie Product Specification

- **High-Density Symmetrically Blocked Architecture**
  - **Sixteen 64-Kbyte Blocks**
- **Extended Cycling Capability**
  - **100K Block Erase Cycles**
  - **1.6M Block Erase Cycles per Chip**
- **Automated Byte Write and Block Erase**
  - **Command User Interface**
  - **Status Register**
- **System Performance Enhancements**
  - **RY/BY# Status Output**
  - **Erase Suspend Capability**
- **Deep Powerdown Mode**
  - **0.2 μA I_{CC} Typical**
- **High-Performance Read**
  - **120 ns Maximum Access Time**
- **SRAM-Compatible Write Interface**
- **Hardware Data Protection Feature**
  - **Erase/Write Lockout During Power Transitions**
- **ETOX™ III Nonvolatile Flash Technology**
  - **12V Byte Write/Block Erase**
- **Independent Software Vendor Support**
  - **Flash Translation Layer (FTL)**
- **Intel SmartDie Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C to +80°C (Junction) Temperature Range**
  - **Available in 120 ns Access Time Only**

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice.

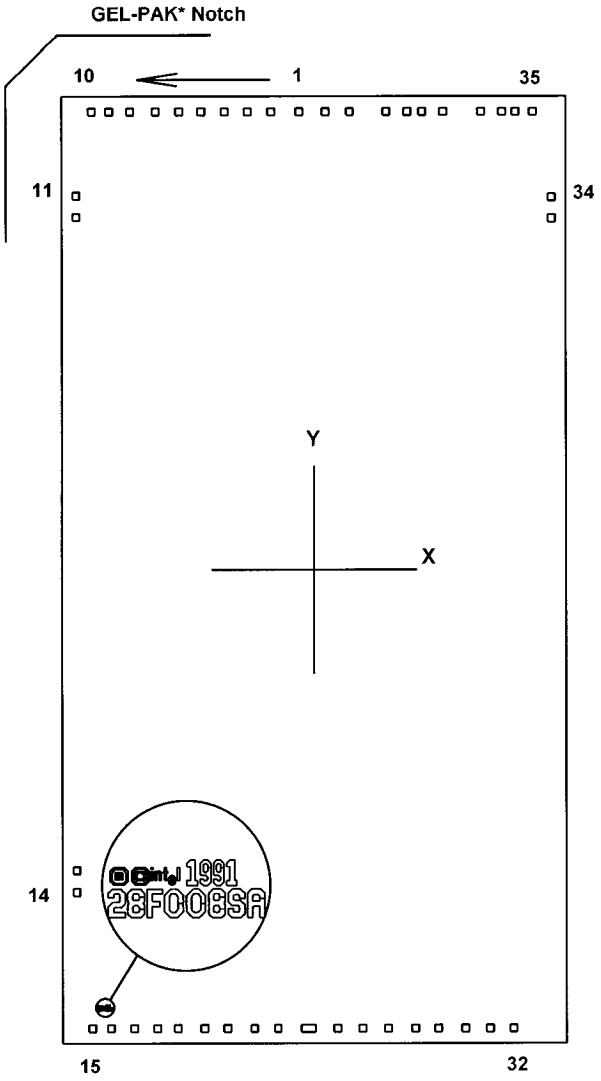
REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet/Book (Order No. 290429) for additional product information and specifications not found in this document.

December 1995 **Order Number: 271296-002**



28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Die Photo

1.0 DIE SPECIFICATIONS



NOTE:
This drawing and the photo on the opposite page indicate the actual orientation of the die in the GEL-PAK* (shipping container). The 45 ° notches shown on the plot and the photo indicate the location of the GEL-PAK notch.

Figure 1. 28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Die/Bond Pad Layout

1.1 Pad Description

Table 1. 28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Bond Pad Center Data

Pad	Signal	Pad Center			
		(Inches)		(Microns)	
		X	Y	X	Y
001	V_{PP}	−0.0084	0.2652	−212	6736
002	PWD#	−0.0248	0.2652	−630	6736
003	A11	−0.0387	0.2652	−982	6736
004	A10	−0.0523	0.2652	−1328	6736
005	A9	−0.0660	0.2652	−1676	6736
006	A8	−0.0789	0.2652	−2004	6736
007	A7	−0.0927	0.2652	−2354	6736
008	A6	−0.1075	0.2652	−2731	6736
009	A5	−0.1199	0.2652	−3045	6736
010	A4	−0.1301	0.2652	−3306	6736
011	N.C.	−0.1392	0.2165	−3535	5498
012	N.C.	−0.1392	0.2041	−3535	5184
013	N.C.	−0.1392	−0.1740	−3535	−4420
014	N.C.	−0.1392	−0.1864	−3535	−4734
015	A3	−0.1301	−0.2652	−3305	−6736
016	A2	−0.1191	−0.2652	−3025	−6736
017	A1	−0.1055	−0.2652	−2681	−6736
018	A0	−0.0922	−0.2652	−2341	−6736
019	DQ0	−0.0801	−0.2652	−2036	−6736
020	DQ1	−0.0644	−0.2652	−1637	−6736
021	DQ2	−0.0510	−0.2652	−1294	−6736
022	DQ3	−0.0353	−0.2652	−896	−6736
023	V_{SS}	−0.0215	−0.2652	−545	−6736
024	V_{SS}(4)	−0.0037	−0.2652	−95	−6736
025	V_{CC}	0.0135	−0.2652	342	−6736
026	DQ4	0.0280	−0.2652	712	−6736
027	DQ5	0.0431	−0.2652	1094	−6736
028	DQ6	0.0590	−0.2652	1499	−6736
029	DQ7	0.0725	−0.2652	1841	−6736
030	RY/BY#	0.0883	−0.2652	2242	−6736
031	OE#	0.1028	−0.2652	2611	−6736
032	WE#	0.1164	−0.2652	2957	−6736

Table 1. 28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Inches)		(Microns)	
		X	Y	X	Y
033	N.C.	0.1392	0.2032	3535	5162
034	N.C.	0.1392	0.2156	3535	5476
035	A19	0.1282	0.2652	3258	6736
036	A18	0.1180	0.2652	2996	6736
037	A17	0.1103	0.2652	2801	6736
038	A16	0.0979	0.2652	2488	6736
039	A15	0.0758	0.2652	1925	6736
040	A14	0.0634	0.2652	1611	6736
041	A13	0.0547	0.2652	1389	6736
042	A12	0.0423	0.2652	1076	6736
043	CE#	0.0210	0.2652	533	6736
044	V_{CC}	0.0068	0.2652	173	6736

Notes:
1. **N.C. signifies no connect. These pads must not be connected.**
2. **The symbol "#" is used at the end of the signal name to denote an active low signal.**
3. **X-Y pad coordinates represent bond pad centers and are relative to center of die.**
4. **Double wide bond pad.**

2.0 INTEL DIE PRODUCTS PROCESSING

TEST PROCEDURE

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

WAFER PROBE

Wafer probing is performed on every wafer produced in an Intel Fab. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

WAFER SAW

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts completely through the wafer.

DIE INSPECTION

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

PACKING PROCEDURE

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel Die Products
- Intel Part Number
- Spec
- Customer Part Number (if applicable)
- Fab Lot Number
- Quantity
- Assembly Lot Traveler Number
- Seal Date
- ROM Code (if applicable)

NOTE:
GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

INSPECTION STEPS

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

STORAGE REQUIREMENTS

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent bond pad corrosion.

ESD

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Handling Requirements

There are two key areas of concern for the 28F008SA. The first is our recommendation to avoid exposing Flash devices to ultraviolet light. Erasing the device under a UV light erases not only the bits in the array but also the device-specific control information stored in the chips. The second area of concern is in the exposure of the 28F008SA to temperatures above 350°C for more than 10 minutes. Exposure above this time/temperature envelope may cause damage to the device reference cells.

3.2 28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Physical Specifications

Substrate Bias Condition: Isolate. Chip self-biases (to V_{SS}). Alternative is to drive V_{SS}.

Post-saw die dimensions:
Mils: X = 294 ±0.5, Y = 547 ±0.5
See associated Die/Bond Pad Layout for X,Y orientation.

Die Backside: Polished bare silicon.

Pad Passivation Opening Size:
Mils: 4.1 x 4.1
Microns: 105 x 105

Die Thickness: 17 ± 1 mils

Pad Pitch:
Pads are not all evenly pitched. Minimum pitch is 7.7 mils between pads 36 and 37.

Bond Pad Metalization (outermost layer listed first):
0.9 microns Aluminum (0.5% Copper)
0.1 micron Titanium

Die Revision: A

Pads per Die: 44

Intel Fabrication Process: ETOX™ III (minimum feature size: 0.8 micron)

Passivation (outermost layer listed first):
2.3 microns B-Pyrox
1.1 microns Oxynitride

3.3 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature . . . . . 0°C to +70°C

For Junction Temperature Under Bias, Supply Voltage with Respect to V_{SS} and Voltage on Other Pads reference the 28F008SA 8-Mbit (1-Mbit x 8) Flash Memory Data Sheet, Order No. 290429.

OPERATING CONDITIONS*

V_{CC} (Digital Supply Voltage) . . . . . 4.5V to 5.5V

T_J (Junction Temperature Under Bias) . . . . . 0°C to +80°C

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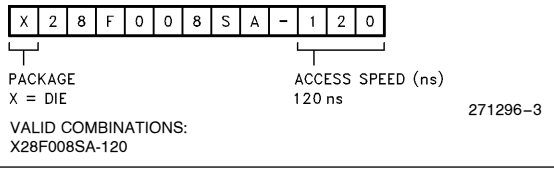
***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



5.0 REFERENCE INFORMATION

Title	Order No.
28F008SA 8-Mbit FlashFile Memory Data Sheet	290429
AP-359, 28F008SA Hardware Interfacing	292094
AP-360, 25F008SA Software Drivers	292095
AP-364, 28F008SA Automation and Algorithms	292099
ER-27, The Intel 28F008SA Flash Memory	294011
ER-28, ETOX™ III Flash Memory Technology	290412

6.0 REVISION HISTORY

Rev	Date	Description
001	3/94	Original version
002	6/94	Replace Figure 1 to add GEL-PAK orientation information. General re-write of Section 2.0.

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