PRELIMINARY

28F010 1024K (128K x 8) FLASH MEMORY

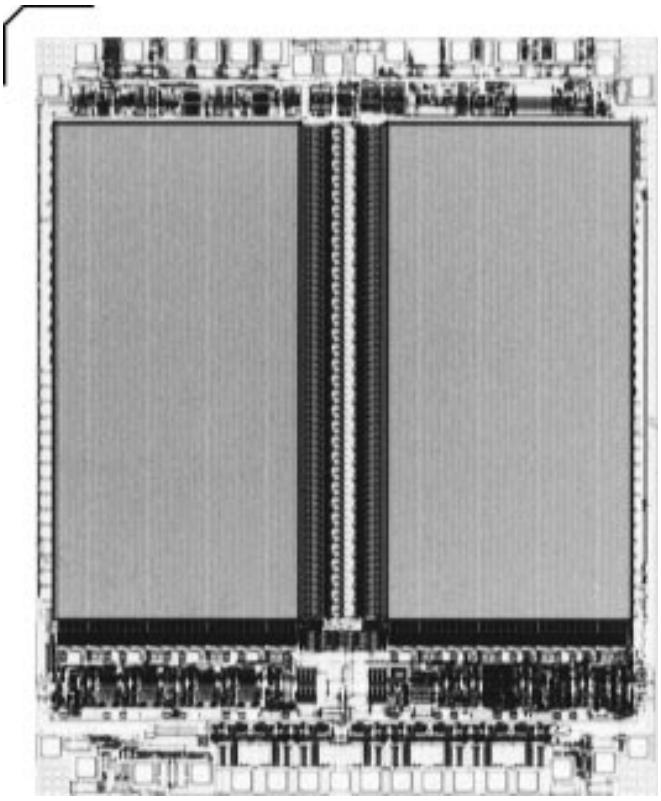
SmartDie Product Specification

- **Flash Electrical Chip Erase**
  - **1 Second Typical Chip Erase**
- **Quick-Pulse Programming Algorithm**
  - **10 μs Typical Byte Program**
  - **2 Second Chip Program**
- **100K Erase/Program Cycles Typical**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **90 ns Access Time**
- **CMOS Low Power Consumption**
  - **10 mA Typical Active Current**
  - **50 μA Typical Standby Current**
  - **0 Watts Data Retention Power**
- **Integrated Program/Erase Stop Timer**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™ III Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **Intel SmartDie Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C to +80°C (Junction) Temperature Range**
  - **Available in 90 ns Access Time Only**
- **Reference the 28F010 1024K (128K x 8) CMOS Flash Memory Data Sheet, #290207, for Device Parameters and Architectural Features**

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet/Book (Order No. 290207) for additional product information and specifications not found in this document.

November 1995 **Order Number: 271294-002**



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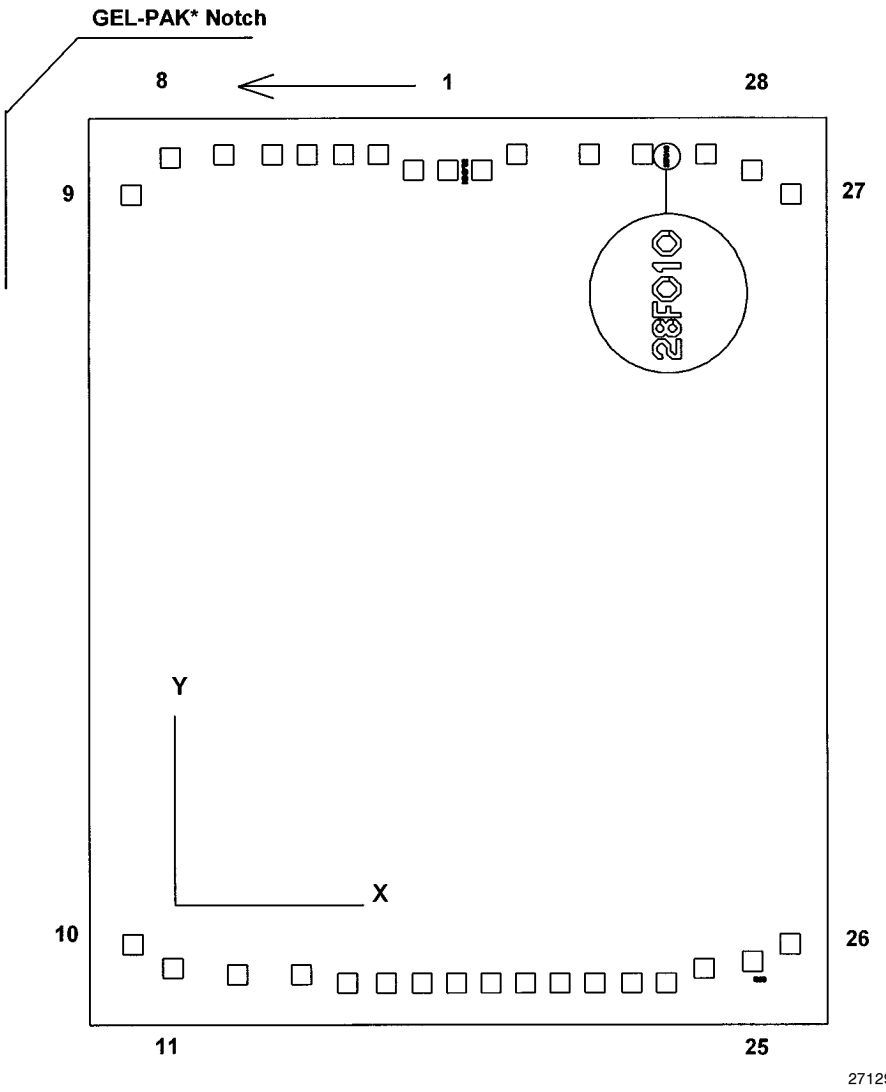
28F010 1024K (128K x 8) Flash Memory Die Photo

1.0 DIE SPECIFICATIONS



NOTE:
This drawing and the photo on the opposite page indicate the actual orientation of the die in the GEL-PAK* (shipping container). The 45° notches shown on the plot and the photo indicate the location of the GEL-PAK notch.

Figure 1. 28F010 1024K (128K x 8) Flash Memory Die/Bond Pad Layout

1.1 Pad Description

Table 1. 28F010 1024K (128K x 8) Flash Memory Bond Pad Center Data

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
001	V_{CC}	−2.1	84.2	−53	2138
002	V_{PP}	−9.4	84.2	−238	2138
003	A16	−16.7	87.4	−425	2219
004	A15	−24.2	87.4	−615	2219
005	A12	−31.9	87.4	−810	2219
006	A7	−39.3	87.4	−998	2219
007	A6	−49.5	87.4	−1257	2219
008	A5	−60.8	86.8	−1545	2204
009	A4	−69.1	79.0	−1756	2007
010	A3	−68.9	−78.1	−1750	−1983
011	A2	−60.5	−83.0	−1536	−2109
012	A1	−46.9	−84.4	−1190	−2144
013	A0	−33.3	−84.4	−845	−2144
014	DQ0	−23.6	−86.2	−601	−2190
015	DQ1	−15.3	−86.2	−389	−2190
016	DQ2	−7.8	−86.2	−198	−2190
017	V_{SS}	−0.4	−86.2	−11	−2190
018	V_{SS}	6.8	−86.2	174	−2190
019	DQ3	14.1	−86.2	359	−2190
020	DQ4	21.5	−86.2	545	−2190
021	DQ5	28.9	−86.2	735	−2190
022	DQ6	36.7	−86.2	932	−2190
023	DQ7	44.0	−86.2	1117	−2190
024	CE#	52.1	−83.2	1322	−2114
025	A10	62.2	−81.7	1579	−2076
026	OE#	70.1	−78.1	1781	−1983
027	A11	70.5	79.0	1790	2007
028	A9	62.2	84.0	1580	2133
029	A8	52.6	87.4	1337	2219
030	A13	39.3	87.4	998	2219

Table 1. 28F010 1024K (128K x 8) Flash Memory Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
031	A14	28.0	87.4	710	2219
032	WE#	12.5	87.4	318	2219
033	V_{CC}	5.2	84.2	132	2138

Notes:

1. **The symbol "#" is used at the end of the signal name to denote an active low signal.**
2. **X-Y pad coordinates represent bond pad centers and are relative to center of die.**

2.0 INTEL DIE PRODUCTS PROCESSING

TEST PROCEDURE

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

WAFER PROBE

Wafer probing is performed on every wafer produced in an Intel Fab. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

WAFER SAW

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts completely through the wafer.

DIE INSPECTION

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

PACKING PROCEDURE

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel Die Products
- Intel Part Number
- Spec
- Customer Part Number (if applicable)
- Fab Lot Number
- Quantity
- Assembly Lot Traveler Number
- Seal Date
- ROM Code (if applicable)

NOTE:
GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

INSPECTION STEPS

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

STORAGE REQUIREMENTS

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent bond pad corrosion.

ESD

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 28F010 1024K (128K x 8) Flash Memory Handling Requirements

There are two key areas of concern for the 28F010. The first is our recommendation to avoid exposing Flash devices to ultraviolet light. Erasing the device under a UV light erases not only the bits in the array but also the device-specific control information stored in the chips. The second area of concern is in the exposure of the 28F010 to temperatures above 475°C for more than 10 minutes. Exposure above this time/temperature envelope may cause damage to the device reference cells.

3.2 28F010 1024K (128K x 8) Flash Memory Physical Specifications

Substrate Bias Condition: Float (self-biasing to V_{SS}). Alternative is to drive V_{SS}.

Post-saw die dimensions:
Mils: X = 155 ±0.5, Y = 189 ±0.5
See associated Die/Bond Pad Layout for X, Y orientation.

Die Backside: Polished bare silicon.

Pad Passivation Opening Size:
Mils: 4.1 x 4.1
Microns: 105.0 x 105.0

Die Thickness: 17 ± 1 mils

Pad Pitch:
Pads are not all evenly pitched. Minimum pitch is 185 microns (7.3 mils).

Bond Pad Metalization (outermost layer listed first):
0.9 micron Aluminum (0.5% Copper)
0.1 micron Titanium

Die Revision: A

Pads per Die: 33

Intel Fabrication Process: ETOX™ III (minimum feature size: 0.8 micron).

Passivation: (from top surface)
2.3 microns B-Pyrox
1.1 microns Oxynitride

3.3 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature . . . . . 0°C to +70°C

For Junction Temperature Under Bias, Supply Voltage with Respect to V_{SS} and Voltage on Other Pads reference the 28F010 1024K (128K x 8) CMOS Flash Memory Data Sheet, #290207.

OPERATING CONDITIONS*

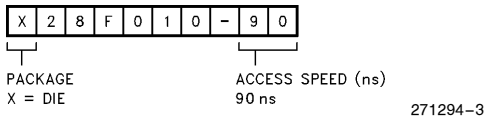
V_{CC} (Digital Supply Voltage) . . . . . 4.5V to 5.5V

T_J (Junction Temperature Under Bias) . . . . . 0°C to 80°C

NOTICE: This document contains prelminary information on new products in production. It is valid for the new devices indicated in the revision history. This specification is subject to change without notice.

****WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



5.0 ADDITIONAL INFORMATION

Title	Order No.
28F010 1-Mbit Flash Memory	290207
ER-20, ETOX™ II Flash Memory Technology	294005
ER-24, Intel Flash Memory	294008
RR-60, ETOX™ II Flash Memory Reliability Data Summary	293002
AP-316, Using Flash Memory for In-System Reprogrammable Nonvolatile Storage	292046
AP-325, Guide to Flash Memory Reprogramming	292059

6.0 REVISION HISTORY

Rev	Date	Description
001	3/94	Original Version.
002	6/94	Replace Figure 1 to add GEL-PAK orientation information. General re-write of Section 2.0.

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