WRITE-BACK ENHANCED IntelDX4™ PROCESSOR

SmartDie™ Product Specification

- **High Performance Design**
  - **100 MHz Version Uses 33 MHz External Bus**
  - **75 MHz Version Uses 25 MHz External Bus**
  - **RISC Integer Core**
  - **Frequent Instruction Execution in One Core Clock**
  - **80, 106 Mbyte/sec Burst Bus**
  - **On Chip Floating Point Unit**
  - **Paged, Virtual Memory Management**
  - **Complete 32-Bit Architecture**
- **On-Chip 16 KByte Write-Back Cache**
  - **Write-back Enhanced**
  - **Unified Code and Data**
  - **4-Way 16-Byte Line Size**
  - **Software Transparent**
- **Binary Compatible with Large Software Base**
  - **MS-DOS*, Windows*, OS/2*, UNIX***
- **0.6 Micron BiCMOS Silicon Technology**
- **Low Power Consumption**
  - **3.3V Core Operation**
  - **SL Enhanced Features**
  - **Static Design**
- **Ease of Design**
  - **5V Tolerant Input Buffers with TTL Compatible Outputs**
  - **Hardware Debugging Support**
- **Testability**
  - **IEEE 1149.1 Boundary Scan Compatibility**
  - **Built-In Self Test**
- **Multiprocessor Support**
  - **Multiprocessor Instructions**
  - **Support for Second Level Cache**
- **Intel SmartDie™ Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C to 95°C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest SmartDie™ product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet for this product. Please reference the Standard Package Data Book (Order No. 242202) for additional product information and specifications not found in this document.

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December 1995 **Order Number: 272752-001**

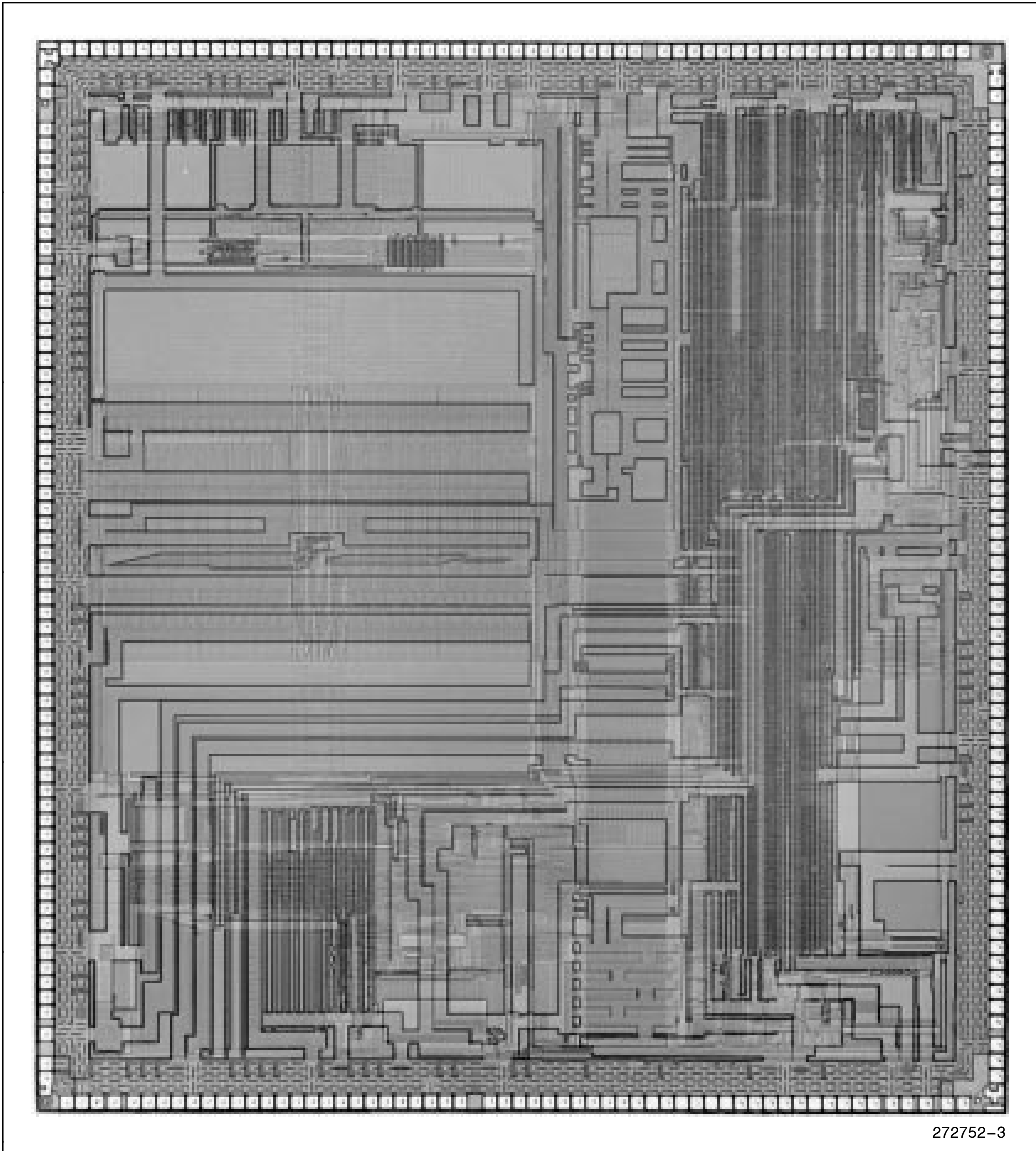

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Figure 1. Write-Back Enhanced IntelDX4™ Processor Die Photo

1.0 DIE SPECIFICATIONS

The plot and the die photo on the opposite page indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name "8HE4S" appears on IntelDX4™ die.

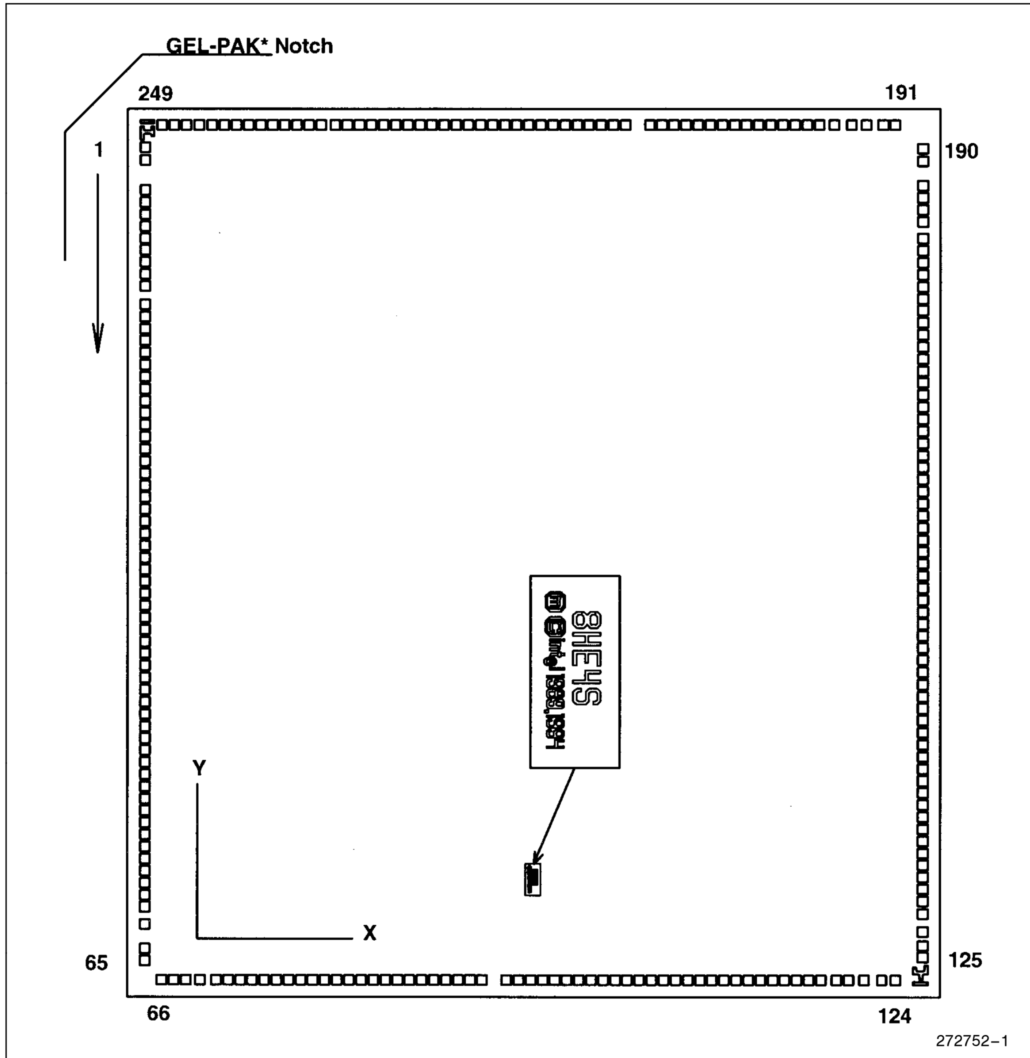


Figure 2. Write-Back Enhanced IntelDX4™ Processor Die/Bond Pad Layout

1.1 Pad Description

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data

PAD #	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
001	V_{SS}	−150.3	157.4	−3818	3998
002	V_{CC}	−150.3	152.4	−3818	3871
003	A25	−150.3	140.7	−3818	3575
004	A26	−150.3	136.1	−3818	3456
005	A27	−150.3	131.4	−3818	3337
006	A28	−150.3	126.7	−3818	3219
007	V_{CC}	−150.3	122.0	−3818	3100
008	A29	−150.3	117.4	−3818	2981
009	A30	−150.3	112.7	−3818	2862
010	A31	−150.3	108.0	−3818	2744
011	V_{SS}	−150.3	103.3	−3818	2623
012	V_{SS}	−150.3	96.2	−3818	2443
013	V_{CC}	−150.3	91.5	−3818	2324
014	DP0	−150.3	86.8	−3818	2205
015	D0	−150.3	82.2	−3818	2087
016	D1	−150.3	77.5	−3818	1968
017	D2	−150.3	72.8	−3818	1849
018	D3	−150.3	68.1	−3818	1730
019	D4	−150.3	63.5	−3818	1612
020	V_{CC}	−150.3	58.8	−3818	1493
021	V_{SS}	−150.3	54.1	−3818	1374
022	V_{CC}	−150.3	49.4	−3818	1255
023	V_{SS}	−150.3	44.8	−3818	1137
024	V_{SS}	−150.3	40.1	−3818	1018
025	V_{CC}	−150.3	35.4	−3818	899
026	V_{CC}	−150.3	30.7	−3818	780
027	V_{SS}	−150.3	26.0	−3818	662
028	N.C.	−150.3	21.4	−3818	543
029	V_{CC}	−150.3	16.7	−3818	424
030	V_{CC}	−150.3	12.0	−3818	305
031	V_{SS}	−150.3	7.3	−3818	187
032	N.C.	−150.3	2.7	−3818	68
033	V_{SS}	−150.3	−2.0	−3818	−51
034	V_{CC}	−150.3	−6.7	−3818	−170
035	D5	−150.3	−11.4	−3818	−288
036	D6	−150.3	−16.0	−3818	−407
037	V_{SS}	−150.3	−20.7	−3818	−526
038	V_{CC}	−150.3	−25.4	−3818	−645

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data (Continued)

PAD #	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
039	N.C.	−150.3	−30.1	−3818	−763
040	D7	−150.3	−34.7	−3818	−882
041	DP1	−150.3	−39.4	−3818	−1001
042	D8	−150.3	−44.1	−3818	−1120
043	D9	−150.3	−48.8	−3818	−1238
044	V_{SS}	−150.3	−53.4	−3818	−1357
045	V_{CC}	−150.3	−58.1	−3818	−1476
046	N.C.	−150.3	−62.8	−3818	−1595
047	V_{SS}	−150.3	−67.5	−3818	−1713
048	V_{CC}	−150.3	−72.1	−3818	−1832
049	D10	−150.3	−76.8	−3818	−1951
050	D11	−150.3	−81.5	−3818	−2070
051	D12	−150.3	−86.2	−3818	−2188
052	D13	−150.3	−90.8	−3818	−2307
053	V_{SS}	−150.3	−95.5	−3818	−2426
054	V_{CC}	−150.3	−100.2	−3818	−2545
055	D14	−150.3	−104.9	−3818	−2663
056	D15	−150.3	−109.5	−3818	−2782
057	V_{CC}	−150.3	−114.2	−3818	−2901
058	V_{SS}	−150.3	−118.9	−3818	−3020
059	V_{CC}	−150.3	−123.6	−3818	−3138
060	DP2	−150.3	−128.2	−3818	−3257
061	D16	−150.3	−132.9	−3818	−3376
062	V_{CC}	−150.3	−137.6	−3818	−3495
063	V_{SS}	−150.3	−144.5	−3818	−3671
064	V_{CC}	−150.3	−153.8	−3818	−3908
065	V_{SS}	−150.3	−158.5	−3818	−4026
066	V_{SS}	−143.8	−166.0	−3651	−4217
067	V_{CC}	−139.1	−166.0	−3533	−4217
068	D17	−134.4	−166.0	−3414	−4217
069	V_{CC}	−128.8	−166.0	−3271	−4217
070	D18	−122.8	−166.0	−3118	−4217
071	D19	−118.1	−166.0	−2999	−4217
072	D20	−113.4	−166.0	−2880	−4217
073	V_{CC}	−108.7	−166.0	−2762	−4217
074	V_{SS}	−104.1	−166.0	−2643	−4217
075	V_{CC}	−99.4	−166.0	−2524	−4217
076	V_{SS}	−94.7	−166.0	−2405	−4217
077	D21	−90.0	−166.0	−2287	−4217
078	D22	−85.4	−166.0	−2168	−4217

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data (Continued)

PAD #	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
079	D23	−80.7	−166.0	−2049	−4217
080	DP3	−76.0	−166.0	−1931	−4217
081	V_{CC}	−71.3	−166.0	−1812	−4217
082	V_{SS}	−66.7	−166.0	−1693	−4217
083	D24	−62.0	−166.0	−1574	−4217
084	V_{CC}	−57.3	−166.0	−1456	−4217
085	D25	−52.6	−166.0	−1337	−4217
086	D26	−48.0	−166.0	−1218	−4217
087	D27	−43.3	−166.0	−1099	−4217
088	V_{CC}	−38.6	−166.0	−980	−4217
089	V_{SS}	−33.9	−166.0	−862	−4217
090	V_{CC}	−29.3	−166.0	−743	−4217
091	D28	−24.6	−166.0	−624	−4217
092	D29	−19.9	−166.0	−506	−4217
093	V_{CC}	−10.6	−166.0	−268	−4217
094	V_{SS}	−5.9	−166.0	−149	−4217
095	D30	−1.2	−166.0	−31	−4217
096	D31	3.5	−166.0	88	−4217
097	STPCLK #	8.1	−166.0	207	−4217
098	IGNNE #	12.8	−166.0	326	−4217
099	INV	17.5	−166.0	445	−4217
100	CACHE #	22.2	−166.0	563	−4217
101	V_{SS}	26.9	−166.0	682	−4217
102	V_{CC}	31.5	−166.0	801	−4217
103	TDO	36.2	−166.0	920	−4217
104	N.C.	40.9	−166.0	1038	−4217
105	FERR #	45.6	−166.0	1157	−4217
106	N.C.	50.2	−166.0	1276	−4217
107	SMI #	54.9	−166.0	1395	−4217
108	N.C.	59.6	−166.0	1513	−4217
109	N.C.	64.3	−166.0	1632	−4217
110	WB/WT #	68.9	−166.0	1751	−4217
111	HITM #	73.6	−166.0	1869	−4217
112	V_{CC}	78.3	−166.0	1988	−4217
113	V_{SS}	83.0	−166.0	2107	−4217
114	V_{CC}	87.6	−166.0	2226	−4217
115	N.C.	92.3	−166.0	2345	−4217
116	SMIACT #	97.0	−166.0	2463	−4217
117	N.C.	101.7	−166.0	2582	−4217
118	SRESET	106.3	−166.0	2701	−4217

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data (Continued)

PAD #	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
119	N.C.	111.0	−166.0	2820	−4217
120	V_{SS}	116.9	−166.0	2969	−4217
121	V_{CC}	121.7	−166.0	3092	−4217
122	V_{SS}	127.6	−166.0	3241	−4217
123	V_{CC}	134.4	−166.0	3414	−4217
124	V_{SS}	139.7	−166.0	3547	−4217
125	V_{SS}	150.3	−157.2	3818	−3993
126	V_{CC}	150.3	−152.5	3818	−3874
127	V_{SS}	150.3	−147.2	3818	−3739
128	NMI	150.3	−140.3	3818	−3563
129	INTR	150.3	−135.3	3818	−3436
130	N.C.	150.3	−130.6	3818	−3317
131	FLUSH #	150.3	−125.9	3818	−3198
132	N.C.	150.3	−121.2	3818	−3079
133	RESET	150.3	−116.6	3818	−2961
134	A20M #	150.3	−111.9	3818	−2842
135	N.C.	150.3	−107.2	3818	−2723
136	EADS #	150.3	−102.5	3818	−2604
137	N.C.	150.3	−97.9	3818	−2486
138	V_{CC}	150.3	−93.2	3818	−2367
139	V_{CC}	150.3	−88.5	3818	−2248
140	V_{SS}	150.3	−83.8	3818	−2129
141	V_{CC}	150.3	−79.2	3818	−2011
142	PCD	150.3	−74.5	3818	−1892
143	PWT	150.3	−69.8	3818	−1773
144	D/C #	150.3	−65.1	3818	−1654
145	V_{CC}	150.3	−60.5	3818	−1536
146	M/IO #	150.3	−55.8	3818	−1417
147	V_{SS}	150.3	−51.1	3818	−1298
148	V_{SS}	150.3	−46.4	3818	−1179
149	V_{CC}	150.3	−41.8	3818	−1061
150	BE3 #	150.3	−37.1	3818	−942
151	BE2 #	150.3	−32.4	3818	−823
152	BE1 #	150.3	−27.7	3818	−704
153	BE0 #	150.3	−23.1	3818	−586
154	BREQ	150.3	−18.4	3818	−467
155	V_{CC}	150.3	−13.7	3818	−348
156	V_{SS}	150.3	−9.0	3818	−229
157	W/R #	150.3	−4.4	3818	−111
158	HLDA	150.3	0.3	3818	8

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data (Continued)

PAD#	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
159	V_{CC}	150.3	5.0	3818	127
160	CLK	150.3	9.7	3818	246
161	V_{CC}	150.3	14.3	3818	364
162	V_{CC}	150.3	19.0	3818	483
163	V_{SS}	150.3	23.7	3818	602
164	V_{CC}	150.3	28.4	3818	721
165	V_{SS}	150.3	33.0	3818	839
166	V_{CC}	150.3	37.7	3818	958
167	TCK	150.3	42.4	3818	1077
168	N.C.	150.3	47.1	3818	1196
169	AHOLD	150.3	51.7	3818	1314
170	HOLD	150.3	56.4	3818	1433
171	N.C.	150.3	61.1	3818	1552
172	V_{SS}	150.3	65.8	3818	1671
173	V_{CC}	150.3	70.4	3818	1789
174	KEN#	150.3	75.1	3818	1908
175	RDY#	150.3	79.8	3818	2027
176	N.C.	150.3	84.5	3818	2146
177	CLKMUL	150.3	89.1	3818	2264
178	V_{SS}	150.3	93.8	3818	2383
179	V_{SS}	150.3	98.5	3818	2502
180	V_{CC}	150.3	103.2	3818	2621
181	BS8#	150.3	107.9	3818	2739
182	BS16#	150.3	112.5	3818	2858
183	BOFF#	150.3	117.2	3818	2977
184	BRDY#	150.3	121.9	3818	3096
185	PCHK#	150.3	128.4	3818	3263
186	N.C.	150.3	133.1	3818	3381
187	$V_{CC}5$	150.3	137.8	3818	3500
188	V_{SS}	150.3	142.5	3818	3619
189	V_{CC}	150.3	152.0	3818	3860
190	V_{SS}	150.3	156.8	3818	3984
191	V_{SS}	139.6	166.0	3546	4217
192	V_{CC}	134.9	166.0	3427	4217
193	LOCK#	128.4	166.0	3261	4217
194	PLOCK#	122.8	166.0	3118	4217
195	V_{CC}	115.9	166.0	2944	4217
196	BLAST#	110.3	166.0	2802	4217
197	ADS#	105.6	166.0	2683	4217
198	A2	100.8	166.0	2560	4217

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data (Continued)

PAD#	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
199	V_{SS}	96.1	166.0	2441	4217
200	V_{CC}	91.4	166.0	2322	4217
201	V_{SS}	86.8	166.0	2203	4217
202	V_{CC}	82.1	166.0	2085	4217
203	A3	77.4	166.0	1966	4217
204	A4	72.7	166.0	1847	4217
205	A5	68.1	166.0	1729	4217
206	UP#	63.4	166.0	1610	4217
207	A6	58.7	166.0	1491	4217
208	A7	54.0	166.0	1372	4217
209	V_{CC}	49.4	166.0	1254	4217
210	V_{CC}	44.7	166.0	1135	4217
211	A8	35.3	166.0	897	4217
212	V_{SS}	30.6	166.0	778	4217
213	V_{CC}	26.0	166.0	660	4217
214	A9	21.3	166.0	541	4217
215	A10	16.6	166.0	422	4217
216	V_{SS}	11.9	166.0	303	4217
217	V_{CC}	7.3	166.0	185	4217
218	V_{SS}	2.6	166.0	66	4217
219	V_{CC}	−2.1	166.0	−53	4217
220	A11	−6.8	166.0	−171	4217
221	V_{SS}	−11.4	166.0	−290	4217
222	A12	−16.1	166.0	−409	4217
223	V_{CC}	−20.8	166.0	−528	4217
224	A13	−25.5	166.0	−646	4217
225	A14	−30.1	166.0	−765	4217
226	V_{CC}	−34.8	166.0	−884	4217
227	V_{SS}	−39.5	166.0	−1003	4217
228	A15	−44.2	166.0	−1121	4217
229	A16	−48.8	166.0	−1240	4217
230	V_{SS}	−53.5	166.0	−1359	4217
231	V_{CC}	−58.2	166.0	−1478	4217
232	A17	−62.9	166.0	−1596	4217
233	V_{SS}	−67.5	166.0	−1715	4217
234	V_{SS}	−72.2	166.0	−1834	4217
235	V_{CC}	−76.9	166.0	−1953	4217
236	TDI	−82.3	166.0	−2091	4217
237	TMS	−87.0	166.0	−2209	4217
238	A18	−91.7	166.0	−2328	4217

Table 1. Write-Back Enhanced IntelDX4™ Processor Bond Pad Center Data (Continued)

PAD#	SIGNAL	Pad Center			
		Mils		Microns	
		X	Y	X	Y
239	A19	−96.3	166.0	−2447	4217
240	A20	−101.0	166.0	−2566	4217
241	V_{SS}	−105.7	166.0	−2684	4217
242	V_{CC}	−110.4	166.0	−2803	4217
243	V_{CC}	−115.0	166.0	−2922	4217
244	A21	−119.7	166.0	−3041	4217
245	A22	−124.5	166.0	−3161	4217
246	A23	−129.4	166.0	−3286	4217
247	A24	−134.4	166.0	−3415	4217
248	V_{CC}	−139.2	166.0	−3535	4217
249	V_{SS}	−143.9	166.0	−3654	4217

Bond Pad Center Notes:
1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   103 (TDO), 167 (TCK), 236(TDI), 237(TMS)
5. $V_{CC}5$ (pad #187) is a 5V input signal.

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent package unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAK with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel Smart Die
- Intel Part Number
- Assembly Process Order/Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:
GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines the Write-Back Enhanced IntelDX4 processor physical specifications.

Table 2. Write-Back Enhanced IntelDX4™ Processor Physical Specifications

Die Revision:	A-2
Post-Saw Die Dimensions:	Mils: X = 313 ± 0.5, Y = 344 ± 0.5 See associated Die/Bond Pad Layout for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	118.75 microns (4.7 mils)
Pad Passivation Opening Size:	Mils: 3.7 x 3.7 (single pads) Microns: 95 x 95 (single pads)
Bond Pad Metalization: (outermost layer first)	14,000 Angstroms Al (0.5% Cu), 1000 Angstroms Ti, 365 Angstroms TiN
Pads per Die:	249
Die Backside Material: (outermost layer first)	1600 Angstroms Gold, 150 Angstroms Chrome
Passivation: (outermost layer first)	6.13 microns polyimide, 0.45 microns nitride
Intel Fabrication Process:	BiCMOS (min. feature size 0.6 microns)

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature .... 0°C to +70°C
Junction Temperature Under Bias .... −65°C to +110°C
Supply Voltage V_{CC} wrt V_{SS} .... −0.5V to +6.5V
Voltage on Other Pads .... −0.5V to V_{CC} +0.5V

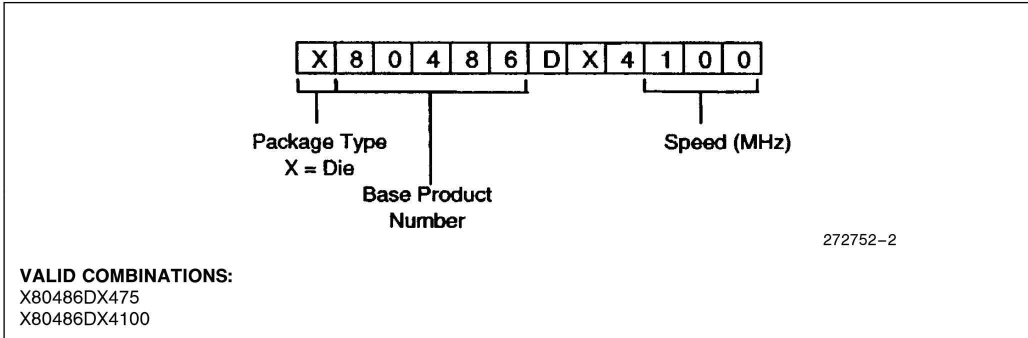
OPERATING CONDITIONS*

T_J (Junction Temperature Under Bias) .... 0°C to 95°C
Substrate Bias . . Float (Self Biasing to V_{SS}), Alternative is to Drive V_{SS}
Digital Supply Voltage .... 3.3V ± 0.3V
Core Operating Frequency .... 75, 100 MHz (25, 33 MHz Bus)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest SmartDie Product Specification before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



VALID COMBINATIONS:
X80486DX475
X80486DX4100

5.0 REFERENCE INFORMATION

Title	Order No.
Intel486™ Microprocessor Family Data Sheet	242202
Intel486 Microprocessor Hardware Reference Manual	240552
Intel486 Microprocessor Family Programmer's Reference Manual	240486
Intel486 Microprocessors and Related Products Data Book	241731

6.0 REVISION HISTORY

Rev	Date	Description
001	10/95	Original Version.