PRELIMINARY

Intel486™ SX MICROPROCESSOR

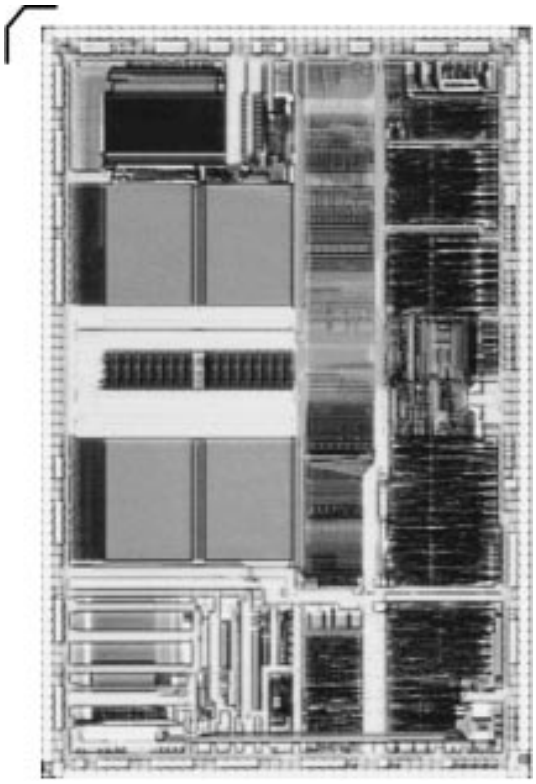
SmartDie™ Product Specification

- **SL Technology for Energy Efficiency**
  - **— Intel's System Management Mode**
  - **— Stop Clock, Auto HALT and Auto Idle Power Down**
- **Binary-Compatible with Large Software Base**
  - **— MS-DOS*, OS/2*, Windows***
  - **— UNIX* System V/386**
  - **— iRMX Software, iRMK Kernels**
- **High Integration Enables On-Chip**
  - **— 8 Kbyte Code and Data Cache**
  - **— Paged, Virtual Memory Management**
- **Easy to Use**
  - **— Built-In Self Test**
  - **— Hardware Debugging Support**
  - **— Intel Software Support**
  - **— Extensive Third Party Software Support**
- **High-Performance Design**
  - **— Intel486 One Clock Instruction Core**
  - **— 80/100 Mbyte/sec Burst Bus at 25/33 MHz**
  - **— CHMOS V Process Technology**
  - **— Dynamic Bus Sizing for 8-Bit, 16-Bit and 32-Bit Buses**
- **Complete 32-Bit Architecture**
  - **— Address and Data Buses**
  - **— Registers**
  - **— 8-Bit, 16-Bit and 32-Bit Data Types**
- **Multiprocessor Support**
  - **— Multiprocessor Instructions**
  - **— Cache Consistency Protocols**
  - **— Support for Second-Level Cache**
- **IEEE 1149.1 Boundary Scan Compatibility**
- **Intel SmartDie Product**
  - **— Full AC/DC Testing at Die Level**
  - **— 0°C to +80°C (Junction) Temperature Range**
  - **— 25 MHz and 33 MHz Speeds @ 3.3V**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice. Verify with your local Intel Sales Office that you have the latest SmartDie product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet/Book (Order No. 242202) for additional product information and specifications not found in this document.

January 1995 **Order Number: 271292-002**



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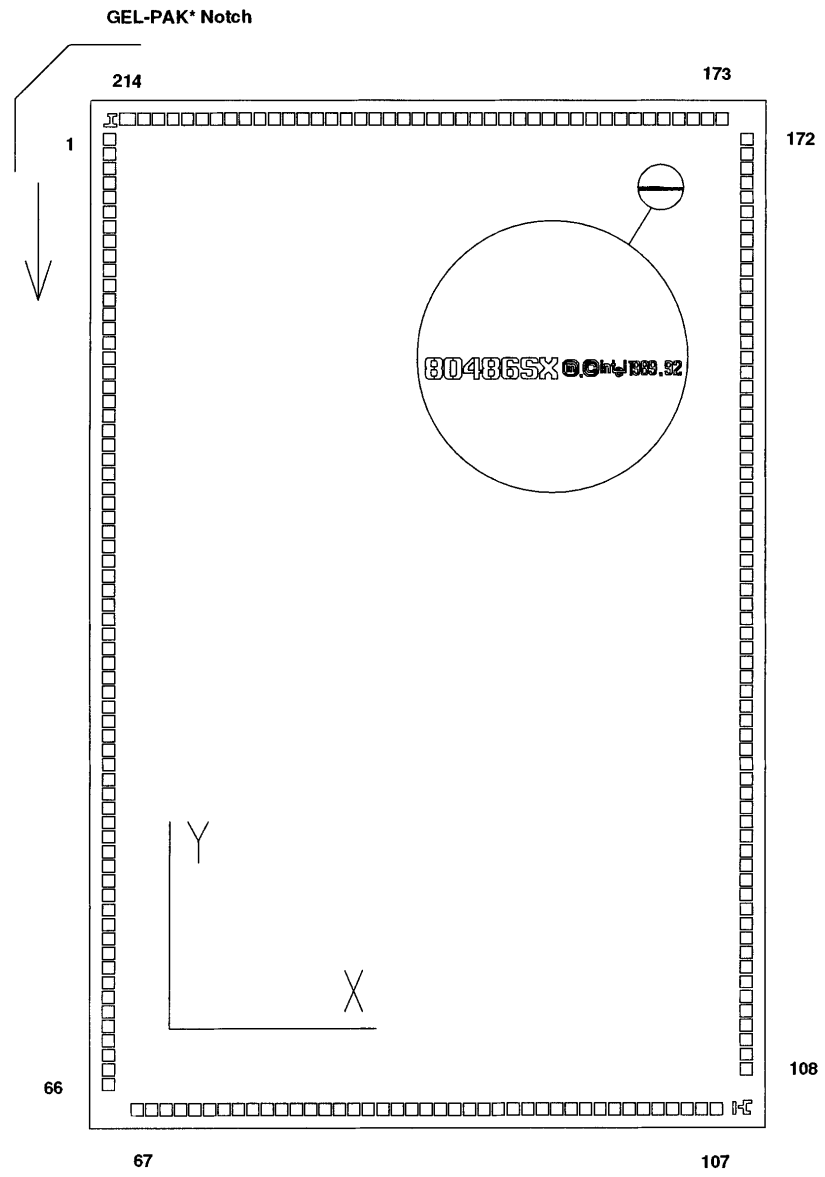
Intel486™ SX Microprocessor Die Photo

1.0 DIE SPECIFICATIONS



NOTE:
This drawing indicates orientation of the die in the GEL-PAK (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK.

Figure 1. Intel486™ SX Microprocessor Die/Bond Pad Layout

1.1 Pad Description

Table 1. Intel486™ SX Microprocessor Bond Pad Center Data

Pad	Signal	Pad Center (Mils = 0.001 in.) X	Pad Center (Mils = 0.001 in.) Y	Pad Center (Microns) X	Pad Center (Microns) Y
001	V_{CC}	−123.7	183.3	−3142	4657
002	V_{SS}	−123.7	177.7	−3142	4514
003	A21	−123.7	172.1	−3142	4372
004	A22	−123.7	166.5	−3142	4229
005	A23	−123.7	160.9	−3142	4087
006	A24	−123.7	155.3	−3142	3944
007	V_{CC}	−123.7	149.7	−3142	3802
008	V_{SS}	−123.7	144.1	−3142	3659
009	A25	−123.7	138.5	−3142	3517
010	A26	−123.7	132.9	−3142	3374
011	A27	−123.7	127.2	−3142	3232
012	A28	−123.7	121.6	−3142	3089
013	V_{CC}	−123.7	116.0	−3142	2947
014	V_{SS}	−123.7	110.4	−3142	2804
015	A29	−123.7	104.8	−3142	2662
016	A30	−123.7	99.2	−3142	2519
017	A31	−123.7	93.6	−3142	2377
018	N.C.	−123.7	88.0	−3142	2234
019	DP0	−123.7	82.4	−3142	2092
020	D0	−123.7	76.7	−3142	1949
021	D1	−123.7	71.1	−3142	1807
022	D2	−123.7	65.5	−3142	1664
023	D3	−123.7	59.9	−3142	1522
024	D4	−123.7	54.3	−3142	1379
025	V_{CC}	−123.7	48.7	−3142	1237
026	V_{SS}	−123.7	43.1	−3142	1094
027	V_{CC}	−123.7	37.5	−3142	952
028	V_{SS}	−123.7	31.9	−3142	809
029	V_{CC}	−123.7	26.3	−3142	667
030	V_{SS}	−123.7	20.6	−3142	524
031	V_{SS}	−123.7	15.0	−3142	382
032	V_{CC}	−123.7	9.4	−3142	239
033	V_{SS}	−123.7	3.8	−3142	97
034	V_{CC}	−123.7	−1.8	−3142	−46
035	V_{SS}	−123.7	−7.4	−3142	−188
036	V_{CC}	−123.7	−13.0	−3142	−331
037	V_{CC}	−123.7	−18.6	−3142	−473
038	V_{SS}	−123.7	−24.2	−3142	−616
039	D5	−123.7	−29.8	−3142	−758
040	D6	−123.7	−35.5	−3142	−901
041	V_{CC}	−123.7	−41.1	−3142	−1043
042	V_{SS}	−123.7	−46.7	−3142	−1186
043	D7	−123.7	−52.3	−3142	−1328
044	DP1	−123.7	−57.9	−3142	−1471
045	D8	−123.7	−63.5	−3142	−1613
046	D9	−123.7	−69.1	−3142	−1756
047	V_{CC}	−123.7	−74.7	−3142	−1898
048	V_{SS}	−123.7	−80.3	−3142	−2041
049	V_{CC}	−123.7	−85.9	−3142	−2183
050	V_{SS}	−123.7	−91.6	−3142	−2326
051	V_{SS}	−123.7	−97.2	−3142	−2468
052	D10	−123.7	−102.8	−3142	−2611
053	D11	−123.7	−108.4	−3142	−2753
054	D12	−123.7	−114.0	−3142	−2896
055	D13	−123.7	−119.6	−3142	−3038
056	V_{CC}	−123.7	−125.2	−3142	−3181
057	V_{SS}	−123.7	−130.8	−3142	−3323
058	V_{CC}	−123.7	−136.4	−3142	−3466
059	V_{SS}	−123.7	−142.1	−3142	−3608
060	D14	−123.7	−147.7	−3142	−3751
061	D15	−123.7	−153.3	−3142	−3893
062	DP2	−123.7	−158.9	−3142	−4036

Table 1. Intel486™ SX Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
063	D16	−123.7	−164.5	−3142	−4178
064	V_{SS}	−123.7	−170.1	−3142	−4321
065	V_{CC}	−123.7	−175.7	−3142	−4463
066	V_{SS}	−123.7	−181.3	−3142	−4606
067	V_{SS}	−112.6	−191.1	−2859	−4854
068	D17	−106.9	−191.1	−2716	−4854
069	V_{CC}	−101.3	−191.1	−2574	−4854
070	D18	−95.7	−191.1	−2431	−4854
071	D19	−90.1	−191.1	−2289	−4854
072	D20	−84.5	−191.1	−2146	−4854
073	V_{SS}	−78.9	−191.1	−2004	−4854
074	V_{CC}	−73.3	−191.1	−1861	−4854
075	D21	−67.7	−191.1	−1719	−4854
076	D22	−62.1	−191.1	−1576	−4854
077	D23	−56.5	−191.1	−1434	−4854
078	DP3	−50.8	−191.1	−1291	−4854
079	V_{CC}	−45.2	−191.1	−1149	−4854
080	V_{SS}	−39.6	−191.1	−1006	−4854
081	D24	−34.0	−191.1	−864	−4854
082	D25	−28.4	−191.1	−721	−4854
083	D26	−22.8	−191.1	−579	−4854
084	D27	−17.2	−191.1	−436	−4854
085	V_{SS}	−11.6	−191.1	−294	−4854
086	V_{CC}	−6.0	−191.1	−151	−4854
087	V_{CC}	−0.4	−191.1	−9	−4854
088	V_{SS}	5.3	−191.1	134	−4854
089	D28	10.9	−191.1	276	−4854
090	D29	16.5	−191.1	419	−4854
091	D30	22.1	−191.1	561	−4854
092	D31	27.7	−191.1	704	−4854
093	STPCLK#	33.5	−191.1	852	−4854
094	V_{SS}	39.1	−191.1	994	−4854
095	V_{CC}	44.8	−191.1	1137	−4854
096	TDO	50.4	−191.1	1279	−4854
097	SMI#	56.0	−191.1	1422	−4854
098	V_{SS}	61.6	−191.1	1564	−4854
099	V_{CC}	67.2	−191.1	1707	−4854
100	V_{SS}	72.8	−191.1	1849	−4854
101	V_{CC}	78.4	−191.1	1992	−4854
102	SMIACT#	84.0	−191.1	2134	−4854
103	SRESET	89.6	−191.1	2277	−4854
104	NMI	95.2	−191.1	2419	−4854
105	INTR	100.9	−191.1	2562	−4854
106	FLUSH#	106.5	−191.1	2704	−4854
107	V_{SS}	112.1	−191.1	2847	−4854
108	V_{SS}	123.7	−175.7	3142	−4463
109	RESET	123.7	−170.1	3142	−4321
110	A20M#	123.7	−164.5	3142	−4178
111	EADS#	123.7	−158.9	3142	−4036
112	V_{SS}	123.7	−153.3	3142	−3893
113	V_{CC}	123.7	−147.7	3142	−3751
114	V_{SS}	123.7	−142.1	3142	−3608
115	V_{CC}	123.7	−136.4	3142	−3466
116	PCD	123.7	−130.8	3142	−3323
117	PWT	123.7	−125.2	3142	−3181
118	D/C#	123.7	−119.6	3142	−3038
119	M/IO#	123.7	−114.0	3142	−2896
120	V_{SS}	123.7	−108.4	3142	−2753
121	V_{SS}	123.7	−102.8	3142	−2611
122	V_{CC}	123.7	−97.2	3142	−2468
123	BE3#	123.7	−91.6	3142	−2326
124	BE2#	123.7	−85.9	3142	−2183

Table 1. Intel486™ SX Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
125	BE1#	123.7	−80.3	3142	−2041
126	BE0#	123.7	−74.7	3142	−1898
127	BREQ	123.7	−69.1	3142	−1756
128	V_{SS}	123.7	−63.5	3142	−1613
129	V_{CC}	123.7	−57.9	3142	−1471
130	V_{SS}	123.7	−52.3	3142	−1328
131	V_{CC}	123.7	−46.7	3142	−1186
132	W/R#	123.7	−41.1	3142	−1043
133	HLDA	123.7	−35.5	3142	−901
134	CLK	123.7	−29.8	3142	−758
135	V_{SS}	123.7	−24.2	3142	−616
136	V_{CC}	123.7	−18.6	3142	−473
137	V_{SS}	123.7	−13.0	3142	−331
138	V_{CC}	123.7	−7.4	3142	−188
139	V_{SS}	123.7	−1.8	3142	−46
140	V_{CC}	123.7	3.8	3142	97
141	V_{SS}	123.7	9.4	3142	239
142	V_{CC}	123.7	15.0	3142	382
143	N.C.	123.7	20.6	3142	524
144	TCK	123.7	26.3	3142	667
145	AHOLD	123.7	31.9	3142	809
146	HOLD	123.7	37.5	3142	952
147	V_{SS}	123.7	43.1	3142	1094
148	V_{CC}	123.7	48.7	3142	1237
149	KEN#	123.7	54.3	3142	1379
150	RDY#	123.7	59.9	3142	1522
151	N.C.	123.7	65.5	3142	1664
152	V_{SS}	123.7	71.1	3142	1807
153	V_{CC}	123.7	76.7	3142	1949
154	BS8#	123.7	82.4	3142	2092
155	BS16#	123.7	88.0	3142	2234
156	BOFF#	123.7	93.6	3142	2377
157	BRDY#	123.7	99.2	3142	2519
158	PCHK#	123.7	104.8	3142	2662
159	N.C.	123.7	110.4	3142	2804
160	V_{SS}	123.7	116.0	3142	2947
161	V_{CC}	123.7	121.6	3142	3089
162	V_{SS}	123.7	127.2	3142	3232
163	V_{CC}	123.7	132.9	3142	3374
164	LOCK#	123.7	138.5	3142	3517
165	PLOCK#	123.7	144.1	3142	3659
166	V_{SS}	123.7	149.7	3142	3802
167	V_{CC}	123.7	155.3	3142	3944
168	BLAST#	123.7	160.9	3142	4087
169	ADS#	123.7	166.5	3142	4229
170	A2	123.7	172.1	3142	4372
171	V_{SS}	123.7	177.7	3142	4514
172	V_{CC}	123.7	183.3	3142	4657
173	V_{CC}	114.1	191.1	2897	4854
174	V_{SS}	108.5	191.1	2755	4854
175	A3	102.9	191.1	2613	4854
176	A4	97.2	191.1	2470	4854
177	A5	91.6	191.1	2327	4854
178	UP#	86.0	191.1	2185	4854
179	A6	80.4	191.1	2042	4854
180	A7	74.8	191.1	1900	4854
181	A8	69.2	191.1	1757	4854
182	V_{SS}	63.6	191.1	1615	4854
183	V_{CC}	58.0	191.1	1472	4854
184	V_{SS}	52.4	191.1	1330	4854

Table 1. Intel486™ SX Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.) X	Pad Center (Mils = 0.001 in.) Y	Pad Center (Microns) X	Pad Center (Microns) Y
185	V_{CC}	46.8	191.1	1187	4854
186	A9	41.1	191.1	1045	4854
187	A10	35.5	191.1	902	4854
188	V_{SS}	29.9	191.1	760	4854
189	V_{CC}	24.3	191.1	617	4854
190	V_{SS}	18.7	191.1	475	4854
191	V_{CC}	13.1	191.1	332	4854
192	V_{SS}	7.5	191.1	190	4854
193	V_{CC}	1.9	191.1	47	4854
194	A11	−3.7	191.1	−95	4854
195	N.C.	−9.4	191.1	−237	4854
196	A12	−15.0	191.1	−380	4854
197	V_{SS}	−20.6	191.1	−522	4854
198	V_{CC}	−26.2	191.1	−665	4854
199	A13	−31.8	191.1	−807	4854
200	A14	−37.4	191.1	−950	4854
201	V_{SS}	−43.0	191.1	−1092	4854
202	V_{CC}	−48.6	191.1	−1235	4854
203	A15	−54.2	191.1	−1377	4854
204	A16	−59.8	191.1	−1520	4854
205	A17	−65.5	191.1	−1662	4854
206	V_{SS}	−71.1	191.1	−1805	4854
207	V_{CC}	−76.7	191.1	−1947	4854
208	TDI	−82.3	191.1	−2090	4854
209	TMS	−87.9	191.1	−2232	4854
210	A18	−93.5	191.1	−2375	4854
211	A19	−99.1	191.1	−2518	4854
212	A20	−104.7	191.1	−2660	4854
213	V_{SS}	−110.3	191.1	−2802	4854
214	V_{CC}(4)	−116.6	191.1	−2963	4854

NOTES:
1. N.C. signifies no connect. These pads must not be connected.
2. The symbol ''#'' is used at the end of the signal name to denote an active low signal.
3. X-Y pad coordinates represent bond pad centers and are relative to center of die.
4. Double bond pad opening.

2.0 INTEL DIE PRODUCTS PROCESSING

TEST PROCEDURE

Intel has instituted full-speed functional testing at the die level for all SmartDie™ products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

WAFER PROBE

Wafer probing is performed on every wafer produced in an Intel Fab. The process consists of specific electrical tests as well as device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications.

Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the--wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then sorted for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

WAFER SAW

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts completely through the wafer.

DIE INSPECTION

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAK*s for shipment.

*GEL-PAK™ is a trademark of Vichem Corporation.

PACKING PROCEDURE

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Device Type
- Spec
- Customer Part Number (if applicable)
- Fab
- Quantity
- APO
- Date
- ROM Code (if applicable)

NOTE:
GEL-PAKs require a Vacuum Release Station. For additional information about GEL-PAK's, contact Vichem Corporation.

INSPECTION STEPS

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

STORAGE REQUIREMENTS

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

ESD

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Intel486™ SX Microprocessor Physical Specifications

Substrate Bias Condition: V_{SS}

Post-Saw Die Dimensions:

Mils: X = 261 ±0.5, Y = 396 ±0.5

See associated Die/Bond Pad Layout for X,Y orientation.

Die Backside Metalization: (from substrate)
200 Å Chrome ±100 Å
1500 Å Gold ±500 Å

Pad Passivation Opening Size:
Mils: 4.6 x 4.6 (single pads),
6.1 x 4.6 (double-wide pads)
Microns: 117.5 x 117.5 (single pads),
153.9 x 117.5 (double-wide pads)

Die Thickness: 17 (±1 mil) mils

Minimum Pad Pitch:
Pads may not be evenly pitched. Minimum pitch is 142.5 microns (5.6 mils).

Bond Pad Metalization (outer most layer first)
1.0 micron Al—0.5% Copper, 0.1 micron Titanium

Die Revision: aC-0

Pads per Die: 214

Intel Fabrication Process: CHMOS V (min. feature size 0.8 microns)

Passivation: (outer most layer first)
5.0 ±0.7 microns Polyimide.
0.6 ±0.1 microns Silicon Nitride

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature . . . . . 0°C to +70°C

Junction Temperature
Under Bias . . . . . −65°C to +110°C

Supply Voltage with
Respect to V_{SS} . . . . . −0.5V to +6.5V

Voltage on Other Pads . . . . . −0.5 V to V_{CC} + 0.5V

OPERATING CONDITIONS*

V_{CC} (Digital Supply Voltage) . . . . . 3.3V ±0.3V

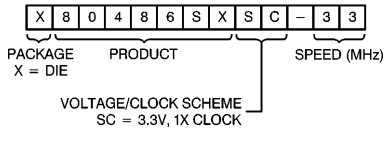
T_J (Junction Temperature
Under Bias) . . . . . 0°C to +80°C

Operating Frequency . . . . . 25/33 MHz

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



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5.0 ADDITIONAL INFORMATION

Title	Order No.
Intel486™ Microprocessor Family Data Sheet	242202
Intel486™ Microprocessor Hardware Reference Manual	240552
Intel486™ Microprocessor Family Programmer's Reference Manual	240486

6.0 REVISION HISTORY

Rev	Date	Description
-001	3/94	Original release.
-002	10/94	aC-0 Stepping. 33 MHz Speed Added