DATASHEET ADDENDUM

Intel 430HX PCIset
82439HX System Controller (TXC) Timing Specification

272945-001

September, 1996

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-764
or call 1-800-548-4725

Intel 430HX PCIset
82439HX SYSTEM CONTROLLER (TXC) FEATURES

- **Supports the Pentium® Processor at 66 MHz, 60 MHz, and 50 MHz at 3 V**
- **Supports the Universal Serial Bus (USB)**
- **Dual Processor Support**
- **PCI 2.1 Compliant**
- **Integrated Second Level Cache Controller**
  - **— Direct Mapped Organization**
  - **— Write-Back Cache Policy**
  - **— Cacheless, 256 Kbytes, and 512 Kbytes**
  - **— Pipelined Burst SRAMs**
  - **— Cache Hit Read/Write Cycle Timings at 3-1-1-1**
  - **— Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1**
  - **— Integrated Tag/Valid Status Bits for Cost Savings and Performance**
  - **— Optional 512 MB DRAM Cacheability Limit**
  - **— Supports 5 V SRAMs for Tag Address**
- **Integrated DRAM Controller**
  - **— 4 Mbytes to 512 Mbytes Memory**
  - **— 64-Mbit DRAM Technology Support**
  - **— Asymmetric DRAM Support**
  - **— 8 Qword Deep Merging DRAM Write Buffer**
  - **— Enhanced EDO/Hyper Page Mode DRAM Supports 4-2-2-2 Reads and x-2-2-2 Writes at 60 MHz, 5-2-2-2 Reads and x-2-2-2 Writes at 66 MHz**
  - **— 8 RAS Lines Available**
  - **— Integrated Programmable-Strength MA Buffers**
  - **— CAS-Before-RAS Refresh**
- **Optional Parity**
- **Optional Error Checking and Correction (ECC)**
  - **— Superior DRAM Data Integrity**
  - **— Single-Bit Error Correction, Multi-Bit Error Detection plus Nibble Failure Detection ECC Code**
  - **— Single- and Multi-bit Error Reporting**
  - **— Virtual Swapable Bank Support (i.e., can swap out problem banks)**
  - **— Merging Write Buffer Eliminates Most Partial Write Cycles**
- **Fully Synchronous, Minimum Latency 25/30/33 MHz PCI Bus Interface**
  - **— Zero Wait State CPU-to-PCI Write Timings for Superior Graphics Performance**
  - **— Enhanced CPU-to-PCI Read Latencies for Superior Graphics/PIO Performance**
  - **— 21 DWORD PCI-DRAM Post Buffer**
  - **— 22 DWord PCI-to-DRAM Read Prefetch Buffer**
  - **— Writeback Merging for PCI-to-DRAM Writes**
  - **— Writeback Forwarding for PCI-to-DRAM Reads**
  - **— Pipelined Snoop Ahead**
  - **— Multi-Transaction Timer to Support Multiple Short PCI Transactions Within the Same PCI Arbitration Cycle**
- **Single 324-Pin BGA Package**

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet published for the Intel 430HX PCIset. Please refer to the standard package datasheet (order number 290551) for product information and specifications not found in this document.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

82439HX System Controller (TXC) Timing Specification

FIGURES

TABLES

1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C
Storage Temperature ..... -55°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3 V to VDD + 0.3 V
Maximum Power Dissipation ..... 1.26 W

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.*

1.2 Thermal Characteristics

The 82439HX is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the 82439HX BGA (Ball Grid Array) package are given in Table 1.

Table 1. 82439HX System Controller (TXC) Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/Watt)	29.0	24.5
θ_{jc} (°C/Watt)	9.0	

1.3 D.C. Characteristics

Table 2. 82439HX System Controller (TXC) D.C. Characteristics
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Notes 1,8; VDD3 = 3.135 V
V_{IH1}	Input High Voltage	2.0	VDD3 + 0.3	V	Notes 1,9; VDD3 = 3.6V
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2; VDD = 4.75V
V_{IH2}	Input High Voltage	2.0	VDD + 0.3	V	Note 2; VDD = 5.25V
V_{IL3}	Input Low Voltage	-0.4	0.8	V	Note 3; VDD3 = 3.135
V_{IH3}	Input High Voltage	2.8	VDD3 + 0.3	V	Note 3; VDD3 = 3.6
V_{OL1}	Output Low Voltage		0.4	V	Note 4
V_{OH1}	Output High Voltage	2.4		V	Note 4
I_{OL1}	Output Low Current		4	mA	Note 5
I_{OH1}	Output High Current	-2		mA	Note 5
I_{OL2}	Output Low Current		8	mA	Note 6
I_{OH2}	Output High Current	-2		mA	Note 6
I_{OL3}	Output Low Current		12	mA	Note 7
I_{OH3}	Output High Current	-2		mA	Note 7
I_{IH1}	Input Leakage Current		10	µA	0 V<V_{in}<VDD/VDD3
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		10	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		10	pF	FC = 1 MHz
I_{CC}	V_{CC} Supply Current		10 350	mA mA	5 V Supply 3 V Supply

NOTES:

1. V_{IL1} and V_{IH1} apply to the following 3.3 V input signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#, SMIACT#, PHLD#, REQ[3:0]#, RST#, HCLKIN, PCLKIN as well the following signals when used as 3.3 V inputs during NAND tree testing: BRDY#, NA#, AHOLD, EADS#, BOFF#, KEN#/INV, CADV#, CADS#, CCS#, COE#, GWE#, BWE#, TWE#, MWE#, MA[11:2], MAA[1:0], MAB[1:0]
2. V_{IL2} and V_{IH2} apply to the following 5.0 V tolerant input signals: TIO[10:0], AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, SERR#, MD[63:0], MPD[7:0], HD[63:0]
3. V_{IL3} and V_{IH3} apply to the following input signals: TESTIN#, RST#
4. V_{OL1} and V_{OH1} apply to the following signals: TIO[10:0], TWE#, CADV#, CADS#, CCS#, COE#, GWE#, BWE#, A[31:3], HD[63:0], KEN#/INV, AHOLD, BRDY#, NA#, BOFF#, EADS#, MAA[1:0], MAB[1:0], MA[11:2], MWE#, MD[63:0], MPD[7:0], CAS[7:0]#, RAS[7:0]#, GNT[3:0]#, PHLDA#, AD[31:0], C/BE[3:0]#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, SERR#, PLOCK#
5. I_{OL1} and I_{OH1} apply to: BRDY#, NA#, AHOLD, EADS#, BOFF#, KEN#/INV, CADV#, CADS#, CCS#, COE#, GWE#, BWE#, TWE#, A[31:3], T10[10:0], MD[63:0], MPD[7:0]
6. I_{OL2} and I_{OH2} apply to: MWE#, MA[11:2], MAA[1:0], MAB[1:0], RAS[7:0]#, CAS[7:0]#, PHLDA#, GNT[3:0]#, HD[63:0]
7. I_{OL3} and I_{OH3} apply to: MWE#, MA[11:2], MAA[1:0], MAB[1:0] if programmed for 12 mA strength
8. For transient voltages, V_{IL1} min is V_{SS} - 1.4 V. This applies to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#.
9. For transient voltages, V_{IH1} max is VDD3 + 1.7 V. This applies to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#.

1.4 82439HX System Controller (TXC) AC Characteristics

All timings are in nanoseconds (ns), unless otherwise specified.

Table 3. Host Clock Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t1	HCLKIN Period	15.0	20.0	1	
	HCLKIN Period Stability		±100		pS
t3	HCLKIN High Time	6.0		1	
t4	HCLKIN Low Time	6.0		1	
t5	HCLKIN Rise Time		1.2	1	
t6	HCLKIN Fall Time		1.2	1	
	HCLKIN Rising Edge to PCLKIN Rising Edge Skew	1	6		HCLKIN must lead PCLKIN

Table 4. CPU Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C) (Sheet 1 of 2)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t7	ADS# Setup Time to HCLKIN Rising	5.0		4	
t7a	ADS# Hold Time from HCLKIN Rising	1.5		4	
t8	W/R# Setup Time to HCLKIN Rising	5.5		4	
t9	BE[7:0]# Setup Time to HCLKIN Rising	5.0		4	
t10	HITM# Setup Time to HCLKIN Rising	6.0		4	
t11	CACHE# Setup Time to HCLKIN Rising	5.0		4	
t11a	M/IO# Setup Time to HCLKIN Rising	6.0		4	
t12	D/C# Setup Time to HCLKIN Rising	5.0		4	
t13	HLOCK#, SMIACT# Setup Time to HCLKIN Rising	5.0		4	
t14	HITM#, W/R#, M/IO#, D/C#, BE[7:0], HLOCK#, CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.0		4	
t15	A[31:3] Setup Time to HCLKIN Rising	3.0		4	
t16	A[31:3] Hold Time from HCLKIN Rising	1.0		4	
t18	A[31:3] Valid Delay from HCLKIN Rising	2.0	13	3	0 pf

Table 4. CPU Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C) (Sheet 2 of 2)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t21	BRDY# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pf
t22	NA# Valid Delay from HCLKIN Rising	1.5	8.0	3	0 pf
t23	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t24	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t25	EADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t26	KEN#/INV Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t30	HD[63:0] Setup Time to HCLKIN Rising	3.0		4	
t31	HD[63:0] Hold Time from HCLKIN Rising	1.5		4	
t32	HD[63:0] Valid Delay from HCLKIN Rising	1.5	7.5	3	0 pf
t33	HD[63:0] Valid Delay from HCLKIN Rising, 66 Mhz ECC enabled	1.5	8.0	3	0 pf
t34	HD[63:0] Valid Delay from HCLKIN Rising, 60 Mhz 4 clk Leadoff, no L2	1.5	7.0	3	0 pf
t35	HD[63:0] Valid Delay from HCLKIN Rising, 66 MHz 5-222	1.5	6.0	3	0 pf

Table 5. Second Level Cache Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
Pipelined Burst SRAMs					
t40	COE# Valid Delay from HCLKIN Rising	2.0	10.0	3	0 pf
t41	TIO [10:0] Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pf
t42	TIO[10:0] Setup time to HCLKIN Rising	3.0		4	
t43	TIO[10:0] Hold time from HCLKIN Rising	2.0		4	
t44	TWE# Valid Delay from HCLKIN Rising	2.0	10.0	3	0 pf
t45	GWE# Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pf
t45a	BWE# Valid Delay from HCLKIN Rising	2.0	9.0	3	0 pf
t46	CCS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t47	CADS# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t48	CADV# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf

Table 6. DRAM Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Fig.	Notes
		Min	Max		
t50	RAS[4:0]# Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pf
t51	CAS[7:0]# Valid Delay from HCLKIN Rising	1.5	6.0	3	0 pf
t52	MWE# Valid Delay from HCLKIN Rising	1.5	7.0	3	0 pf
t53	MA[11:2] Valid Delay from HCLKIN Rising (Read Row Addr)	2.0	9.0	3	0 pf
t54	MAA/B[1:0] Valid Delay from HCLKIN Rising (Read Col Addr burst cycles)	2.0	7.0	3	0 pf
t55	MA[11:2], MAA/B[1:0] Flow Through Delay from HCLKIN Rising (Read Col Addr leadoff)	2.0	8.0	6	0 pF
t56	MA[11:2], MAA/B[1:0] Valid Delay from HCLKIN Rising for a Write Cycle	2.0	10.0	3	0 pF
t57	MD[63:0] Setup Time to HCLKIN Rising	0			
t58	MD[63:0] Setup Time to HCLKIN Rising for ECC cycles	11.0			
t59	MD[63:0], MPD[7:0] Hold Time from HCLKIN Rising	4.0			
t60	MD[63:0], MPD[7:0] Valid Delay from HCLKIN Rising	2.0	8.0		0 pF
t61	MPD[7:0] Setup Time to HCLKIN RISING	0			
t62	MPD[7:0] Setup Time to HCLKIN Rising for ECC cycles	11.0			

Table 7. PCI Clock Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figure	Notes
		Min	Max		
t70	PCLKIN High Time	12.0		1	
t71	PCLKIN Low Time	12.0		1	
t72	PCLKIN Rise Time		3.0	1	
t73	PCLKIN Fall Time		3.0	1	

Table 8. PCI Interface Timing; 66 MHz (82439HX)
Functional Operating Range (VDD = 5 V ± 5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	66 MHz		Figures	Notes
		Min	Max		
t74	AD[31:0] Valid Delay from PCLKIN Rising	2	11	3	Min: 0 pF Max: 50 pF
t75	AD[31:0] Setup Time to PCLKIN Rising	7		4	
t76	AD[31:0] Hold Time from PCLKIN	0		4	
t77	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Valid Delay from PCLKIN Rising	2	11	3	Min: 0 pF Max: 50 pF
t78	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Output Enable Delay from PCLKIN Rising	2		8	
t79	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Float Delay from PCLKIN Rising	2	28	5	
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Setup Time to PCLKIN Rising	7		4	
t81	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Hold Time from PCLKIN Rising	0		4	
t82	PHLDA# Valid Delay from PCLKIN Rising	2	9.0	3	Min: 0 pF Max: 50 pF
t83	PHLD# Setup Time to PCLKIN Rising	12		4	
t84	PHLD# Hold Time from PCLKIN Rising	0		4	
t85	GNT[3:0] # Valid Delay from PCLKIN Rising	2	9.0	3	Min: 0 pF Max: 50 pF
t86	REQ[3:0]# Setup Time to PCLKIN Rising	12		4	
t87	REQ[3:0]# Hold Time from PCLKIN Rising	0		4	
t88	RST# Low Pulse Width	1 ms		7	

1.5 82439HX System Controller (TXC) Timing Diagrams

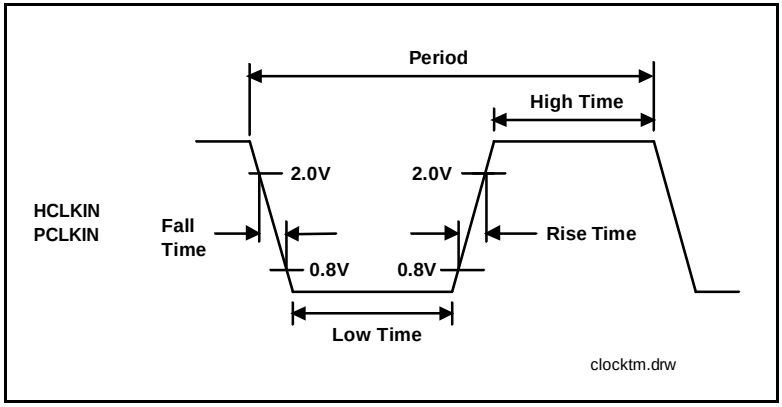

Figure 1. Clock Timing

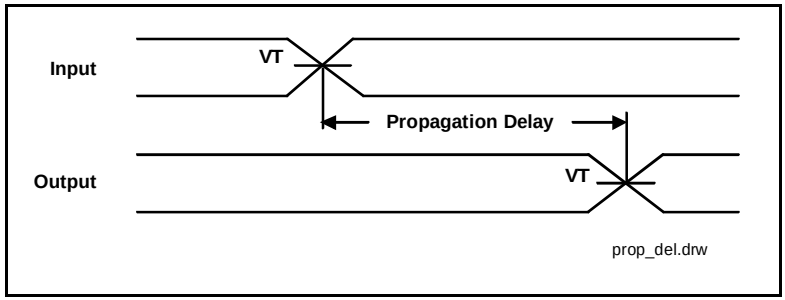

Figure 2. Propagation Delay

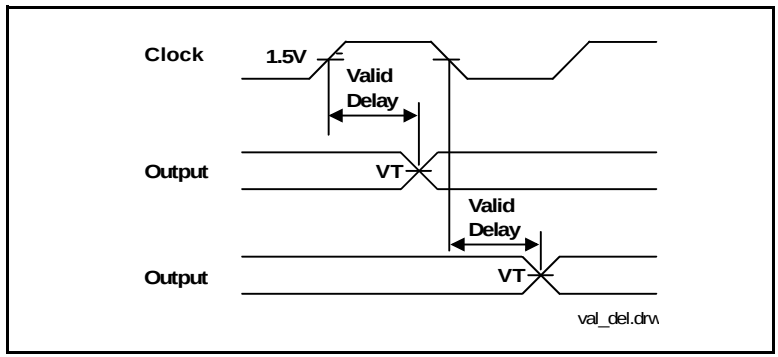

Figure 3. Valid Delay From Rising Clock Edge

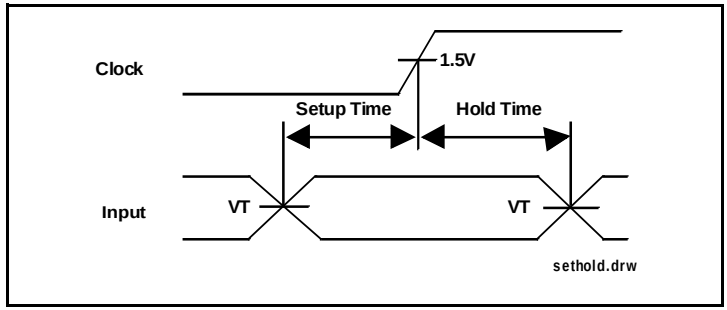

Figure 4. Setup and Hold Times

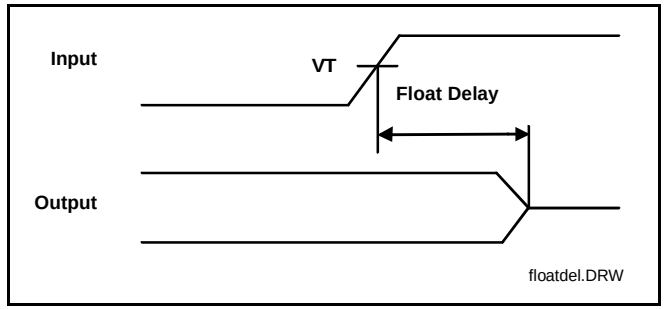

Figure 5. Float Delay

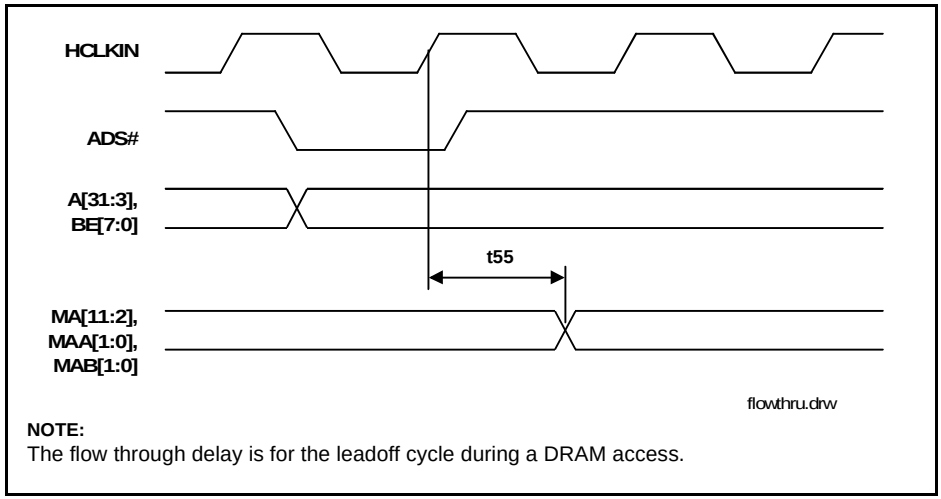

Figure 6. Flow Through Delay

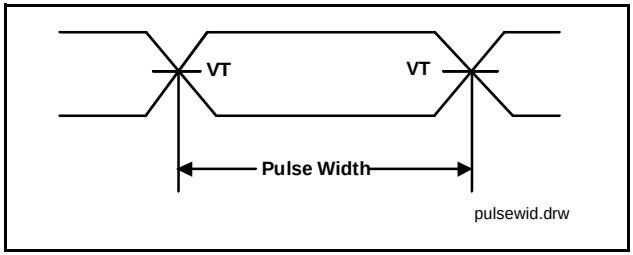

Figure 7. Pulse Width

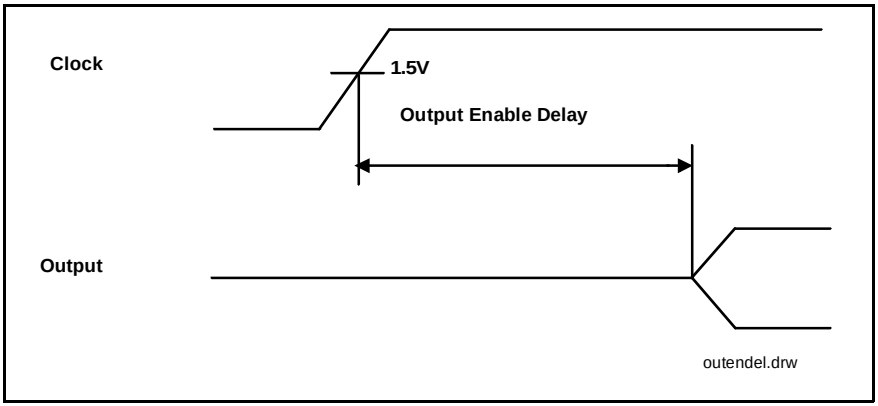

Figure 8. Output Enable Delay