AP-741

APPLICATION NOTE

Designing an Embedded System Using the Pentium® Processor with Voltage Reduction Technology (VRT) and the Intel 430HX PCIset

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November 1996

Order Number: 272967-001

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TABLES

1.0 Introduction

Designs that use the low power features of the Pentium® processors with Voltage Reduction Technology (VRT) can also take advantage of the high performance capabilities of the Intel 430HX PCIsets. This application note describes the differences between the Pentium processor with VRT and the 3.3 V Pentium processor and discusses some of the design considerations in using the Pentium processor with VRT with the Intel 430HX PCIset.

This application note should be used in conjunction with the Pentium processor documents listed in "Related Information" on page 7.

2.0 Voltage Reduction Technology (VRT)

The greatest challenge in developing systems based on new low power processor architectures is maintaining efficient thermal energy management. Since low power systems do not usually contain a cooling fan for internal components, heat is dissipated using innovative thermodynamic design techniques such as heat pipes and thermal sensors, and by using the mobile system chassis to vent heat externally. Proper thermal design is critical to ensuring the reliability of low power systems. Components that run too hot will be more likely to fail during normal use and may reduce the life of the system.

To help solve thermal issues, Intel developed Voltage Reduction Technology, which is integrated into new versions of the 75-, 90-, 100-, 120-, 133- and 150-MHz Pentium processors. The external pins of the Pentium processor with VRT remain powered at 3.3 Volts, which allows the processor to communicate with existing 3.3 Volt components in the system. The internal core of the processor operates at 2.9/3.1 Volts, resulting in up to a 40 percent power savings over its desktop counterpart. Consequently, the 150 MHz Pentium processor delivers over 60 percent faster performance than the 3.3 Volt 75 MHz version while retaining long battery life.

The Pentium processor with VRT is offered in the Tape Carrier Package (TCP) and the Staggered Pin Grid Array (SPGA) package. In this document, only the features of the SPGA package are discussed.

The architecture and internal features of the Pentium processor with VRT are identical to those of the desktop version of the Pentium processor, as described in the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors*, except some features which will be discussed later.

3.0 Intel 430HX PCIset

The Intel 430HX PCIset consists of the 82439HX System Controller (TXC) and the 82371SB PCI ISA IDE Xcelerator (PIIX3). The TXC is a single-chip host-to-PCI bridge and provides the second level cache control and DRAM control functions. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory is implemented with synchronous pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM is used for the cache line status bits. The TXC provides a 64/72-bit data path to main memory and memory sizes up to 512 Mbytes. The DRAM controller provides eight rows and optional DRAM error detection/correction or parity. The TXC's optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, The TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC contains read prefetch and posted write buffers.

4.0 Differences Between the SPGA Pentium® Processor with Voltage Reduction Technology and the 3.3 V Pentium Processor

All specifications for the SPGA Pentium processor with VRT are identical to those of the 3.3 V Pentium processor, except for the differences described in this section.

4.1 Features Removed

The following features have been removed for the Pentium processor with VRT: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins on the 3.3 V Pentium processor that have been removed on the Pentium processor with VRT.

Table 1. Signals Removed from the Pentium® Processor with Voltage Reduction Technology

Signal	Type†	Function
ADSC#	O	Additional Address Status. This signal is mainly used for large or stand-alone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	I	Additional Burst Ready. This signal is mainly used for large or stand-alone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	I	CPU Type. This signal is used for dual processing systems.
D/P#	O	Dual/Primary processor identification. This signal is used only for an upgrade processor.
FRCMC#	I	Functional Redundancy Checking. This signal is used only for error detection via processor redundancy, and requires two Pentium® processors (master/checker).
PBGNT#	I/O	Private Bus Grant. This signal is used only for dual processing systems.
PBREQ#	I/O	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	I/O	Private Hit. This signal is used only for dual processing systems.
PHITM#	I/O	Private Modified Hit. This signal is used only for dual processing systems.
PICCLK	I	APIC Clock. This signal is the APIC interrupt controller serial data bus clock.
PICD0 [DPEN#]	I/O	APIC's Programmable Interrupt Controller Data line 0. PICD0 shares a pin with DPEN# (Dual Processing Enable).
PICD1 [APICEN]	I/O	APIC's Programmable Interrupt Controller Data line 1. PICD1 shares a pin with APICEN (APIC Enable upon RESET).

†The pins are classified as Input or Output based on their function in Master Mode.

4.2 Maximum Rating

The following values are stress ratings only. Functional operation at the maximum rating is neither implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the SPGA Pentium processor with VRT contains protective circuitry to resist damage from static electric discharge, precautions should be taken to avoid high static voltages or electric fields.

WARNING:

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 2. SPGA Absolute Maximum Ratings

Parameter	Value	Notes
Case temperature under bias	-65^{o}C to 110^{o}C	
Storage Temperature	-65^{o}C to 150^{o}C	
3.3 V Supply voltage with respect to V_{SS}	-0.5 V to +4.6 V	
3.1 V Supply voltage with respect to V_{SS}	-0.5 V to +4.1 V	
3.3 V Only Buffer DC Input Voltage	-0.5 V to V_{CC3} + 0.5 V	Not to exceed 4.6 V (1)
5 V Safe Buffer DC Input Voltage	-0.5 V to +6.5 V	(2)(3)

NOTES:

1. Applies to all SPGA Pentium processor with VRT inputs except CLK.
2. Applies to CLK.
3. See Table 4.

4.3 DC Specifications

Tables 3, 4, and 5 list the DC specifications that apply to the SPGA Pentium processor with VRT. The SPGA Pentium processor with VRT core operates at 3.1 V internally while the I/O interface operates at 3.3 V. The CLK input may be at 3.3 V or 5 V. Since the 3.3 V (5 V safe) input levels defined in Table 4 are the same as 5 V TTL levels, the CLK input is compatible with existing 5 V clock drivers. The power dissipation specification in Table 6 is provided for the design of thermal solutions during operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

Table 3. SPGA 3.3 V DC Specifications
T_{CASE} = 0 to 85°C; V_{CC2} = 3.1 V ± 165 mV; V_{CC3} = 3.3 V ± 165 mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	-0.3	0.8	V	TTL Level (1)
V_{IH3}	Input High Voltage	2.0	V_{CC3} + 0.3	V	TTL Level (1)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1)(2)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (1)(3)
I_{CC2}	Power Supply Current from 3.1 V core supply		2500 2775	mA mA	@120 MHz (4) @133 MHz (4)
I_{CC3}	Power Supply Current from 3.3 V I/O buffer supply		320 355	mA mA	@120 MHz (4) @133 MHz (4)

NOTES:

1. 3.3 V TTL level apply to all signals except CLK.
2. Parameter measured at 4 mA.
3. Parameter measured at 3 mA.
4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and V_{CC2} = 3.1 V ± 165 mV and V_{CC3} = 3.3 V ±165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes.

Table 4. 3.3 V (5 V safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	-0.3	0.8	V	TTL Level (1)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTE:

1. Applies to CLK only.

Table 5. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(1)
C_O	Output Capacitance		20	pF	(1)
$C_{I/O}$	I/O Capacitance		25	pF	(1)
C_{CLK}	CLK Input Capacitance		15	pF	(1)
C_{TIN}	Test Input Capacitance		15	pF	(1)
C_{TOUT}	Test Output Capacitance		20	pF	(1)
C_{TCK}	Test Clock Capacitance		15	pF	(1)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (2)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (2)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4 V (3)
I_{IL}	Input Leakage Current		400	µA	V_{IN} = 0.4 V (4)

NOTES:

1. Guaranteed by design.
2. This parameter is for input without pull up or pull down.
3. This parameter is for input with pull down.
4. This parameter is for input with pull up.

Table 6. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical(1)	Max(2)	Unit	Notes
Thermal Design Power (Typ)	2.5 - 3.5 3.0 - 4.0	7.1 7.9	Watts Watts	@120 MHz @133 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		1.2 1.3	Watts Watts	@120 MHz (3) @133 MHz (3)
Stop Clock Power Dissipation	0.02	0.05	Watts	(4)

NOTES:

1. This is typical power dissipation in a system. This value is the average value measured in a system using a typical device at V_{CC2} = 3.1 V and V_{CC3} = 3.3 V running typical applications. This value is highly dependent upon a specific system configuration.
2. Systems must be designed to thermally dissipate the maximum thermal design power (typ). It is determined using a worst case instruction mix with V_{CC2} = 3.1 V and V_{CC3} = 3.3 V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

4.4 AC Specifications

The AC specifications of the SPGA Pentium processor with VRT consist of setup times, hold times, and valid delays at 0 pF. All SPGA Pentium processor with VRT AC specifications are valid for V_{CC2} = 3.1 V ±165 mV, and T_{CASE} = 0 to 85°C.

For the AC timing changes for the Pentium processor with VRT (60 MHz and 66 MHz bus operations) refer to the *Pentium® Processor with Voltage Reduction Technology Datasheet.*

4.5 Thermal Specifications

The SPGA Pentium processor with VRT is specified for proper operation when the case temperature T_{CASE} (T_C) is within the specified range of 0°C to 85°C.

4.6 SPGA Package Differences

The SPGA Pentium processor with VRT has a pin array that is mechanically identical to the SPGA version of the 3.3 V Pentium, but some pins are connected differently. Also, there are small differences in the package dimensions. Refer to the *Pentium® Processor with Voltage Reduction Technology Datasheet* for these differences.

4.7 I/O Buffer Models

The I/O buffer models of the Pentium processor with VRT (both TCP and SPGA) differ from that of the 3.3 V Pentium processor. Refer to the *Pentium® Processor with Voltage Reduction Technology Datasheet*. Also, the capacitance (Cp) and inductance (Lp) parameter values differ between the two packages (TCP and SPGA) for the Pentium processor with VRT. For SPGA Pentium processors with VRT values, refer to the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors*.

5.0 Design Considerations

Designing a system that uses the Pentium processor with VRT and the Intel 430HX PCIset is similar to designing a single-processor, 3.3 V Pentium processor-based system, but without using the Advanced Programmable Interrupt Controller (APIC). The considerations for designing with the Pentium processor with VRT and the Intel 430HX PCIset are described below.

5.1 Power and Ground

For clean on-chip power distribution, the SPGA Pentium processor with VRT has 25 V_{CC2} (3.1 V power), 28 V_{CC3} (3.3 V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be must made to all external V_{CC2}, V_{CC3} and V_{SS} pins of the SPGA Pentium processor with VRT. On the circuit board all V_{CC2} pins must be connected to a 3.1 V V_{CC2} plane (or island) and all V_{CC3} pins must be connected to a 3.3 V V_{CC3} plane. All V_{SS} pins must be connected to a V_{SS} plane.

5.2 Power Sequencing

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, for compatibility with future processors, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both on or both off within one second of each other.

5.3 Decoupling Recommendations

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor. Low inductance capacitors and interconnects are recommended for best high frequency and electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the 3.3 V plane and the 3.1 V plane (or island). Capacitor values should be chosen to ensure that they eliminate both low and high frequency noise components. Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction,

causing the processor to enter the Auto HALT Powerdown state. Such occurrences may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 µF to 100 µF range are required to maintain a regulated supply voltage during the interval between when the current load changes and when the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel. These capacitors should be placed near the processor (on the 3.3 V plane and the 3.1 V plane or island) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems Application Note*.

5.4 Connection Specifications

All NC (No Connect) pins must remain unconnected and all RESERVED pins must remain unconnected. For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3} and unused active high inputs should be connected to ground.

6.0 Related Information

Intel offers a variety of information through the World Wide Web at http://www.intel.com.

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