Glossary

GLOSSARY

A

Access hole: A hole or series of holes in successive layers of a multilayer board that provide(s) access to the surface of the land in one or more layers of the board.

All-metal package: A hybrid circuit package made solely of metal, excluding glass or ceramic.

Alternating current resistance: The resistance offered by any circuit to the flow of alternating current.

Alumina: **Aluminum oxide:** Alumina substrates are made of formulations that are primarily alumina.

Ambient: The environment that surrounds a system or component.

Ampere: The unit used for measuring the quantity of an electric current flow. One ampere represents a flow of one coulomb per second.

Annular ring: The portion of a conductive material that completely surrounds a hole.

Anode: The electrode from which the forward current flows within a device.

Application-Specific Integrated Circuit (ASIC): An integrated circuit chip customized for a specific product.

Area array tape-automated bonding: Tape-automated bonding in which edge-located pads and additional pads on the inner surface area of a chip are addressed in the bonding scheme.

ATE: Automated Test Equipment.

A/T QRE: Assembly/Test Quality & Reliability Engineering

Auger: A surface analysis technique for detecting the chemical composition of material.

B

Backside bias: The electrical connection to the backside of the silicon device used to assure proper performance.

Base plane: The plane through the lowest point of the mounting surface of the package, except for packages using stand-offs.

Bipolar: A device in which both majority and minority carriers are present. Bipolar and Metal-Oxide Semiconductor (MOS) are the two most common device types.

BLT: Bondline Thickness-the thickness of adhesive between two adherands.

Body: The main or largest portion of a connector, to which other portions are attached or connected.

Bonding: The joining of two materials; for example, the attachment of wires to an integrated circuit or the mounting of an integrated circuit to a substrate.

Bonding pads: Areas of metallization on the integrated circuit die that permit connection of fine wires or circuit elements to the die.

Bond schedule: Bonding machine set-up parameters.

Bond window: The acceptable range of each bonding variable, including time, force, power, and temperature.

Bump: A means of providing a connection to the terminal area of a device. A small mound is formed on the device or substrate pads and is used as a contact for facedown bonding.

Bump contacts: Contacting pads that rise substantially above the surface level of the chip.

Bump tape: A tape used in the tape-automated bonding process whose innerlead bond sites have been formed into raised metal bumps, thus eliminating the need for bumps on the chip itself.

Bumped wafer: A semiconductor wafer which has undergone wafer bumping, an electroplating process, to form gold “bumps” over the bond pad metallization. These pumps are welded to the gold-plated copper leads of the TAB tape during innerlead bond to form the interconnections to the chip.

Buried via: A via hole not extending to the surface.

Burn-in: The process of screening out marginal component parts by exposing them to elevated temperatures and voltage stress.

Butt lead: A lead count of surface mount devices in which pin tips contact the PC board.

C

Carrier: A frame which holds individual sites of TAB tape for handling and testing.

Ceramic: Inorganic, nonmetallic, clay, or glasslike material whose final characteristics are produced by subjection to high temperatures.

Ceramic Quad Flatpack (CQFP): An aluminum ceramic integrated circuit package with four sets of leads extending from the sides and parallel to the base.

CERDIP: A dual in-line package composed of a ceramic header and lid, a stamped metal lead frame, and frit glass to secure the structure.

Cerpack: A flatpack composed of a ceramic base and lid, a stamped metal lead frame, and frit glass to secure the structure.

Cerquad: A ceramic equivalent of plastic leaded chip carriers, consisting of a glass-sealed ceramic package with J-leads and ultraviolet window capability.

Chip: The individual circuit or component of a silicon wafer, also known as a die.

Chip attach: Creating an attachment of the backside of the chip to the PCB through an adhesive medium, for Intel chips the medium must be electrically and thermally conductive.

Chip carrier: An integrated circuit package, usually square, with a chip cavity in the center. Its connections are normally on all four sides.

Circuit: The interconnection of a number of components in one or more closed paths to perform a desired electrical or electronic function.

C-mode Scanning Acoustic Microscope (CSAM): An analytical tool for the nondestructive evaluation of microelectronic packages via acoustic waves.

COB: Chip On Board-a board level interconnection whereby the silicon chip is attached directly onto the printed circuit board and interconnections are made from the chip to the board traces/lands using either wire bonds or TAB.

Coefficient of Linear Thermal Expansion (CTE): The change in linear dimension per degree change in temperature, usually expressed as parts per million per degree Celsius.

Complementary Metal-Oxide Semiconductor (CMOS): Logic in which cascaded field-effect transistors of opposite polarity are used to minimize power consumption.

Component: An individual functional element in a physically independent body that cannot be further reduced or divided without destroying its stated function. Examples include resistors, capacitors, diodes, and transistors.

Component lead: The solid or stranded wire or formed conductor that extends from a component and serves as a mechanical or electrical connection, or both.

Component lead hole: A hole used for the attachment and electrical connection of a component termination, including pins and wires, to a PC board.

Conductance: A measure of the ability of a material to conduct an electrical current.

Conductivity, electrical: The capability of a material to carry an electrical current.

Conformal coating: An insulative coating that conforms to the configuration of the object being coated.

Connector: Generally, all devices used to provide rapid connect/disconnect service for electrical cable and wire terminations, board to board.

Convection: A conveying or transference of heat or electricity by moving particles of matter.

D

D/A-Die Attach: The material and process of creating mechanical, and in Intel's case thermal and electrical, connection of the backside of the device to the package-leadframe, ceramic body, or PCB.

Dambar: A portion of the lead frame that prevents mold compound from flowing to the ends of the lead frame.

Design of experiments: A systematic methodology for planning an experiment in order to consider all input and output variables.

DFM: Design For Manufacturability is a process for reviewing designs before they are released to production in order to assure that the product can be run on processes which have high yield and quality.

Dicing: The separation of a semiconductor wafer into individual dies.

Die: The individual semiconductor wafer into individual dies.

Die bonding: The attachment of an integrated circuit chip to a substrate or header.

Die paddle: The central portion of the lead frame, onto which the die and the adhesive are placed during die attach.

Discrete: A term applied to single-element electrical components.

Dual In-line Package (DIP): A component that terminates in two straight, parallel rows of pins or lead wires.

E

EIA: Electronic Industries Association.

EIAJ: Electronic Industries Association of Japan.

Electrode: A conductor through which a current enters or leaves an electrolytic cell.

Electronic packaging: The technical discipline of designing a protective enclosure for an electronic circuit so that it will both survive and perform effectively under a variety of environmental conditions.

Electrostatic Discharge (ESD): The instantaneous transfer of charges accumulated on a non-conductor to a conductor, into ground.

Encapsulate: To seal or cover an element or circuit for mechanical and environmental protection.

Energy-Dispersive X-ray (EDX) analysis: Normally, using electron beam excitation in the scanning electron beam microscope.

ESD: Electrostatic Discharge.

Eutectic: The minimum melting point of a combination of two or more metals.

Excise: The excise operation separates the device area, removes it, and leaves the test pad and sprocket hole portion of the tape in the slide carrier.

External leads: Electronic package conductors for input and output signals, power and ground.

F

Facedown bonding: A method of attaching a component or circuit chip to a substrate by inverting the chip and bonding chip contacts to the mirror-image contact points on the substrate.

Failure mode: Failure at the macro level, i.e., the observed effect of failure.

Farad: A unit of electric capacity.

Flatpack: An integrated circuit package whose leads extend from the sides and are parallel to the base.

Flip-chip: A chip that has bumped termination spaced on the face of the device and is designed for facedown mounting.

Footprint: The area occupied on the substrate by a component or element.

Form Factor: The description of a package with respect to its geometrical size and weight. Small form factor packages take up the smallest possible area on the PCB, are thin to accommodate narrow spacing in card cages, and are as light as possible.

FR-4: Literally "Flame Retardant composition 4," an epoxy resin system used in the manufacture of PCBs.

Frequency: Of an electric current, the number of hertz, or completed alterations per second.

Frit: A relatively low softening point of glass composition.

G

Gate array: A semicustom product, implemented from a fully diffused or ion-implanted semiconductor wafer carrying a matrix of identical primary cells arranged into columns with routing channels between them in x and y direction.

Ground: A common reference point for circuit returns, shielding, or heat sinking.

H

Hermetic: Sealed so that an object is gas-tight, to a specific rate, normally less than 1×10^{-6} cc/sec of helium.

High-Density Plastic Quad Flatpack (HD-PQFP): A package with greater than 196 leads and a pitch of 0.4 mm.

Hot bar reflow: See Reflow.

Hot dip: The process of covering a surface by dipping it into a molten bath of coating material.

Hot gas reflow: See Reflow.

I

ILB: Inner Lead Bond. The method and also the actual interconnection of the TAB tape lead to the silicon device surface. The connection of the gold-plated TAB leads to the gold bump on the chip.

I-lead: A surface mount device lead whose ends contact the board at a 90º angle; also called a butt joint.

Imidization: The reaction comprises acylation of the diamine with dianhydride in a polar solvent to give poly (amic acid), conversion of polyamic acid to polyimide with subsequent loss of small molecules, such as water.

Inductance: The resistance of an electric circuit to any change of current during the building up or decaying of a self-induced magnetic field. This property introduces a delay in current change, with resulting operational delay.

Infrared (IR): Radiant energy that is characterized by wavelengths longer than visible red (0.78 to 100 µm or 0.030 to 3.9 mils).

Input/Output (I/O) terminal: A chip or package connector that interconnects the chip to the package, or one package level to the physically adjacent level in the hierarchy.

Insert: To assemble components, manually or automatically, into a PC board.

Insert cavity: A defined hole in the connector insert into which the contacts are inserted.

Insertion mount: The electrical and mechanical connection of a component to the surface of a conductive pattern utilizing component holes.

Insulators: A class of materials with high resistivity; materials that do not conduct electricity.

Integrated Circuit (IC): A microcircuit consisting of multiple interconnected elements inseparably associated and formed on or within a single substrate to perform an electronic circuit function.

Integrated circuit chip: The active semiconductor element that is the functional part of the integrated circuit.

Intermetallic Compound (IMC): An intermediate phase-homogeneous phase whose composition range does not include any pure metal-in an alloy system that has a narrow range of composition, but has an atomic bonding that can be of several types.

IPA: Isopropyl alcohol.

IPC-SM-780: *Component Packaging and Interconnection with Emphasis on Surface Mounting*, published by the Institute for Interconnection and Packaging Electronic Circuits, a subgroup of the Electronic Industries Association, EIA.

IPC-SM-782: *Surface Mount Design and Land Pattern Standard*, published by the Institute for Interconnection and Packaging Electron Circuits, a subgroup of the Electronic Industries Association, EIA.

J

JEDEC: Joint Electronic Device Engineering Council.

J-lead: A surface mount device whose leads are formed into a “J” pattern, folding under the device body.

K

Keeper Bar: A strip of polyimide carrier ring used to maintain coplanarity during fluxing and placement. The keeper bar is a narrow strip of the carrier tape which is cut during the trim operation and remains in place on each row of leads after excise.

Kirkendall voiding: The formation of voids as a result of a disproportional diffusion rate between two neighboring materials.

Kovar: An alloy of 53% iron, 17% cobalt, 29% nickel, and trace elements, with a thermal expansion matching alumina ceramics and sealing glasses.

L

Laminate: A product made by bonding two or more layers together, usually of different materials, under heat and pressure to form a single structure.

Land Pattern: Also called footprint or Pad, define the site where components are to be soldered to a PC board.

Large-Scale Integration (LSI): Usually, monolithic digital integrated circuits with a complexity of 100 or more gates or gate-equivalent circuits.

Laser bonding: Effecting a metal-to-metal bond of two conductors by welding the two materials together with a laser beam as a heat source.

Laser reflow: See Reflow.

Lead: A conductive path, usually self-supporting; the portion of an electrical component that connects it to the outside world.

Lead (Pb): A soft, heavy metal used in solder compositions and other alloys.

Leaded chip carrier: A plastic or ceramic chip carrier with compliant leads for termination.

Leaded surface mounting: The surface mounting of components to a substrate by means of component leads and solder joints.

Lead frame: The metallic portion of the device package that completes the electrical connection path from the die or dies and from ancillary hybrid circuit elements to the outside world.

Leadless Chip Carrier (LCC): An integrated circuit package that allows surface mounting of components directly into the substrate by means of solder joints.

Lead Wires: Wire conductors used for intraconnections requiring fine wires or for interconnections that include input/output.

LFM: Linear Feet per Minute, a measure of air flow velocity.

M

Marking: A method of identifying packages with part numbers, manufacturer code, and other information.

Mobile dislocations: Atomic line defects in polycrystalline material.

Modulus of elasticity: The ratio of stress to strain in an elastic material.

Moisture Barrier Bag (MBB): A strong, three-ply bag that is Electrostatic Discharge (ESD)-safe and allows minimal moisture transmission. The bag is intended to protect enclosed devices from moisture exposure and should not be opened till the devices are ready for board mounting.

Mounting hole: A hole used for the mechanical mounting of a PC board or for the mechanical attachment of components to the board.

Multilayer Molded package (MM): A PQFP with enhanced performance achieved by a pair of power and ground planes. These planes significantly reduce the power-ground capacitance, making the package ideal for high-speed device operation.

O

Ohm: A unit of electrical resistance.

OLB: Outer Lead Bond. The method and also the actual interconnection of the TAB tape lead to the substrate (PCB) surface.

P

Package: An enclosure for a single element, integrated circuit, or hybrid circuit. It provides hermetic or nonhermetic protection, determines the form factor, and serves as the first-level interconnection externally for the device by means of package terminals.

Pad: The metallized area on a substrate or on the face of an integrated circuit used for making electrical connections.

PCB: Printed Circuit Board.

Piezoresistive elements: Pressure-sensitive resistors.

Pin Grid Array (PGA): A square package with pins covering the entire bottom surface at a pitch of 0.1 in. or 0.05 in., perpendicular to the plane of the package.

Pitch: The nominal distance from center to center of adjacent conductors.

Plastic Leaded Chip Carrier (PLCC): A package with J-leads on all sides.

Plating: Metallic deposit on a surface, formed either chemically or electrochemically.

Polyimide, PI: A thermoset polymer which has high temperature stability. In this usage, the polymer support ring of the TAB tape.

PPE: Plastic Package Engineering.

PQFP: Plastic Quad Flatpack.

Printed circuit board: A board with printed-on components as well as point-to-point connections.

PRS: Pattern Recognition System-computerized video method of location objects and often, of controlling motion.

PSMC: Plastic Surface Mount Component.

Q

Quad Flatpacks (QFPs): A generic term for surface mount technology flat packages with leads on all four sides; commonly used to describe chip carrier-like devices with gull-wing formed leads. The lead pitch for QFPs is in metric. The packages have no corner bumpers.

R

Real estate: The surface area of an integrated circuit or substrate.

Reflow: The process of creating the solder interconnection from the component to the land pattern on the PCB. The component leads and the solder on the land pattern are heated above the melting point of the solder, the solder coats both the leads and the lands and resolidifies into a uniform material upon the removal of the heat source.

Hot bar — Uses a thermode or heated bar at a temperature greater than the liquidus temperature of the solder. Only the leads and lands are directly exposed to the maximum temperature. This is a component by component process.

Hot gas — A hot gas, usually nitrogen, is the heat source. Only the leads and lands are directly exposed to the maximum temperature. This is a lead by lead process.

Laser — A laser is the heat source. Only the leads and lands are directly exposed to the maximum temperature. This is a lead by lead process.

IR — Infrared Reflow use IR radian energy as heat source. The entire package body is exposed to the maximum thermal profile. This is a mass (entire board at once) process.

VPS	Vapor Phase reflow uses the heat of condensation of a vapor (usually a fluorinert) as the heat source. The entire package body is exposed to the maximum thermal profile. This is a mass (entire board at once) process.
Convection	The heat source is hot air and thermal transfer occurs by thermal convection of heat from the ambient to the PCB. The entire package body is exposed to the maximum thermal profile. This is a mass (entire board at once) process.

Resistance: The property of an electric circuit that determines, for a given current, the rate at which electric current is converted into heat. The power converted can be calculated by multiplying the current squared by the resistance.

Resistivity: The ability of a material to resist the passage of electric current.

Resistor: A device that offers resistance to the flow of electric current in accordance with Ohm's law: R = E/I, where R = resistance, E = voltage, and I = current.

RH: Relative Humidity.

S

Scanning Electron Microscope (SEM): A microscope that makes use of a scanning beam of electrons to image details less than 100 angstroms in size (surface only).

Shrink DIP: A package resembling a DIP, with a lead pitch of 0.07 in., used in applications requiring high mounting densities.

Single In-Line Memory Module (SIMM): A module to which external connection is made by a row of conductors along one side.

Single In-line Package (SIP): A package with leads on a single side only.

Small Outline with J-lead (SOJ): A small outline package with J-leads.

Small Outline Package (SOP): A package with two rows of narrowly spaced gull-wing leads.

SMEMA: Surface Mount Equipment Manufactures Association.

Solderability: The property of a component lead to be wetted by molten solder under specified conditions.

Soldercoat: A process used to apply solder to package leads directly from a molten solder bath.

Specific gravity: The ratio of the weight of a given volume of a substance to the weight of an equal volume of water; also know as relative density.

Surface Mount Technology (SMT): Electrical and mechanical connection of components to the surface of a conductive pattern without using component holes. Components mounted in this manner are known as Surface Mount Devices (SMDs) or Surface Mount Components (SMCs).

T

Tape-Automated Bonding (TAB): A chip interconnect process that can be used as an alternative to wire bonding.

Tensile strength: The greatest longitudinal tensile-strength stress a substance can bear without tearing apart or rupturing.

Terminal: A metallic termination device used for making electrical connections.

Test Pads: Test probe targets located on the periphery of the device tape site external to the OLB area. These test pads are used for electrical test and Burn-in. They are removed during the excise and form operation prior to board mounting.

Thermal expansion: The expansion of a material when subjected to a temperature change.

Thermosonic bonding: The bonding of wires to metal pads on an integrated circuit by means of heat and ultrasonic scrubbing of wire into the pad to create a metallurgical bond.

Through-hole mounting: The electrical connection of components to the surface of a conductive pattern using component holes.

Tin whisker: A hair like, single crystal growth formed on the metal surface.

Thin Small Outline Package (TSOP): A plastic, surface mount memory package that features 0.5 mm pitch gull-wing leads located on two sides of the package.

Traces: The copper interconnections on the PCB.

Transmission Electron Microscope (TEM): A microscope used to obtain high-resolution images with a transmitted electron beam by electron lens imaging rather than scanning.

U

UFPT: Ultra Fine Pitch Technology.

Ultrasonic bond: A bond formed when a wire is pressed against a bonding pad and the pressing mechanism is ultrasonically vibrated at a high frequency above 10 kHz.

V

Vapor phase soldering (reflow): The technique for soldering reflow to form package interconnections. The energy produced by the condensation of an inert vapor is used to heat solder joints.

Vias: The through-holes in the PCB which connect one layer to another or which act as a thermal path from one layer to another.

Visual index: A visible mark, chamber, notch, tab, or depression indicating the position of pin 1, used to determine the orientation of an integrated circuit.

W

Wave soldering: A process in which PC boards are brought in contact with the surface of continuously flowing and circulating solder.

WDX: Wave-length Dispersive X-ray analysis.

Wire bond: A completed wire connection that includes all its constituents and provides electrical continuity between the semiconductor die and a terminal.