6

Component Handling Precaution

CHAPTER 6
COMPONENT HANDLING PRECAUTION

6.1. ESD

6.1.1. Electrostatic Discharge (ESD)

Electrostatic discharge (ESD) costs the electronics industry millions of dollars each year in damaged components, non-functional circuit boards and scrambled or missing information. ESD can occur in the manufacturing, shipping, receiving, and field handling of integrated circuits or computer boards with no visible signs of damage. A malfunction in these components or boards can occur immediately or the apparatus may perform for weeks, months, or even years before an unpredictable and premature breakdown causes a field failure.

6.1.2. Why Should I Care About Electrostatic Discharge?

If you incorporate electronic components or boards into your products, ESD damage can have a direct impact on your company's reputation and profits. That's because electrostatic damage directly affects the quality and reliability of your products. However, for a small investment in time, manpower, and equipment, you can virtually eliminate ESD-caused problems. The tangible benefits to you include:

- Higher manufacturing yields
- Less rework and inventory
- Reduced overall costs
- Fewer field failures and warranty calls
- Increased product reliability
- More repeat business resulting in greater profits

6.1.3. Intel's Commitment to Stamp Out ESD Damage

Because Intel makes and uses electronic components, it has implemented a comprehensive ESD prevention program to ensure that its products are delivered to customers with the highest possible reliability. Our experts would like to share with our suppliers and customers what they have learned about ESD control. Using this information, you can implement similar preventive practices in your factories and warehouses. As a result, all of us can then assure that our products remain free of hidden component failures.

6.1.4. What is ESD?

Technically, ESD is the transfer of electrical charge between two bodies at different potentials, either through direct contact or through an induced electrical field. It is the phenomenon that gives you a mild shock when you walk across a carpeted floor and then touch a doorknob. While this discharge gives a harmless shock to humans, it is lethal to sensitive electronics. For example, the simple act of walking across a vinyl floor can generate up to 12,000V of static electricity. That is many times the charge needed to ruin a standard Shottky TTL component.

There are several technical failure mechanisms associated with ESD damage to microelectronic devices. These failure mechanisms can include gate oxide breakdown, junction spiking, and latch-up.

Gate oxide failures are a breakdown of the dielectric between the transistor gate and channel resulting in excessive leakage or a functional failure.

Junction spiking failures are a migration of the metallization through the source/drain junction of MOS transistors causing leakage or a functional failure.

Latch-up failures can be triggered by ESD, causing an internal feedback mechanism that gives rise to temporary or permanent loss of circuit function.

6.1.5. Common Causes of ESD

Electrostatic generation arising from friction between two materials is called triboelectric charging. It occurs when two materials are separated or rubbed together. Examples include:

- Opening common plastic bag
- Removing adhesive tape from a roll or container
- Walking across a floor
- Transporting computer boards or components around in their trays on carts
- Sliding circuit boards on a work bench

When handling parts or their containers, ungrounded personnel can transfer high static charges. Unless these static charges are slowly dissipated, the ESD event will inflict damage.

Electrical fields are able to penetrate electrical devices. An ungrounded person handling a component or computer board in a non-static shielding container can cause a large charge to be transferred through the container into the sensitive electronic device.

6.1.6. ESD Occurs at All Levels of Integration

Electrostatic discharge is not selective when damaging your products. It can strike components directly or indirectly by passing to the component via connectors and cables. Components mounted on circuit boards are also susceptible.

In-line film resistors between inputs and off-board connectors provide only marginal ESD protection and are often damaged themselves.

6.1.7. What Can I Do To Prevent ESD?

Fortunately, preventing ESD is relatively easy and inexpensive. Two areas of focus are 1) eliminating static charges from the work place, and 2) properly shielding components and assemblies from static fields.

Eliminating static electricity in the work place is accomplished by grounding operators, equipment, and parts (components and computer boards). Grounding prevents static charge buildup and electrostatic potential differences. Electrical field damage is averted by transporting products in special electrostatic shielding packages.

There are many vendors of ESD-protective equipment who are willing to audit your facilities, recommend appropriate procedures and materials, and assist in their implementation. You should consult with such a firm to determine your exact requirements; however, the basic components of a sound ESD prevention program are listed below.

6.1.8. Outfitting An Effective Work Place

An effective work place should be outfitted with the following items:

ESD protective clothing/smocks. Street clothing must not come in contact with components or computer boards since the various materials in clothing can generate high static charges. ESD protective smocks, manufactured with conductive fibers, are recommended.

Electrostatic shielding containers or totes. These containers (bags, boxes, etc.) are made of specially formulated materials which protect sensitive devices during transport and storage.

Antistatic or dissipative carriers. These provide ESD protection during component movement in the manufacturing process. It must be noted that antistatic materials alone will not provide complete protection. They must be used in conjunction with other methods such as totes or electrostatic shielding bags.

Dissipative table mat. The mat should provide a controlled discharge of static voltages and must be grounded. The surface resistance is designed such that sliding a computer board or component across its surface will not generate more than 100V.

Personal grounding. A wrist strap or ESD cuff is kept in constant contact with bare skin and has a cable for attaching it to the ESD ground. The purpose of the wrist strap is to drain off the operator's static charge. The wrist strap cord has a current-limiting resistor for personnel safety. Wrist straps must be tested frequently to assure that they are undamaged and operating correctly. When a wrist strap is impractical, there are special heel straps or shoes which can be used. These items are effective only when used in conjunction with a dissipative floor.

ESD protective floor or mat. The mat must be grounded through a current-limiting resistor. The floor or mat dissipates the static charge of personnel approaching the work bench. Special conductive tile or floor treatment can be used if mats are not practical or cause a safety hazard. Chairs should be conductive or grounded with a drag chain to the flooring.

6.1.9. Summary

Intel uses the full range of electrostatic discharge prevention techniques. We invest in proper employee training, purchase appropriate ESD protection equipment and supplies and adapt our handling and manufacturing procedures for ESD prevention requirements. The same attention to detail is required of all our suppliers, factories, repair centers, and field service staff.

Intel is committed to helping its partners--both suppliers and customers--to manage the ESD problem. If we can be of further assistance in your efforts to eliminate electrostatic discharge damage, please contact the Intel Components Quality Question Line: USA 1-800-628-8686 or 1-916-356-7599, or your local Intel Sales Office.

6.1.10. References

1. Edward S. Yang, “Microelectronic Devices”, McGraw-Hill, 1988.
2. Kohlhass, Phil, “Controlling Potential Static Charge Problems”, 3MNuclear Products Dept., St.Paul, MN.
3. “Electrical Overstress/Electrostatic Discharge Symposium Proceedings”, The EOS/ESD Association and ITT Research Institute, 1985 and 1986.
4. DOD-HNBK-263,Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment”, 2 May, 1980.
5. McFarland, W.Y., “The electronic benefits of an effective electrostatic discharge awareness and control program—an empirical analysis”. 1981 Electrical Overstress/Electrostatic Discharge Symposium Proceedings.

6.2. EOS

6.2.1. Electrical Overstress (EOS)

EOS is the number one cause of damage to IC components. This section describes EOS and how to prevent it.

6.2.2. How EOS Damages a Component

Damage is caused by thermal overstress to a component’s circuitry. The amount of damage caused by EOS depends on the magnitude and duration of electrical transient pulse widths. We can broadly classify the duration of pulse widths into long (>100 μs) and short (<100 μs) types, and magnitude into exceeding an individual component’s EOS threshold. For short pulse widths the most common failure mode is junction spiking.

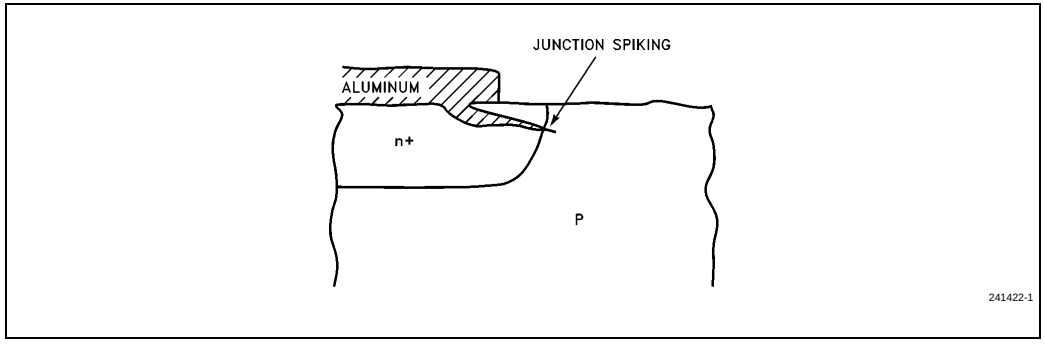

Figure 6-1. Junction Spiking Failure

For long electrical pulse widths the most common failure modes are melted metallization and open bond wires.

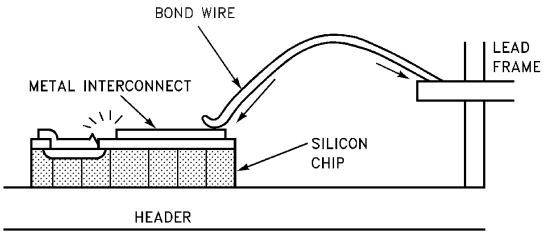

Figure 6-2. Melted Metallization Failure

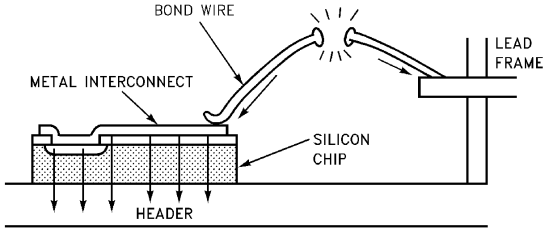

Figure 6-3. Figure 6-3. Open Bond Wire Failure

6.2.3. Common Causes of EOS

Inadequate work procedures:

- Lack of standard work procedures
- Incorrect device orientation
- Insertion/removal of components with power on
- Boards/units not well connected, then power applied

Noisy Production Environments:

- Lack of power line conditioners
- Lack of A.C. line filters

Improper testing at device or board level can create EOS:

- Hot switching effect
- Incorrect test sequence such as application of signals to Device Under Test (DUT) before powering up chip
- Application of excessive voltages to chip beyond spec limits
- Poorly designed electrical stress tests such as burn-in which overstresses sensitive chips

Use of low quality power supplies:

- Poor design considerations can lead to noise sources especially in switching power supplies
- Lack of power supply overvoltage protection circuits
- Insufficient line filtering and/or transient suppression at the input stage of power supplies
- Incorrect selection of fuse providing inadequate protection

Lack of Proper Equipment and Line Monitoring:

- Equipment not grounded
- Loose connections causing intermittent events
- Poor wire maintenance
- AC supply lines not monitored for voltage transients or noise

6.2.4. Prevention of EOS

Establish and follow proper work procedures.

Conduct regular AC supply line monitoring, and if necessary, install EOS line control equipment such as incoming line filtering and transient suppression circuits.

Ensure proper testing of components and boards:

- Check test programs for hot switching and incorrect test sequence.
- Solicit maximum specification ratings from manufacturers to ensure devices are not over-stressed.
- Ensure reliability stress tests are properly designed, especially during burn-in.
- Check for excessive noise levels.
- Use transzorbs to clamp voltage spikes.

Use quality power supplies with the following features:

- Overvoltage protection
- Proper heat dissipation
- Use of fuses at critical locations

Adhere to a strict equipment maintenance program to ensure:

- Equipment is properly grounded
- There are no loose connections

6.2.5. PGA Insertion

6.2.5.1. INTRODUCTION

This section contains a discussion on the insertion mounting of ceramic pin grid array (CPGA) packages into Low Insertion Force (LIF) sockets for Original Equipment Manufacturers (OEMs). Each successive generation of Intel microprocessors has resulted in increased complexity in the structure of the associated CPGA packages. The packages have increased surface area and lead counts while the ceramic thickness has remained relatively unchanged. As the packages get larger and pin count increases, the insertion force needed to seat the packages in LIF sockets increases. Hence, proper insertion mounting procedures are needed to ensure that these packages are correctly mounted in sockets, and that excessive forces have not cracked the package.

6.2.5.2. OVERVIEW

Sockets for PGA packages can be broadly classified into two categories: Zero Insertion Force (ZIF) and Low Insertion Force (LIF) sockets. The ZIF socket designs usually depend on a lever actuated cam mechanism to provide the necessary retention force. The socket has two positions—actuated or unactuated—depending on the position of the lever mechanism (some variations of the ZIF sockets; i.e., the Tool Actuated ZIFs (TAZ) use a tool instead of a lever to switch between the two positions). The user inserts the PGA package into the socket when it is unactuated and it takes a minimal amount of force to seat the package. Once the package is in place, the lever is actuated and a cam mechanism provides the necessary force on the pins to hold the package in place. This socket type has been used in test/burn-in applications and for end user applications for upgrade products. Traditionally, the drawbacks of this package type have been the additional real estate on the board, (mostly) higher socket cost and the occasional applications where the movement of the lever may be obstructed by the heat sink design.

The second category is the LIF sockets which are primarily used in OEM applications. There are two main variations of this socket type i.e. the stamped and formed sockets (sometimes referred to as the true LIF sockets) and the screw machined sockets. The difference between the two categories is that in the stamped and formed sockets, a single contact piece (clip) is embedded in the plastic socket housing as compared to the screw machined types where the

contact piece is a two part assembly, with an inner clip contained in an outer contact shell that is embedded in the plastic socket housing. LIF sockets depend on a friction contact between the clip and the pin to retain the package in the socket. During insertion, as the pin progresses in the socket well, it is required to push open the contact piece. As a consequence, some force is required to completely insert the package in the socket. Different manufacturers have different contact piece designs, the differences being the contact piece material, the surface finish the contact piece design and the layout of the socket wells. The insertion force depends on a number of interacting factors such as the number of pins in the package, the alignment differences in the package and socket layouts, the contact piece designs and the pin tip designs (Reference 1 contains detailed information on the interacting factors).

The extraction (withdrawal) force needed to unseat the package from the socket is an important consideration during socket selection. Friction contact is used in LIF socket designs to provide the necessary retention force for the package. In the early generations of PGA packages with small pin counts and lower power devices, the friction contact force was usually sufficient to hold the package in the socket during shock and vibration tests. As the pin counts increase and the device power increases, requiring larger heatsinks, the mass of the assembly held by the socket increases. This in turn makes it increasingly difficult to depend on friction contact alone to hold the package/sink assembly during shock and vibration testing. The next step is requiring external mechanical retention (i.e. clips between sink and socket or board) to hold the assembly in place.

6.2.5.3. GENERAL GUIDELINES FOR INSERTION MOUNTING

Platen presses are generally used in production environments to insert the PGA package. Intel provides guidelines for the insertion process in three general categories, insertion tool design, package preparation, and insertion process mechanics. The following guidelines can be understood with reference to Figure 6-4 which shows the insertion process for bare packages and packages with heatspreaders.

1. It is recommended that the packages be checked for alignment with the socket and pin straightness prior to insertion.
2. It is recommended that the platen press should distribute the applied pressure evenly and uniformly over as large an area as possible. This can be done by using a hard rubber coating on the platen which can also alleviate possible unevenness on the contact surface.+
3. It is recommended that the insertion pressure should be applied smoothly. Stutter steps, ratchetting and fast impacts especially at the beginning and end of the insertion process should be avoided.
4. It is recommended that the platen press should have a mechanical stop to control the amount of force applied to the package. The package should not be used as a mechanical stop for the press since this will result in excessive forces that may crack the package.
5. It is recommended that the insertion process should be completed before heatsink attach (in cases where a heatsink is needed). In some cases it is not possible to do insertion prior to heatsink attach. An example is when the heatsink adhesive has to be cured at high

temperature. In these cases it is recommended that the platen account for the surface irregularities of the heatsink and ensure even pressure application.

6.2.5.4. INSERTION/EXTRACTION FORCE MEASUREMENTS

Insertion forces for different PGA packages are measured in ongoing studies at Intel to understand the interaction of factors affecting insertion force. The measurement method can be described with a reference to Figure 6-4 and Figure 6-5. Packages are inserted in PGA sockets using a tension/compression test system and uniform pressure is applied to the package surface. The insertion force (load) is measured along with the platen displacement and plotted as shown in Figure 6-5.

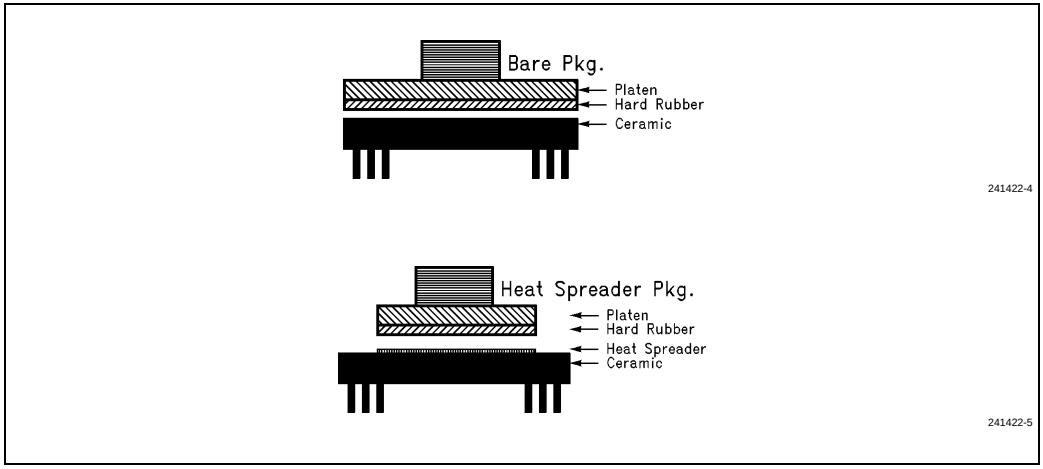

Figure 6-4. Interaction Factors Affecting Insertion Force

Determining the maximum insertion force is an interpretation of the load-displacement graph. Insertion is considered to be complete when the load-displacement curve shows a final distinct change in slope and the load at this point is selected as the maximum insertion force needed. It is determined from the load-displacement profile by extrapolating the final linear portion of the profile. The point where this portion changes slope is chosen as the maximum insertion force.

Average insertion force values, measured for the 296L CPGA package, in different socket types from different vendors vary between 82 lb. to 185 lb. A Finite Element model was used, along with ceramic strength values, to calculate the insertion force that would be needed to initiate cracks in the ceramic body. It was determined that if impacts and stress concentration effects are avoided during the insertion and if the package body is free of initial flaws, forces in excess of 800 lb. would be required to initiate cracking. The measured insertion forces are significantly lower than the forces needed to crack the package ceramic body. Average extraction forces, measured for the 296L CPGA package, show a wide variation (from 93 to 230 lb.) for sockets from different vendors. The extraction forces depend on the contact surfaces and on the spring force exerted by the contact pieces on the pin. The wide variation in extraction forces can be

attributed to the difference in contact piece designs. No correlation has been detected between the insertion and extraction forces.

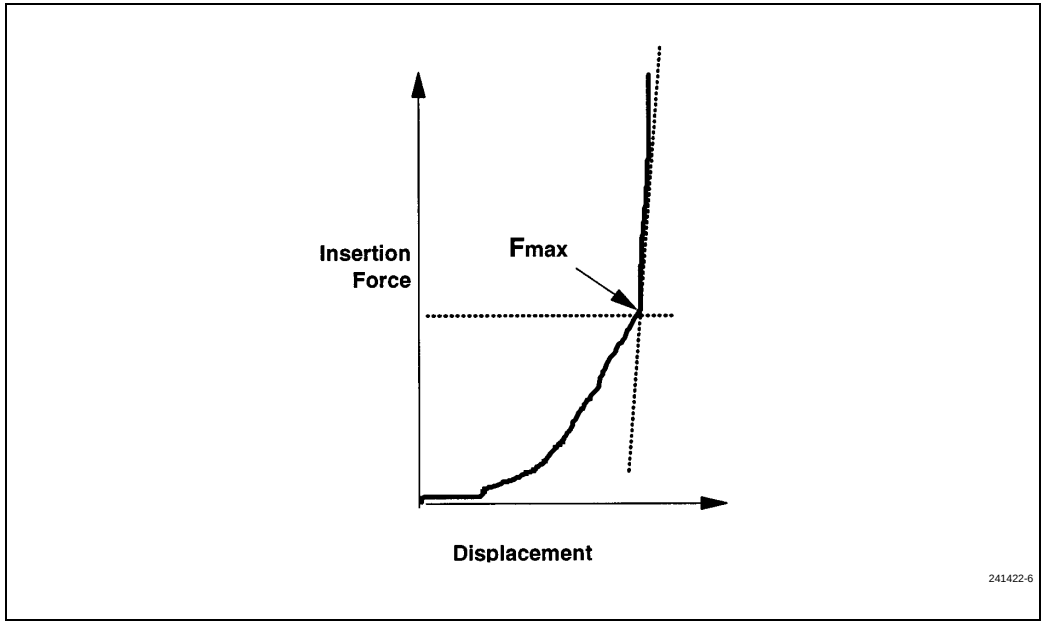

Figure 6-5. Illustration of the Maximum Insertion Force (F_{max}) Determination from the Load-Displacement Curve

6.3. REFERENCE

1. J.B. Cullinane, “Pin Grid Array Socket Total Forces”, Proceedings of the 22nd Annual Connector & Interconnection Technology Symposium, 1989, pp.363-386.

For more information regarding PGA insertion, please request a copy of item # 8130 by calling the Intel FAXBACK line U.S. 1-800-628-2283 or 1-916-356-3105 Europe 44-793-4960646

6.4. REVISION SUMMARY

No Change