14

An Introduction to Plastic Ball Grid Array (PBGA) Packaging

CHAPTER 14
AN INTRODUCTION TO PLASTIC BALL GRID ARRAY (PBGA) PACKAGING

14.1. INTRODUCTION

The plastic ball grid array (PBGA) is today on its way to becoming one of the most popular packaging alternatives for high I/O devices in the industry. Its advantages over other high leadcount (greater than ~208 leads) packages are many. Having no leads, the PBGA has reduced coplanarity problems and minimized handling issues. During reflow the solder balls are self-centering (within limits), thus reducing placement problems during surface mount. Because of the large pad pitch (typically 1.27 mm) the overall package and board assembly yields are better. From a performance perspective, the thermal and electrical characteristics can be better than that of conventional QFPs or PQFPs. The PBGA has a rapid design-to-production cycle time and can also be used in few chip packaging (FCPs) and multi-chip modules (MCMs).

14.2. PACKAGE ATTRIBUTES

Table 14-1 provides a listing of the package attributes for the plastic ball grid array packages.

Table 14-1. PBGA/HL-PBGA Package Attributes

	PBGA			HL-PBGA
Lead Count	208	272	324	352
Sq/Rect.	S	S	S	S
Pitch (mm)	1.27	1.27	1.27	1.27
Package Thickness (mm)	2.13	2.13	2.13	1.54
Weight (gm)	2.34	2.60	2.60	7.03
Max. Footprint (mm)	23.20	27.20	27.20	35.10
UV Erasable				
Shipping Media Tubes Tape & Reel Trays	 X X	 X X	 X X	 X X
Desiccant Pack	X	X	X	X
Comments/Footnotes				Can be thermally enhanced with heatsinks

14.3. PACKAGE MATERIALS

The PBGA package consists of a wire-bonded die on a substrate usually made of a two metal layer copper clad bismaleimide triazine (BT) laminate. Four-metal layer substrate designs often contain additional power and/or ground planes. The die and bonds are protected and encapsulated with molding compound. Via holes drilled through the board provide routing from the lead fingers to the respective eutectic (63/37 Sn/Pb) solder balls on the underside.

The HL-PBGA, however, is configured differently to provide for greater thermal and if required, electrical performance. The thermal advantage provided by this design is based first upon attaching the die to the bottom surface of a heatspeader or slug that also forms the topside of the package. Secondly, because the copper heatspreader forms passes through the package and is exposed on the top of the package, the thermal resistance is extremely low and exposes the package surface to available air flow. If required, this heatslug can be directly coupled to active or passive thermal management devices such as heat sinks or heat pipes.

The electrical performance options made available using the PBGA design can include multiple routing planes for signal and power/ground. These are options that are available but not required to achieve the superior thermal performance of the PBGA package option. See Figure 14-1 and Figure 14-2.

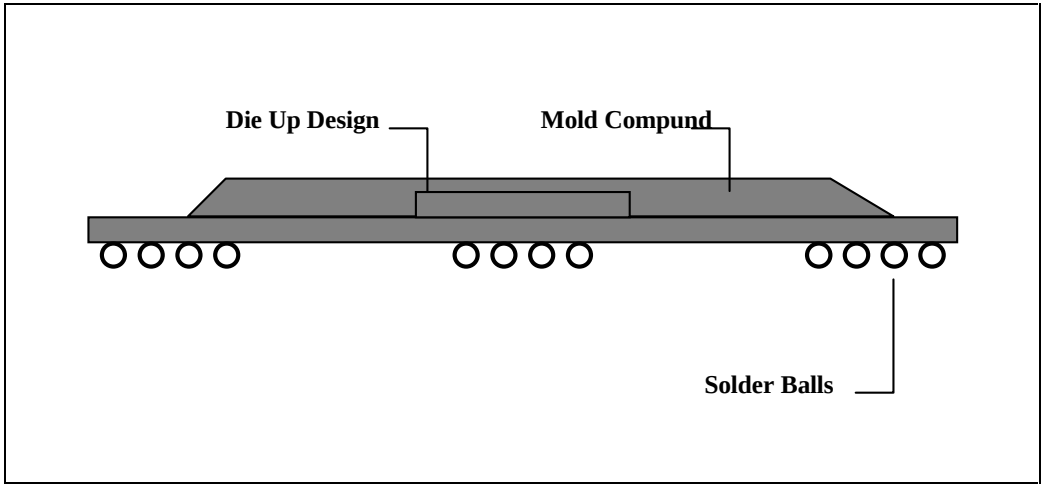

Figure 14-1. PBGA Die Up Cross-Section

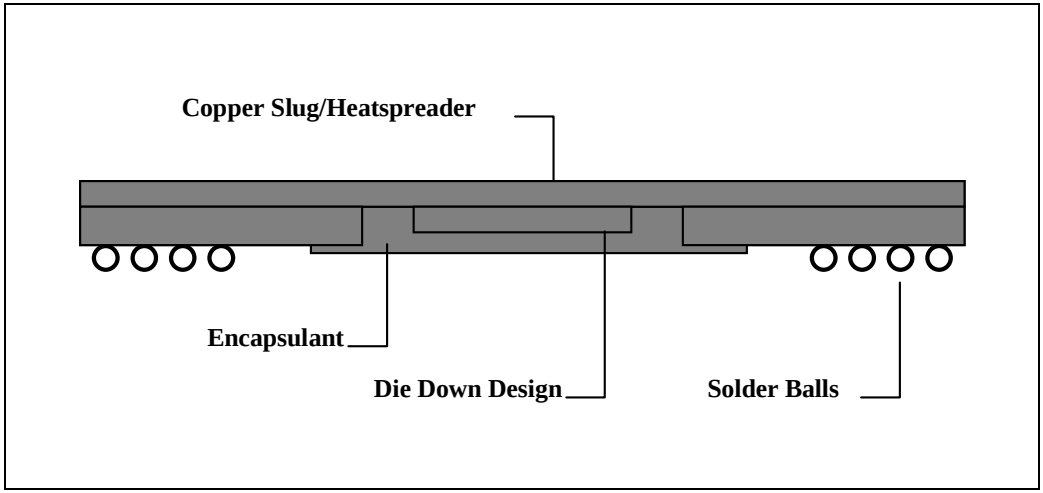

Figure 14-2. HL-PBGA Die Down Cross-Section

14.4. PACKAGE DIMENSIONS

Table 14-2. Symbol List for Plastic Ball Grid Array Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A_1	Stand Off
A_2	Encapsulant Height
b	Ball Diameter
c	Substrate Thickness
D	Package Length
D_1	Encapsulant Length
E	Package Width
E_1	Encapsulant Width
e	Ball Pitch
N	Ball Count (Lead Count)
S_1	Outer Ball Center to Edge of Body

NOTE:

1. Controlling dimensions: Millimeter

Table 14-3. Package Family Attributes

Packaging Family Attributes	
Category	Plastic Ball Grid Array
Acronym	PBGA, HL-PBGA
Ball Counts	PBGA 208, 272, 324. HL-PBGA 352.
Ball Material	Solder
Ball Pitch	1.27 mm
Board Assembly Type	Socket and Surface Mount

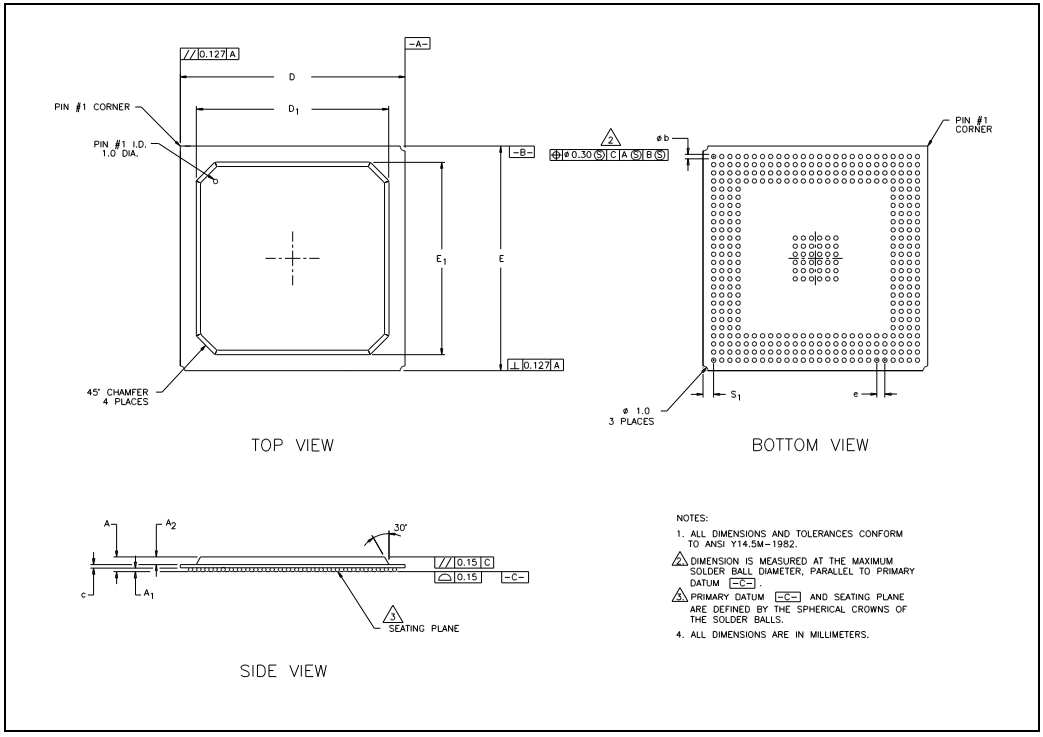

Figure 14-3. PBGA Outline Drawing

Table 14-4. PBGA Package Dimensions

PBGA Packages						
	208 LD		272 LD		324 LD	
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
A	1.94	2.32	1.94	2.32	1.94	2.32
A_1	0.50	0.70	0.50	0.70	0.50	0.70
A_2	1.12	1.22	1.12	1.22	1.12	1.22
b	0.60	0.90	0.60	0.90	0.60	0.90
c	0.32	0.40	0.32	0.40	0.32	0.40
D	22.80	23.20	26.80	27.20	26.80	27.20
D_1	19.25	19.75	23.75	24.25	23.75	24.25
E	22.80	23.20	26.80	27.20	26.80	27.20
E_1	19.25	19.75	23.75	24.25	23.75	24.25
e	1.27		1.27		1.27	
N	208		272		324	
S_1	1.34 REF		1.44 REF		1.44 REF	

NOTE: Measurement in millimeters

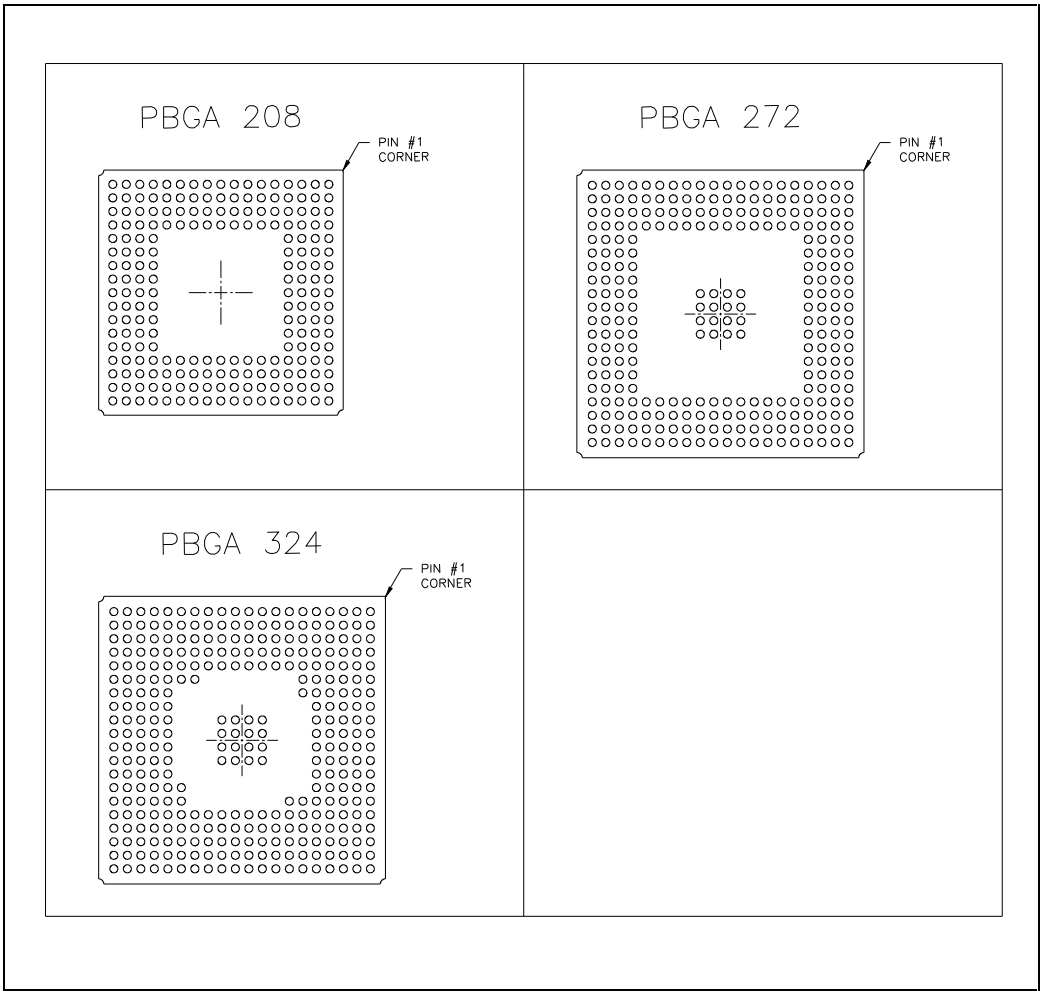

Figure 14-4. PBGA Package Ball Configuration

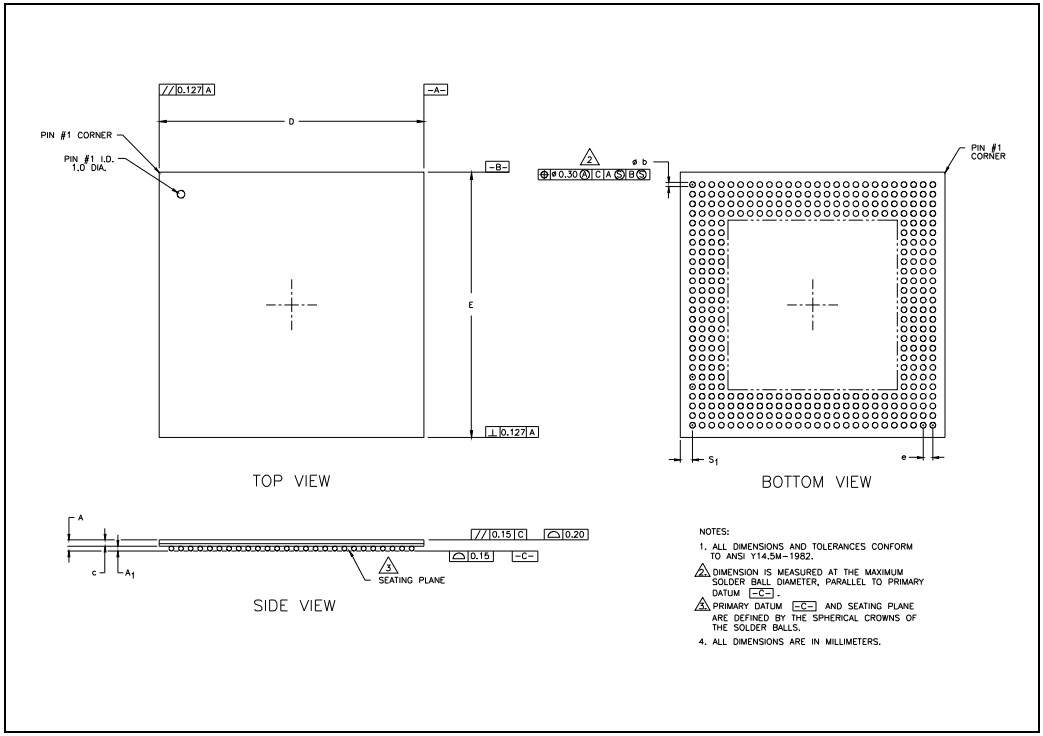

Figure 14-5. HL-PBGA Package Outline and Ball Configuration

Table 14-5. HL-PBGA Dimensions

HL-PBGA Packages		
Symbol	**Min**	**Max**
A	1.41	1.67
A_1	0.56	0.70
b	0.60	0.90
c	0.85	0.97
D	34.90	35.10
E	34.90	35.10
e	1.27	
N	352	
S_1	1.63 REF	

14.5. PACKAGE USAGE

PBGA packaging is used for high-performance applications with high thermal and electrical requirements. PBGAs fit ICs into a smaller footprint, decreasing pitch spacing, by utilizing an array of solder ball connections. This allows for a higher density of I/O connections than that of conventional QFPs or PGAs. The result is a considerably smaller finished package size.

The ball grid array features shorter electrical path lengths which reduce inductance. Mechanical problems such as fragile leads are absent. The larger spacing between solder lands provide adequate tolerances for more reliable surface mounting. Heat dissipation is facilitated through the substrate. These characteristics make the ball grid array package suitable for a wide variety of devices: microprocessors/microcontrollers, ASICs, memory, PC chip sets. A thin profile and reduced footprint also contribute to the PBGAs use in devices in which board space availability is of major concern.

14.6. HANDLING: SHIPPING MEDIA

The PBGA packages are shipped in either a tape and reel or a mid-temperature thin matrix tray that complies to the JEDEC standards. All JEDEC trays have the same ‘x’ and ‘y’ dimensions and are easily stacked for storage and manufacturing. For tray and reel dimensions please refer to Chapter 10 of this manual.

14.6.1. Tape and Reel

The carrier tape is made of conductive polystyrene. It offers exceptional strength and stability over time and temperature variations, while at the same time maintaining flexibility. It has a sheet resistance of 106 ohm/sq. or better. The carrier tape meets the EIAJ standard. The cover tape used is antistatic on both surfaces, transparent and heat sealable. It is engineered to protect and contain surface mount components in embossed semi-conductive PVC or polystyrene carrier tapes. The loaded carrier tapes will be wound onto a plastic reel. The tape and reel packing standards offered by Intel for PBGA packages meet the EIAJ standards, i.e., EIAJ 481-1, 481-2, and 481-3. Mid-temperature Thin Matrix Tray

14.7. PRECONDITIONING AND MOISTURE SENSITIVITY

With most surface mount components, if the units are allowed to absorb moisture beyond a certain point, package damage may occur during the reflow process Chapter 8 provides an in-depth view of package preconditioning and moisture sensitivity requirements. Please refer to Chapter 8 for more information regarding this topic.

Prior to attempting solder reflow, the moisture sensitivity of packages being used by the manufacturer should be understood and proper precautions taken.

14.8. PACKAGE TO BOARD ASSEMBLY

14.8.1. Fluxing

A rosin based mildly activated (RMA), halide free flux, is recommended for use on BGA components. The presence of adequate flux is critical to final yield or reliability. The trend is towards the no clean fluxes, therefore the surface insulation resistance should be monitored.

14.8.2. Solder Paste

The quality of the paste print is an important factor in producing high yield assemblies. The paste is the vehicle to provide the flux necessary to both the PCB and solder ball surfaces to allow soldering. A no-clean or aqueous clean solder paste with 63Pb/37Sn is commonly used in mounting the PBGA. Typically the choice of solder paste determines the profile and reflow parameters. Most paste manufacturers provide a suggested thermal profile for their products and should be referenced prior to manufacturing. Special BGA specific solder pastes are being marketed by paste vendors that exhibit minimized voiding in the solder joint.

14.8.3. Solder Stencils

The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder alloy deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow-solder processing. Stencils are usually made of brass or stainless steel, with stainless steel being more durable. A stencil with a rounded corner, square hole with five degree tapered opening has sometimes been shown to be the best hole design to use for a BGA application. Thickness of the stencils are usually in the 7 to 8 mil (.18 to .20 MM) range. The paste materials tend to dry out when not properly environmentally controlled. A squeegee durometer of 95 or harder should be used. The blade angle and speed must be fine tuned to ensure even paste transfer. An inspection of the stenciled board is recommended before placing parts as proper stencil application is the most important factor with regards to reflow yields further on in the process.

14.8.4. Placement and Alignment

The pick and place accuracy governs the package placement and rotational (theta) alignment. This is equipment/process dependent. Slightly misaligned parts (less than 50% off the pad) will automatically self-align during reflow. Grossly misaligned packages (greater than 50% off pad) should be removed prior to reflow as they may develop electrical shorts, as a result of solder bridges, if they are subjected to reflow.

14.8.5. Solder Reflow

Except for accurate placement of packages, there are no special requirements necessary when reflowing BGA components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple PBGAs on the board, the profile should be checked at the different PBGA locations on the board. Component temperatures may vary because of nearby surrounding components, location of part on the board, and package densities. Temperatures may also be different at the edge of the package than in the center. Chapter 9 provides a more in-depth look at how to manage these types of concerns. Table 14-6 provides specific paramenters to be followed during SMT preheat, preflow, and reflow processes.

14.8.6. PCB Cleaning

Cleaning can be done with aqueous, semi-aqueous, or solvent based systems. With the elimination of CFC containing materials, most companies are moving to a no-clean or aqueous based system. The proper cleaning of solder flux residues and other ionics left on the boards from the assembly process is necessary for long term reliability of the finished product. “NO clean” fluxes simply mean that there is no harmful residues left on the board that will cause any corrosion or damage to the components if left on the board. This residue has sometimes shown to be a collection point for outside contamination on the board surface. An evaluation needs to be done to see if the remaining residue still needs to be removed from the boards in final application.

Table 14-6. PBGA/HL-PBGA Example SMT Reflow

Zones	Characteristic Description	Windows/Limits
Preheat	Initial heating of lead/component Peak temperature	1-3 deg. C/second 100-140 deg.C
Pre-Reflow	Dryout and solder paste activation Soak Time	120 -170 deg. C 120 Seconds
Reflow	Time above 183 deg. C Peak reflow temperature (lead) Peak component body temperature cooling rate	30 - 120 Seconds 205 - 225 deg. C 220 deg. C Maximum 2 -4 deg. C/second

14.8.7. SMT Process

Many factors contribute to a high yielding BGA assembly process. A few of the key focus areas and their contributing factors are highlighted in Table 14-7.

Table 14-7. Essentials for Assembly Quality

Solder paste quality	Uniform viscosity and texture. Free of from foreign material. Solder paste should be used before the expiration date. Shipment and storage temperatures are maintained at the proper temperature. Paste is protected from drying out on the solder stencil.
Mother board quality	Clean, flat, well-plated solder ball land area. Good soldermask coverage.
Placement accuracy	Tight tolerances are not usually required. The BGA can self-center itself as long as a major portion (more than 50%) of the solder ball is in contact with the fluxed solder Paste Land area on the board. Alignment marks (targets) on the PCB are helpful for placing parts.
Moisture Sensitivity Precautions	Know your components moisture sensitivity rating and adhere to IPC/JEDEC moisture control conditions or package delamination or cracking may occur.

14.8.8. Removal and Replacement Process

A removal and replacement procedure for a PBGA package is as follows:

1. Plastic Ball Grid Array Package Removal from Board.
   a. Preheat the board to a minimum temperature of 80°C (max. temperature is 220°C). Any part of the board over 160°C-170°C is close to the solder melting temp of 183°C and risks damaging the joints of other components on the board, especially the bottom side

parts which are closer to the heat source. It is recommended that each customer conducts time and temperature experiments to determine the optimum conditions to minimize board/package warpage. Monitor both top and bottom-side board temperatures.

b. Dispense liquid, no-clean flux between the package and the board.

c. Attach a vacuum pick-up tip onto the package and apply hot air (preheat, ramp time, and temperature to be determined by customer's own experimentation). Note that some cases of mother-board pad lifting problems have been reported possibly due to the machine type used and how much upward tension there is on the vacuum pick-up. This problem may be solved by the customer determining the typical time to release when using the vacuum pick-up, adding 30 seconds and then not applying the vacuum pick-up during removal until this amount of time had passed.

d. Lift the package from the board.

e. Turn off the hot air and carefully remove the board from the heat source and allow to cool to a safe, handling temperature. Inspect the board to determine no damage has occurred to adjacent components or to the board itself.

2. Inspection, Preparation and Replacement of New Package

a. Remove any excess solder from the PBGA solder pads using a solder wick or vacuum.

b. Clean the PBGA solder pads with alcohol and brush. Allow the board to dry and inspect to ensure a clean surface.

c. Preheat the board to a minimum temperature of 80°C (maximum temperature of 220°C). Any part of the board over 160°C-170°C is really close to the solder melting temp of 183°C and risks damaging the joints of other components on the board, especially the bottom side parts which are closer to the heat source. It is advised that each customer conduct temperature experiments to determine optimum conditions to minimize board/package warpage. Monitor both top and bottom-side board temperatures.

d. Use of stenciled solder paste is optional (and as PBGA packages get larger, may be required). For applications where a solder stencil is not possible or not desired, acceptable results may be obtained by only applying flux to the pre-tinned pads. This is done by using a non-metallic spreader and applying a no-clean flux paste to the pads on the board. Be careful not to scratch the pads or the board.

e. Apply liquid flux to the solder balls of the new package. Once the liquid flux is applied, within two minutes, place the package on the board and then reflow (be sure to use the board's alignment features fudicials and then place component using either a mechanical or manual means).

f. Reflow solder balls using hot air directed at the edge and under the package body. It is recommended that temperature experiments be conducted to determine optimum conditions.

g. Remove the board from the heat source and allow to cool to a safe handling temp.

h. Inspect the board and package to verify proper solder ball collapse and observe any defects that may have been caused by the rework procedure.

14.9. PACKAGE PERFORMANCE

14.9.1. Thermal Performance

In general, three factors affect the thermal performance of the PBGA: materials, geometry and environment. Obviously, the more thermally conductive the materials, the better the package dissipates heat. The molding compound that surrounds the chip, providing mechanical protection as well as a surface for marking, is typically 15 to 25 mils in thickness.

In general design-related factors have greater thermal effect on the PBGA than material-related variables. A large die spreads heat easier, as does a larger package size and thus a higher ball count. Substrate design features have tremendous effect on the package's ability to dissipate heat. Vertical vias running through the substrate help to transfer heat from the die down to the solder balls. Four-layer designs often incorporate conductive ground planes, which have a significant, positive effect on thermal performance. The Enhanced PBGA and the HL-PBGA, utilize a heatsink or slug across the top of the package to dissipate heat even more efficiently.

Environmental conditions play a critical role in the thermal performance of PBGAs. Ambient, junction and case temperatures, the device's placement and orientation on a board, in conjunction with the degree of air flowing past the unit present a broad range of possible thermal solutions and problems for IC packaging. Typically a package cannot be capable of handling a given power requirement unless the environmental conditions allow heat to dissipate.

When environmental or geometric constraints limit a PBGA's ability to dissipate heat, a copper or aluminum heatsink is often used to provide a further outlet for heat transfer. As with other types of packages, the heatsinks for PBGAs vary in design and methods of attachment. Most applications recommend a maximum case temperature of 85°C. If the case temperature exceeds 85°C, a heatsink may be required.

14.9.2. Electrical Performance

Generally, due to the fine-laminate base and to the lack of long pins, the electrical performance of PBGA is typically better than the long pinned packages. The shortening of the electrical paths by the solder balls through the plated via-holes to the conducting plane/ground plane reduces electrical parasitics. This can be improved further by optimizing the shortening of the overall trace length. For electrical performance details of the package, please consult the data sheet or call your local Intel sales office.

14.10. REVISION HISTORY

New Chapter