# 13

# An Introduction to Plastic Pin Grid Array (PPGA) Packaging

# CHAPTER 13
# AN INTRODUCTION TO PLASTIC PIN GRID ARRAY (PPGA) PACKAGING

## 13.1. INTRODUCTION

As Intel microprocessors become faster, more complex and more powerful, the demand on package performance increases. The improvements in microprocessor speed and functionality drive the package design improvements in electrical, thermal and mechanical performance. The package electrical and thermal characteristics become attributes of the component performance along with the mechanical protection offered by the package.

To meet these requirements, Intel has introduced a variety of innovative package designs, such as surface mount, small out-line, very thin package, multilayer molded plastic quad flatpacks (PQFP), advanced ceramic pin grid array (CPGA) package, and tape carrier package, (TCP) formats. The development of the plastic pin grid array (PPGA) package has a provided an improvement path for enhanced power distribution and improved thermal and electrical performance. The PPGA components are compatible with those in the CPGA package in form, fit, and function. PPGA meets plastic package reliability requirements.

Table 13-1 summarizes the key attributes of the PPGA package. The following sections detail the physical structure, electrical modeling and performance of the PPGA package.

**Table 13-1. PPGA Package Attributes**

| PPGA Attributes | |
|---|---|
| Physical | |
| Appearance | Circuit board, exposed pins |
| Package Body Material | BT laminate, Ni/Cu slug, encap, Au bond wires |
| Body Thickness | 3.0mm (with heat slug) |
| Weight | 18 gms |
| Package Trace Metal | Copper |
| External Heat Slug | Yes |
| External Capacitors | Yes |
| *Performance* | |
| Thermal ($\theta_{jc}$) with Heat Sink | 0.50 °C/W |
| Power Distribution | Cu traces and multiple planes enhance distribution |
| Package Trace Propagation Delay | Cu traces have low resistance and reduce delay |
| *Others* | |
| Thermal Grease Used for Heat Sink Attachment | Thermally conductive and electrically non-conductive |
| Board Mount | Socket only |

## 13.2. PACKAGE GEOMETRY AND MATERIALS

### 13.2.1. Package Materials

The PPGA package body piece part is a pinned laminated printed circuit board (PCB) structure. Figure 13-1 illustrates the cross section of a typical PPGA piece part The dielectric material, which is chosen for its high temperature stability, is a glass reinforced high glass transition temperature (Tg) Bismaleimide Triazine (BT) with a Tg ranging from 170 °C to 190 °C. Conductors are copper traces. For bondability, the copper (Cu) bond fingers are plated with gold (Au) over nickel (Ni). The heat slug is Ni plated copper, which gives high thermal dissipation. The Kovar pins are plated with Au over Ni, and are surrounded by solder after insertion into the PCB substrate.

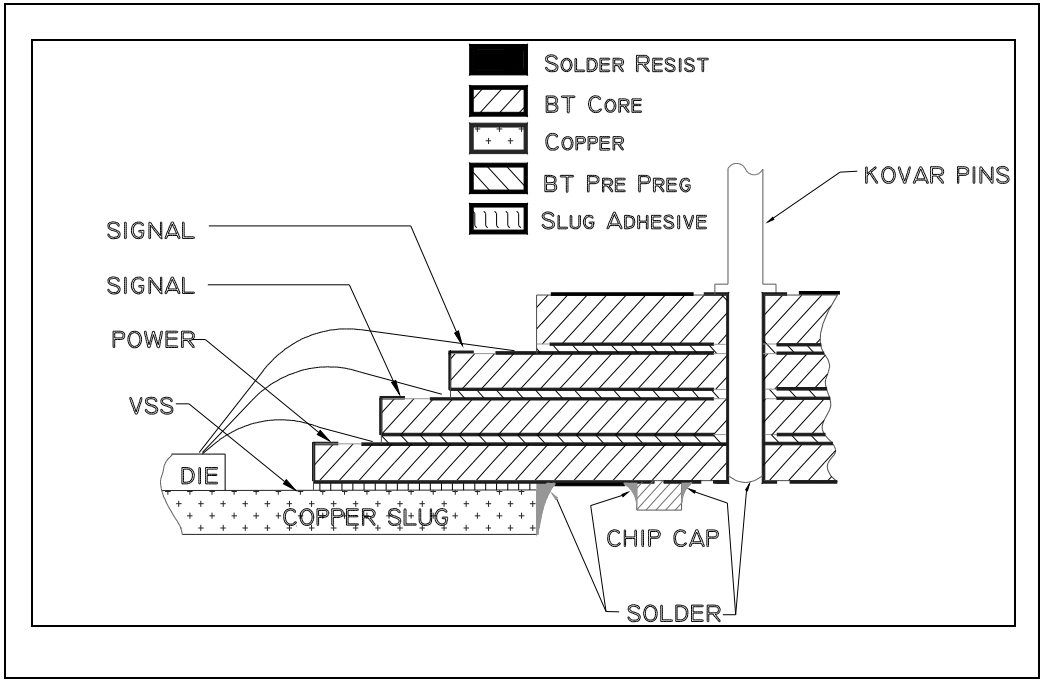



**Figure 13-1. Cross Section View of PPGA Package**

## 13.2.2. Package Outline Drawings

Figure 13-2 is the top view of a PPGA package. Note: It includes a nickel plated copper heatslug and eight discrete capacitors. The capacitors are an optional feature used to decouple the power and ground supplies to enhance performance of the part.

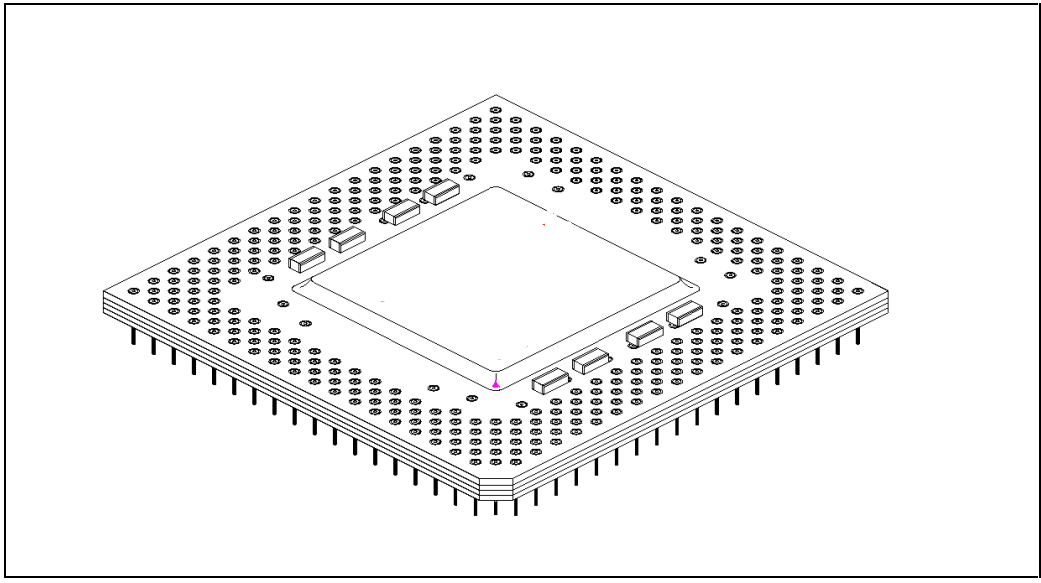


**Figure 13-2. Top View of a PPGA Package**

Figure 13-3 along with Table 13-2 and Table 13-3 illustrate the package outlines drawings and dimensions for the 296 lead PPGA package. The package meets JEDEC Outline spec MO-128 for pin count and package size. The package is square and 1.95 inches on a side and 3 mm in total thickness. The index corner has a 45° chamfer.

**Table 13-2. PPGA Package Drawing Definitions**

| Symbol | Description of Dimensions |
|---|---|
| A | Package Body Thickness Including Heat Slug |
| A1 | Package Body Thickness |
| A2 | Heat Slug Thickness |
| B | Pin Diameter |
| D | Package Body Dimension |
| D1 | Pin Field Width |
| D2 | Heat Slug Width |
| e1 | Pin Pitch |
| F1 | Outer Heat Slug Center to Package Edge |
| F2 | Inner Heat Slug Center to Package Edge |
| L | Pin Length |
| N | Lead Count |
| S1 | Outer Pin Center to Package Edge |

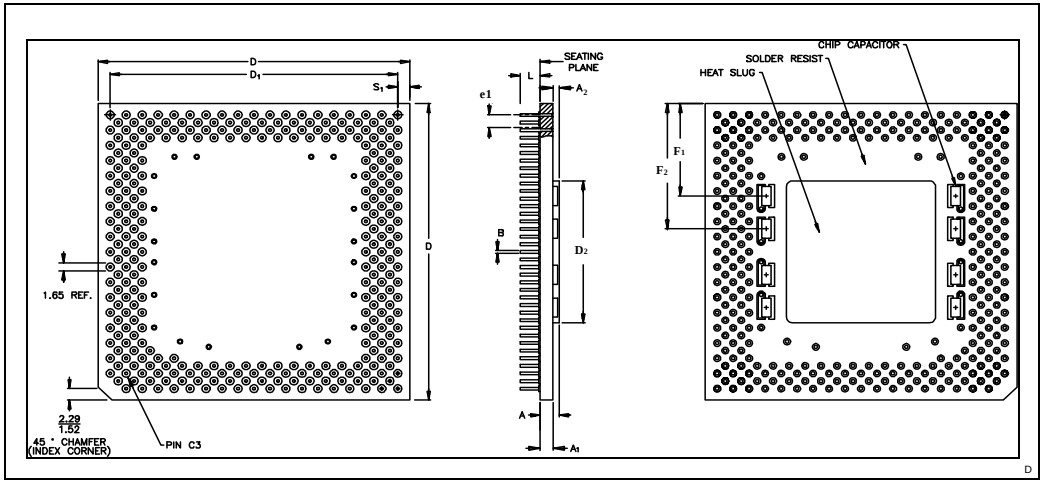



**Figure 13-3. Principal Dimensions**

**Table 13-3. PPGA Package Dimensions and Tolerances**

| Family: Plastic Pin Grid Array Package | | | | |
|---|---|---|---|---|
| **Symbol** | **Millimeters** | | **Inches** | |
| | **Minimum** | **Maximum** | **Minimum** | **Maximum** |
| A | 2.72 | 3.33 | 0.107 | 0.131 |
| A1 | 1.83 | 2.23 | 0.072 | 0.088 |
| A2 | 1.00 | | 0.039 | |
| B | 0.40 | 0.51 | 0.016 | 0.020 |
| D | 49.43 | 49.63 | 1.946 | 1.954 |
| D1 | 45.59 | 45.85 | 1.795 | 1.805 |
| D2 | 23.44 | 23.95 | 0.923 | 0.943 |
| e1 | 2.29 | 2.79 | 0.090 | 0.110 |
| F1 | 17.56 | | 0.692 | |
| F2 | 23.04 | | 0.907 | |
| L | 3.05 | 3.30 | 0.120 | 0.130 |
| N | 296 | | | |
| S1 | 1.52 | 2.54 | 0.060 | 0.100 |

**NOTES:**
1. A2 Typical
2. F1 Typical
3. F2 Typical

## 13.3. APPLICATIONS

The PPGA package has been developed for Intel's advanced microprocessor family of products. It has been designed for use in socketed applications, using socket footprints which are compatible with the Intel ceramic Pin Grid Array package family. The package can be used as as direct replacement for ceramic pin grid arrays (CPGA) in socketed applications.

## 13.4. PPGA COMPONENT ASSEMBLY PROCESS

The PPGA assembly process flow is similar to the CPGA process flow, with the exception of the seal operation.

Wafers are prepared for die attach by being mounted on a pressure sensitive carrier tape and dicing with a high speed saw. The cut wafer is washed with a detergent solution to remove silicon dust prior to the die attach.

A silver filled epoxy adhesive is applied to the package substrate at die attach. A die is picked from the wafer and placed on the adhesive.

The die are connected to the gold plated package leads by way of gold wedge wire bond technology. Bond pad and package lead placement accuracy and wire pull strength monitors ensure high integrity connections.

PPGA packages are encapsulated with silica filled liquid epoxy, in contrast to the CPGA lid seal process. The encapsulant provides mechanical and environmental protection for the die and wires. Process trays are moved beneath a valve which fills the package cavity with epoxy and are transferred to an in-line oven in which the epoxy cures.

A matrix code containing the assembly date code information is marked on the top side of the package using a laser. The mark is inspected for orientation and readability. The packages are then ready for the testing, finishing and packing processes.

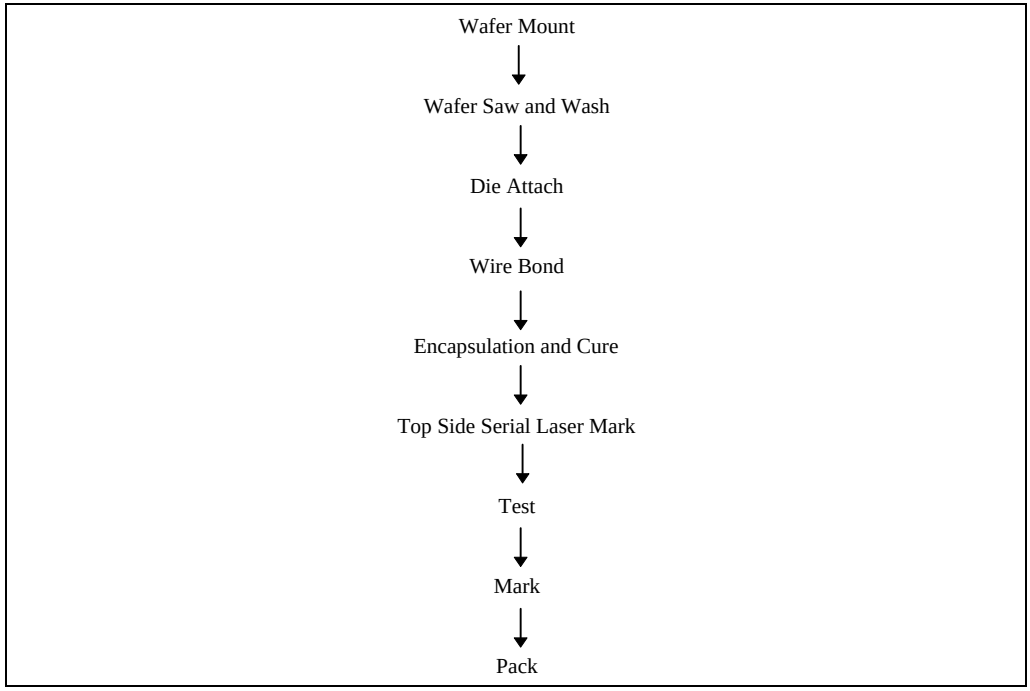



**Figure 13-4. PPGA Generic Process Flow**

## 13.5. PACKAGE USAGE

### 13.5.1. PPGA Package Shipping Media

PPGA shipping trays are compliant to JEDEC standards. All external dimensions of the PPGA tray are the same as the CPGA tray. There is a slight difference in the distance from the top of the tray to the seating plane of the PPGA shipping tray compared to the CPGA shipping tray. The PPGA shipping tray pocket is smaller in the x- and y-axes, also. This slightly smaller pocket dimension reduces package free-play in the tray. Refer to Chapter 10 for the dimensions of the PPGA shipping tray. PPGA's will be shipped in uniquely colored trays separately from CPGAs. This will enable manufacturing personnel to readily identify which package type is being placed into manufacture at any time. This shipping media minimizes foreign material, as well as meets ESD safe shipping requirements.

## 13.5.2. Moisture Sensitivity

PPGA packages have been designed for socketed applications. They are not shipped in moisture barrier bags, nor is floor life exposure time tracking needed for socketed applications. The maximum body temperature which the component should see is 150°C. The component is not intended for either direct through-hole mounting by wave solder processing nor for exposing the entire package body to surface mount-like reflow profiles. Such thermal profiles are not recommended for PPGA packages.

## 13.5.3. Package to Board Assembly

## 13.5.4. Socketing

*Intel recommends that when performing insertion and extraction, the maximum force should not exceed 100lbs, and should be applied uniformly. The insertion and extraction tooling should take into account the clearance for the external capacitors and the heat slug.*

PPGA packages may be used in either low insertion force(LIF) or zero insertion force(ZIF) sockets. The 296 lead sockets are available for PPGA packaged components from many suppliers. The socket design is a standard footprint on the PCB. Insertion and extraction forces were measured on sockets from various vendors. For all LIF socket designs tested, the maximum insertion force required was 80 lbs. Avoid uneven loading during insertion. The applied load overcomes the frictional resistance applied to the package pins as they are inserted in the socket. Table 13-4 summarizes the average measured insertion and extraction force with a selection of different sockets.

**Table 13-4. PPGA Insertion/Extraction Force Measurement**

| Socket* | Average Insertion Force (LB) | Average Extraction Force (LB) |
|---|---|---|
| Preci-Con LIF | 44.69 | 57.43 |
| Mill-Max LIF | 38.09 | 49.65 |
| Robinson Nugent LIF | 78.35 | 73.51 |
| AMP LIF | 65.06 | 69.91 |
| Andon LIF | 54.26 | 58.58 |
| Yamaichi ZIFs | n/a | 80.94** |

**NOTES:**

* This data does not constitute a recommendation for any specific supplier or part number.

** This is measured when the lever is actuated to ensure that the package will not be pulled out during shock and vibration test. When the lever is up, the extraction force is “zero” as expected.

If the manufacturing flow requires inserting the package after the heat sink is applied to the component; the same suggested maximum force of 100lbs may be applied uniformly across the top surface of the heatsink.

## 13.6. HEAT SINK ATTACHMENT

### 13.6.1. Thermal Interface Material

To assure PPGA packages are mechanically compatible with CPGA, Intel has performed a comprehensive evaluation of the effective method of heat sink attachment. Intel suggests that the interface material used for heat sink attachment should have thermal conductivity greater than 0.8 W/mK, and should be electrically insulative. The volume resistivity of the material should be greater than $1x10^6$ Ohm-cm. Intel has demonstrated that Thermalcote I * Conductacoat* with Al foil carrier is an effective interface material for PPGA component heat sink.

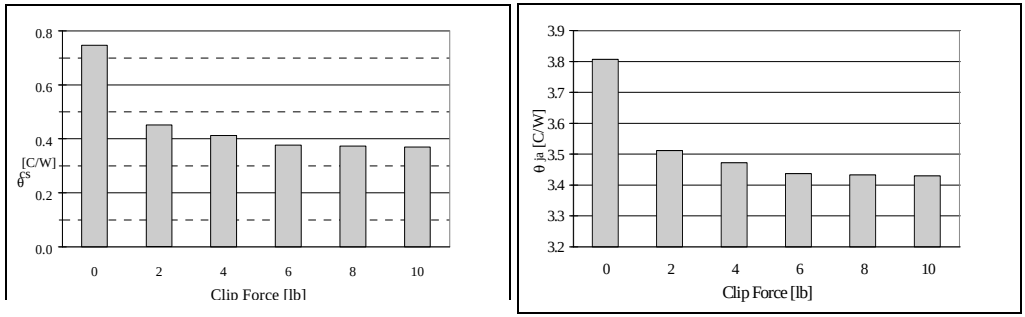
### 13.6.2. Clip Design and Attach

A minimum clip force of five pounds is recommended. Clips retain the heat sink assembly in the socket by exerting a force on the heat sink and the socket. The clip force, in turn, aids in forcing the grease to fill the many microscopic peaks and valleys on the heat sink and package surface, thereby reducing the interface thermal resistance. Since different clip forces result in different amount of grease squeezed out, the corresponding bond lin thickness of the grease will affect thermal performance.

The effect of foil sizes, clip force and voiding on Thermalcote I * Conductacoat* thermal performance was also explored. If there is no grease on the Al foil, voiding will exist in the bond line. This results in higher $\theta_{ja}$ values While up to 30% grease voiding can be tolerated without any impact on PPGA thermal performance, zero voiding is strongly recommended for any heat sink attachment methods.

A larger foil size will cover larger area with grease, but a smaller foil size is preferred for handling. For instance, thermal resistance $\theta_{ja}$ measured with a standard sized foil (1.0” x 1.0”) is 0.1 C/W to 0.2 C/W lower than the $\theta_{ja}$ measure with smaller foil (0.7” x 0.7”). Note that the Aluminum foil is a carrier specific for Thermalcote I * Conductacoat* grease to aid volume manufacturing. The decision to use A1 foils should be based on the OEMs particular heat sink attachment methods and assembly line(s).

Clip force determines the thermal grease bond line thickness and directly impacts thermal performance. To determine the effect of clip force on thermal performance, $\theta_{ja}$ and $\theta_{cs}$ values for the heat sink assemblies were measured at different clip forces. The actual clip forces of these modified clips were individually measured by using a Material Testing System(MTS) before thermal resistance measurement. All clip forces were also verified by using MTS after thermal resistance measurement. Figure 13-5 shows $\theta_{ja}$ and $\theta_{cs}$ values vs. clip force, respectively. If the clip force is higher than five pounds (corresponding to ~ 5 psi), there is no significant effect of clip force on PPGA thermal performance.




**NOTES:**

1. $\theta_{ja}$ = Junction to Ambient
2. $\theta_{cs}$ = Case to Sink Thermal Resistance ($^{o}$C/W)

**Figure 13-5. Comparison of θcs and θja for Different Clip Forces**

## 13.6.3. Heat Sink Design

The PPGA package may affect some existing heat sink designs. In one design, shown in Figure 13-6, the particular heat sink has a lip designed for a CPGA package to prevent movement of the heat sink relative to the package, socket and clip during mechanical shock tests. However, the PPGA package has a heatslug, external capacitors, and exposed pins on the top side of the package. For use on the PPGA package, if the heat sink slips out of its secured position, the lip may touch the exposed pins. Therefore, the lip needs to be extended to a proper length to lock the heat sink in a secured position. Intel's evaluations indicate that a 50 mil lip is not adequate and that a 70 mil lip is needed to ensure reliable performance during shock and vibration testing. Tests also show that the 70 mil lip works well with CPGA packages. Customers need to work with their heat sink suppliers to ensure that their heat sink designs can accommodate both PPGA and CPGA packages.

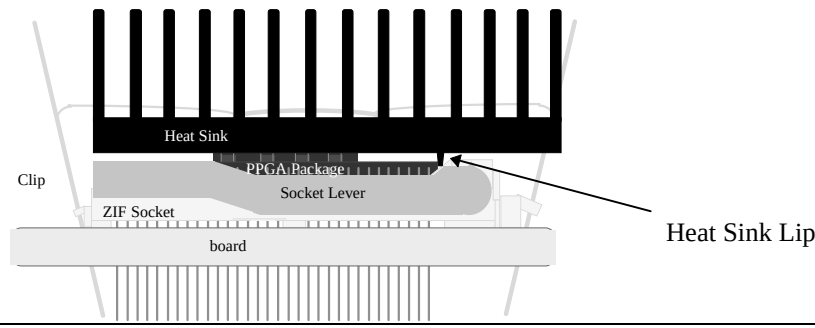



**Figure 13-6. A Heat Sink Design with a Lip**

### 13.6.4. Method for PPGA Heatsink Attach

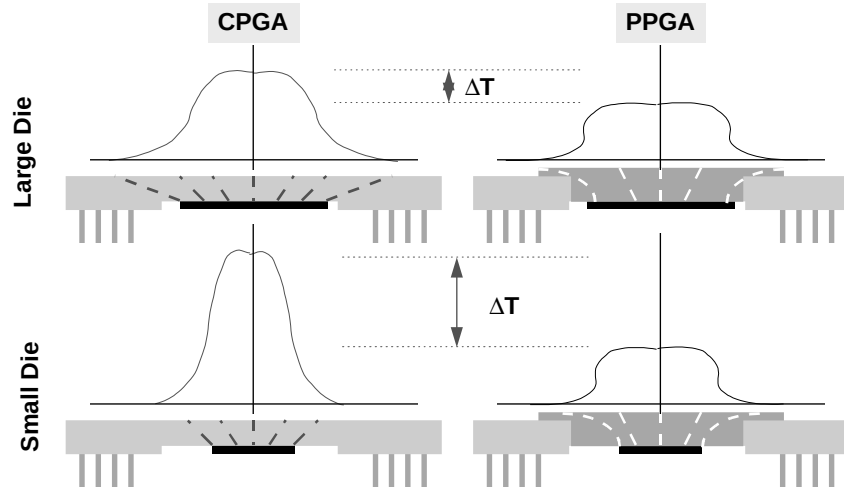
The impact of the PPGA package on board assembly was studied by assembling PPGA packages into sockets soldered on boards. A suggested sequence for mounting the PPGA packages is:

- With the package in the socket place the Conductacoat* foil on top of the package. The process flow for this step may be slightly different for the ZIF vs. LIF sockets. For ZIF the grease foil is placed on the CPU before insertion into the socket. For LIF socket place the thermal grease foil on the CPU after it is inserted into the socket. However, use manufacturing controls when stacking up the CPU, thermal interface and the heat sink to avoid foil misplacement on the PPGA slug.
- Place the heat sink on the package and hook the heat sink clip on to the socket.

## 13.7. PPGA PERFORMANCE CHARACTERISTICS

### 13.7.1. Thermal Characteristics

To improve thermal performance, the PPGA package uses a high thermal conductivity heat slug. The die is attached directly to the nickel plated copper heat slug, resulting in a lower thermal resistance than the comparable ceramic version. By effectively spreading the heat flux, the PPGA package is able to lower its thermal resistance. Based on measurements on the components, Figure 13-7 demonstrates the advantage of PPGA over CPGA in terms of thermal resistance.




**PPGA thermal benefits *(Tj improvements)* more pronounced when:**

absolute power is higher*....because of lower thermal R*

die size is smaller*....better spreading of concentrated heat flux*

**Figure 13-7. PPGA Has Better Thermal Conduction / Spreading**

$\theta_{ja}$ of PPGA is about 1.1 °C/W lower than that of CPGA. Table 13-5 to Table 13-10 detail the thermal resistance values for the components in ceramic pin grid array and plastic pin grid array packages.

**Table 13-5. $\theta_{ca}$ [°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)**

| | $\theta_{ca}$ [°C/W] vs Air Flow Rate [LFM] | | | | | |
|---|---|---|---|---|---|---|
| **Heat Sink Height** | **0** | **100** | **200** | **400** | **600** | **800** |
| 0.25” | 9.4 | 8.3 | 6.9 | 4.7 | 3.9 | 3.3 |
| 0.35” | 9.1 | 7.8 | 6.3 | 4.3 | 3.6 | 3.1 |
| 0.45” | 8.7 | 7.3 | 5.6 | 3.9 | 3.2 | 2.8 |
| 0.55” | 8.4 | 6.8 | 5.0 | 3.5 | 2.9 | 2.6 |
| 0.65” | 8.0 | 6.3 | 4.6 | 3.3 | 2.7 | 2.4 |
| 0.80” | 7.3 | 5.6 | 4.2 | 2.9 | 2.5 | 2.3 |
| 1.00” | 6.6 | 4.9 | 3.9 | 2.9 | 2.4 | 2.1 |
| 1.20” | 6.2 | 4.6 | 3.6 | 2.7 | 2.3 | 2.1 |
| 1.40” | 5.7 | 4.2 | 3.3 | 2.5 | 2.2 | 2.0 |
| 1.50” | 5.5 | 4.1 | 3.1 | 2.4 | 2.2 | 2.0 |
| None | 14.5 | 13.8 | 12.6 | 10.5 | 8.6 | 7.5 |

**NOTE:** $\theta_{ca}$ is case to ambient thermal resistance. $\theta_{ca}$ values shown in this table are typical values. The actual $\theta_{ca}$ values depends on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

**Table 13-6. $\theta_{jc}$ [°C/W] for a CPGA Package with and without a Heat Sink (CPGA)**

| | **No Heat Sink** | **With Heat Sink** |
|---|---|---|
| Average $\theta_{jc}$ | 1.7 | 1.25 |

**Table 13-7. $\theta_a$ [°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)**

| | $\theta_{ja}$ [°C/W] vs Air Flow Rate [LFM] | | | | | |
|---|---|---|---|---|---|---|
| **Heat Sink Height** | **0** | **100** | **200** | **400** | **600** | **800** |
| 0.25” | 10.6 | 9.5 | 8.1 | 5.9 | 5.1 | 4.5 |
| 0.35” | 10.3 | 9.0 | 7.5 | 5.5 | 4.8 | 4.3 |
| 0.45” | 9.9 | 8.5 | 6.8 | 5.1 | 4.4 | 4.0 |
| 0.55” | 9.6 | 8.0 | 6.2 | 4.7 | 4.1 | 3.8 |
| 0.65” | 9.2 | 7.5 | 5.8 | 4.5 | 3.9 | 3.6 |
| 0.80” | 8.5 | 6.8 | 5.4 | 4.1 | 3.7 | 3.5 |
| 1.00” | 7.8 | 6.1 | 5.1 | 4.1 | 3.6 | 3.3 |
| 1.20” | 7.4 | 5.8 | 4.8 | 3.9 | 3.5 | 3.3 |
| 1.40” | 6.9 | 5.4 | 4.5 | 3.7 | 3.4 | 3.2 |
| 1.50” | 6.7 | 5.3 | 4.3 | 3.6 | 3.4 | 3.2 |
| None | 16.2 | 15.5 | 14.3 | 12.2 | 10.3 | 9.2 |

**Table 13-8. $\theta_{ca}$ [°C/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)**

| | $\theta_{ca}$ [°C/W] vs Air Flow Rate [LFM] | | | | | |
|---|---|---|---|---|---|---|
| **Heat Sink Height** | **0** | **100** | **200** | **400** | **600** | **800** |
| 0.25” | 9.0 | 7.9 | 6.5 | 4.3 | 3.5 | 2.9 |
| 0.35” | 8.7 | 7.4 | 5.9 | 3.9 | 3.2 | 2.7 |
| 0.45” | 8.3 | 6.9 | 5.2 | 3.5 | 2.8 | 2.4 |
| 0.55” | 8.0 | 6.4 | 4.6 | 3.1 | 2.5 | 2.2 |
| 0.65” | 7.6 | 5.9 | 4.2 | 2.9 | 2.3 | 2.0 |
| 0.80” | 6.9 | 5.2 | 3.8 | 2.5 | 2.1 | 1.9 |
| 1.00” | 6.2 | 4.5 | 3.5 | 2.5 | 2.0 | 1.7 |
| 1.20” | 5.8 | 4.2 | 3.2 | 2.3 | 1.9 | 1.7 |
| 1.40” | 5.3 | 3.8 | 2.9 | 2.1 | 1.8 | 1.6 |
| 1.50” | 5.1 | 3.7 | 2.7 | 2.0 | 1.8 | 1.6 |
| None | 13.0 | 12.3 | 11.4 | 8.0 | 6.6 | 5.7 |

**NOTES:** $\theta_{ca}$ is case to ambient thermal resistance. $\theta_{ca}$ values shown in this table are typical values. The actual $\theta_{ca}$ values depends on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

**Table 13-9. $\theta_{jc}$ [°C/W] for a PPGA CPGA Package with and without a Heat Sink (PPGA)**

| | No Heat Sink | With Heat Sink |
|---|---|---|
| **Average $\theta_{jc}$** | 1.3 | 0.50 |

**Table 13-10. $\theta_{ja}$ [°C/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)**

| | $\theta_{ja}$ [°C/W] vs Air Flow Rate [LFM] | | | | | |
|---|---|---|---|---|---|---|
| **Heat Sink Height** | **0** | **100** | **200** | **400** | **600** | **800** |
| 0.25” | 9.5 | 8.4 | 7.0 | 4.8 | 4.0 | 3.4 |
| 0.35” | 9.2 | 7.9 | 6.4 | 4.4 | 3.7 | 3.2 |
| 0.45” | 8.8 | 7.4 | 5.7 | 4.0 | 3.3 | 2.9 |
| 0.55” | 8.5 | 6.9 | 5.1 | 3.6 | 3.0 | 2.7 |
| 0.65” | 8.1 | 6.4 | 4.7 | 3.4 | 2.8 | 2.5 |
| 0.80” | 7.4 | 5.7 | 4.3 | 3.0 | 2.6 | 2.4 |
| 1.00” | 6.7 | 5.0 | 4.0 | 3.0 | 2.5 | 2.2 |
| 1.20” | 6.3 | 4.7 | 3.7 | 2.8 | 2.4 | 2.2 |
| 1.40” | 5.8 | 4.3 | 3.4 | 2.6 | 2.3 | 2.1 |
| 1.50” | 5.6 | 4.2 | 3.2 | 2.5 | 2.3 | 2.1 |
| None | 14.3 | 13.6 | 12.7 | 9.3 | 7.9 | 7.0 |

## 13.8. ELECTRICAL CHARACTERISTICS

### 13.8.1. I/O Buffer

The package I/O model for components in PPGA packages is shown in Figure 13-7 as a first order buffer model. $R_0$ and $C_0$ values are independent of the package. Lp is the package inductance that includes bond wire inductance, trace inductance, pin inductance and socket inductance. Cp is the package capacitance consisting primarily of trace capacitance and socket capacitance. In this model, an effective inductance is used for the bond wire. Both self and mutual inductance are taken into account. The pin and its socket are considered as a single entity and a typical inductance value of 4.5 nH is used. A typical value of 1.0 pF is used for the socket capacitance.

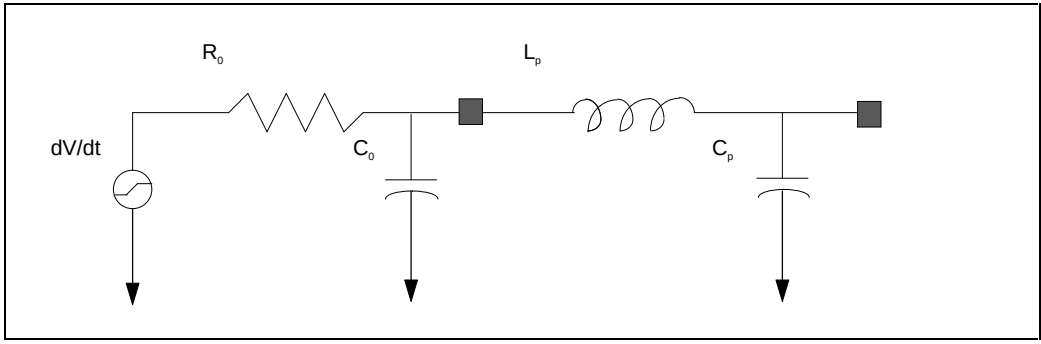



**Figure 13-8. First Order I/O Buffer Model for PPGA**

## 13.8.2. Signal Quality

Intel has performed noise measurements on components in both CPGA and PPGA packages. The results show that at the component level, the PPGA packages are comparable with the CPGA packages. In addition, the results indicate that all PPGA parts have a higher mean-core-power supply level than CPGA parts.

## 13.8.3. EMI

The Federal Communications Commission (FCC) has set limits on the maximum radiation from electrical systems. In turn, each component in a system should not exceed the typical level that is allocated to it. Electromagnetic Interference (EMI) levels from components in CPGA and PPGA packages have been measured with and without heat sinks attached. Measurements were performed up to a core clock frequency of 280 MHz. EMI levels are well below critical levels at all clock speeds tested. There is no significant EMI performance difference between CPGA and PPGA.

## 13.9. REVISION HISTORY

New Chapter