

**International
Packaging
Specifications**



CHAPTER 11

INTERNATIONAL PACKAGING SPECIFICATIONS

11.1. ELECTRONIC INDUSTRIES ASSOCIATION OF JAPAN (EIAJ)

EIAJ publishes the following general rules and standards as they apply to preparation of outline drawings on integrated circuits:

| Number | Nomenclature |
|------------|---|
| SD-74-1 | General rules for the preparation of outline drawings of semiconductor devices |
| ED-7400 | Standards for the dimensions of semiconductor devices |
| ED-7400-1 | Standards for the dimensions of semiconductor devices |
| ED-7400-2 | Standards for the dimensions of semiconductor devices |
| ED-7401A | Recommended practice for the preparation of outline drawings of semiconductor devices |
| ED-7402-1 | General rules for the preparation of outline drawings of integrated circuits; Small Outline Packages(SOP) |
| ED-7402-3 | General rules for the preparation of outline drawings of integrated circuits; Thin Small Outline Packages (type 1)(TSOP1) |
| ED-7402-4A | General rules for the preparation of outline drawings of integrated circuits; Thin Small Outline Packages (type 2)(TSOP2) |
| ED-7403-1 | General rules for the preparation of outline drawings of integrated circuits; Plastic Dual In-line Packages |
| ED-7404A | General rules for the preparation of outline drawings of integrated circuits; Quad Flat Packages(ZIP) |
| ED-7405 | General rules for the preparation of outline drawings of integrated circuits; Zig-zag In-line Packages |
| ED-7406A | General rules for the preparation of outline drawings of integrated circuits; Small Outline J-lead packages(SOJ) |
| ED-7407 | General rules for the preparation of outline drawings of integrated circuits; Quad Flat J-lead Packages (QFJ/PLCC) |
| ED-7408A | General rules for the preparation of outline drawings of integrated circuits; Pin Grid Array packages(PGA) |
| ED-7413 | General rules for the preparation of outline drawings of integrated circuits; Small Inline Packages(SIP) |
| ED-7431A | General rules for the preparation of outline drawings of integrated circuits; Quad Tape Carrier Packages(QTP) |

11.2. JOINT ELECTRON DEVICE ENGINEERING COUNCIL (JEDEC)

JEDEC Publication 95 lists all package outlines.

11.3. MIL STANDARDS

The following military standards include specifications required to meet U. S. Military requirements:

- **MIL-M-38510** General Specifications for Microcircuits
- **MIL-STD-883** Test Methods/Procedures for Microelectronics

11.4. SEMICONDUCTOR EQUIPMENT AND MATERIALS INSTITUTE, INC.

For a list of SEMI standards, reference the *Book of SEMI Standards*, 1990, Vol.4, Packaging Division, 605 E. Middlefield Road, Mountain View, CA 94043, U.S.A. Phone:(415) 964-5111. FAX: (415) 967-5375. TELEX: 856-777 SEMI-MNTV

11.5. INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC) STANDARDS

| Number | Nomenclature |
|----------------------------|---|
| ANSI/IPC-S-815B | General requirements for soldering electronic connections |
| ANSI/IPC-SM-780 surface | Component packaging and inter-connecting, with emphasis on mounting |
| ANSI/IPC-SM-782 | Surface mount land patterns |
| ANSI/IPC-SM-786 | Impact of moisture on plastic I/C package cracking |

For a list of additional IPC standards, contact: IPC, 7380 N. Lincoln Ave., Lincolnwood, Illinois, 60646. Phone: (708) 677-2850.