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Introduction

CHAPTER 1
INTRODUCTION

1.1. OVERVIEW OF INTEL PACKAGING TECHNOLOGY

As semiconductor devices become significantly more complex, electronics designers are challenged to fully harness their computing power.Today's products can feature more than three million transistors, and device count is expected to increase to one hundred million by the year 2000. With a greater number of functions integrated on a die or chip of silicon, manufacturers and users will face new and increasingly challenging electrical interconnect issues. To tap the power of the die efficiently, each level of electrical interconnect from the die to the functional hardware or equipment must also keep pace with these revolutionary devices. Package design, at the first interconnect level, has a major impact on device performance and functionality.

Today, submicron feature size at the die level is driving package feature size down to the design-rule level of the early transistors. At the same time, electronic equipment designers are shrinking their products, increasing complexity, and setting higher expectations for performance. To meet these demands, package technology must deliver higher lead counts, reduced pitch, minimum footprint area, and significant overall volume reduction.

Circuit performance is only as good as the weakest link. Therefore, device performance is for all practical purposes determined by the package. While packaging cannot add to the theoretical performance of the device design, it can have adverse effects if not optimized. An optimum package design would achieve 100% of the theoretical device, application-specific performance, which in practice is un-achievable. Package performance, therefore, is the best compromise of electrical, thermal, and mechanical attributes, as well as physical outline, to meet product specific reliability and cost objectives.

Package technology has responded to these challenges with a number of changes and improvements. To address the increasing pin counts, array connections are used rather than the peripheral pins. While helping to control package size, this approach also enhances electrical performance by reducing trace length. Electrical performance is also improved by the use of copper signal traces in the package. Copper provides a significant reduction in resistance when compared to tungsten used in ceramic packages. To further improve the electrical environment, substrate material has been changed from ceramic to organic.

The continuing demand for higher performance products is requiring levels of package performance unattainable by the molded plastic and ceramic packages of the past decade. These factors have driven a variety of major innovations in Intel package design, such as the Tape Carrier Package (TCP), the Plastic Pin Grid Array (PPGA) and the Plastic Ball Grid Array (PBGA) packages. While they differ in form factor, all provide improved electrical and/or thermal performance.

Fit, form, and function are in the eye of the beholder, and any Intel device can serve more than one market and/or application requiring widely divergent package attributes.

Therefore, "one size fits all" is not a practical approach to device packaging. Packaging technology is not a single technology , but instead consists of more than 20 industry proven combinations of technologies or technology sets that can be categorized by package families.

In support of the growing number of Intel devices and to meet the industry demand for package-specific applications, Intel's package portfolio has more than doubled during the last ten years.

1.2. PURPOSE OF THIS DATABOOK

Intel's Packaging Databook is intended to serve as a data reference for engineering design, as well as a guide to Intel package selection and availability. Each of the chapters provide a comprehensive and in-depth analysis of Intel packaging technology, from information on IC assembly, performance characteristics, and physical constants, to detailed discussions of surface mount technology and Intel shipping and packing.

Chapter 1 provides an analysis of Intel's package families, including package attributes, package types, and a package selection guide.

Chapter 2 offers a detailed view into Intel package module outlines and dimensions.

Chapter 3 covers assembly manufacturing technology. The chapter begins with a brief introduction and a discussion of statistical tools used in the manufacturing process. It also includes a comprehensive analysis of Intel's IC assembly process flow.

Chapter 4 explores package characteristics and tabulates in-depth data electrical, mechanical, and thermal IC package characteristics.

Chapter 5 addresses physical constants of IC package materials. The charts in this chapter provide valuable information on mechanical, electrical, and thermal properties of case materials, lead/lead frames, and soldering material characteristics.

Chapter 6 ESD/EOS Precautions describes electrical static discharge and electrical over stress.

Chapter 7 explores surface mount technology.

Chapter 8 describes Desiccant Packing Methods and Materials. Moisture Sensitivity and Package Cracking is also examined.

Chapter 9 provides an in-depth analysis of Board Solder Reflow Process Recommendations.

Chapter 10 describes the various packing and shipping methods used at Intel. Packing media, desiccant pack materials, and shipping data are clearly illustrated.

Chapter 11 provides the reader with a listing of international packaging specifications and a comprehensive resource library.

Chapter 12 Profiles the Tape Carrier Package.

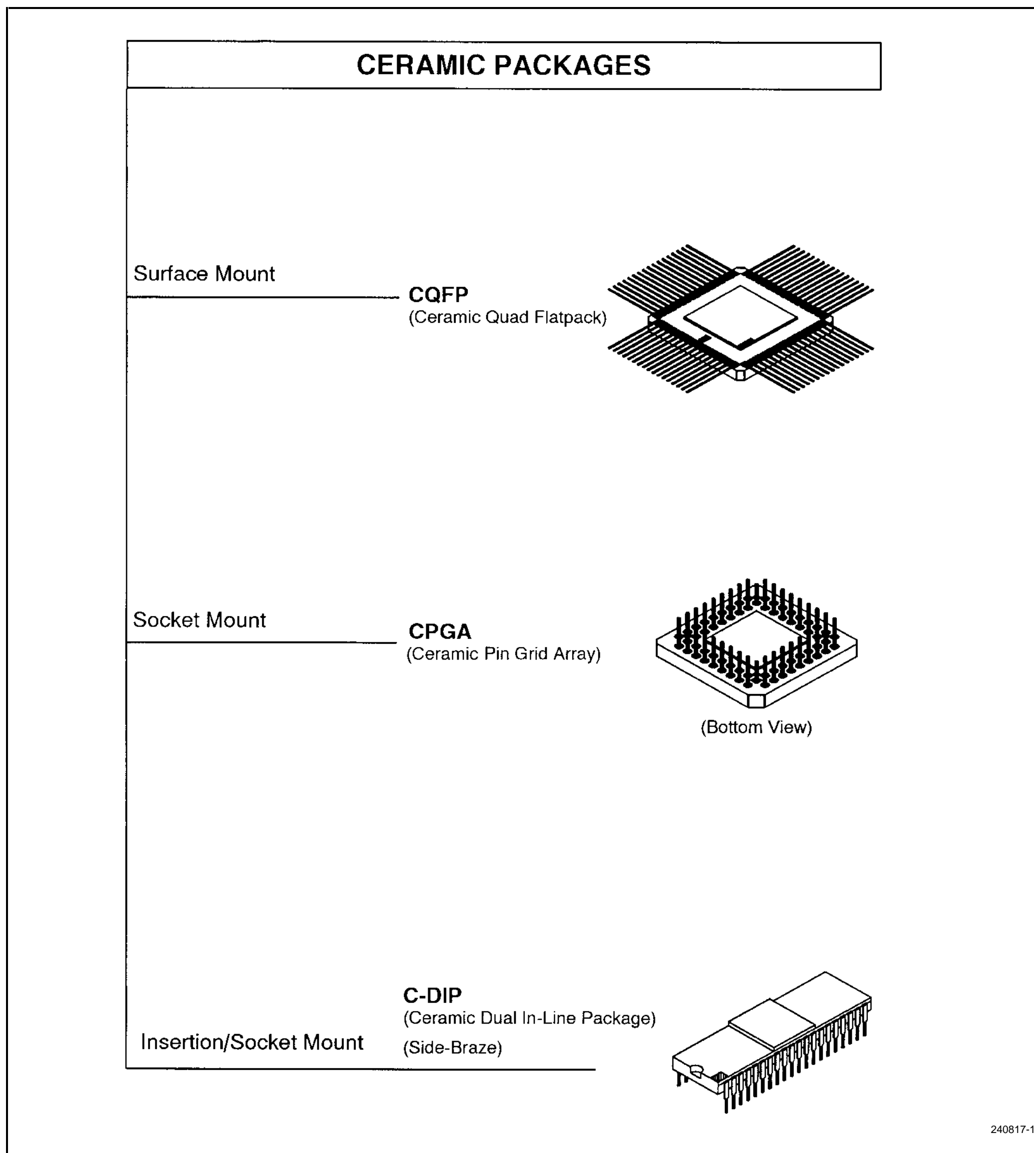
Chapter 13 Introduces the new Plastic Pin Grid Array Package technology.

Chapter 14 Provides a profile of the Intel Plastic Ball Grid Array technology.

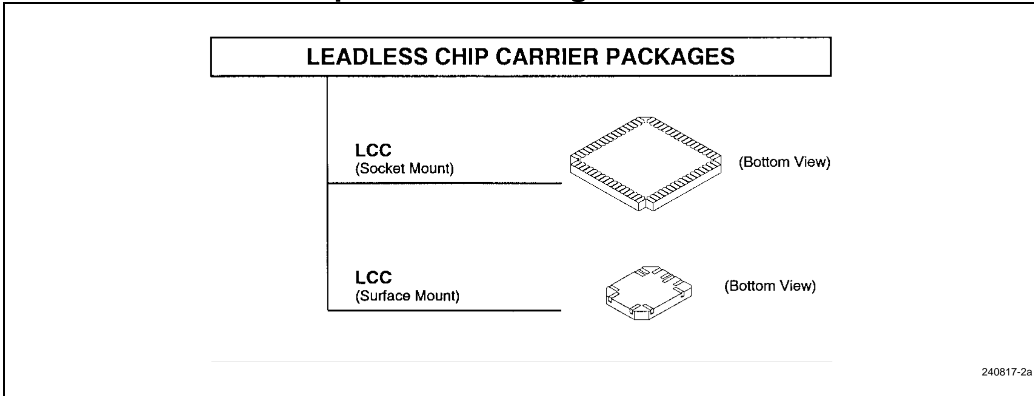
Glossary offers a detailed view of packaging related technical terminology.

1.3. PACKAGE TYPES

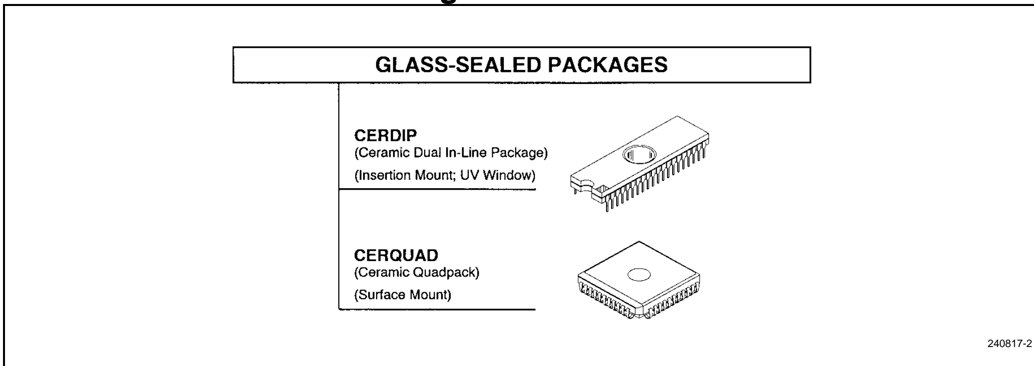
1.3.1. Ceramic Packages



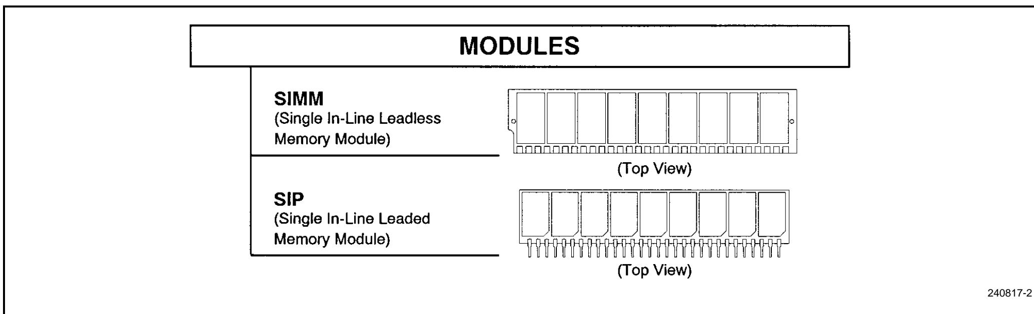
1.3.2. Leadless Chip Carrier Packages



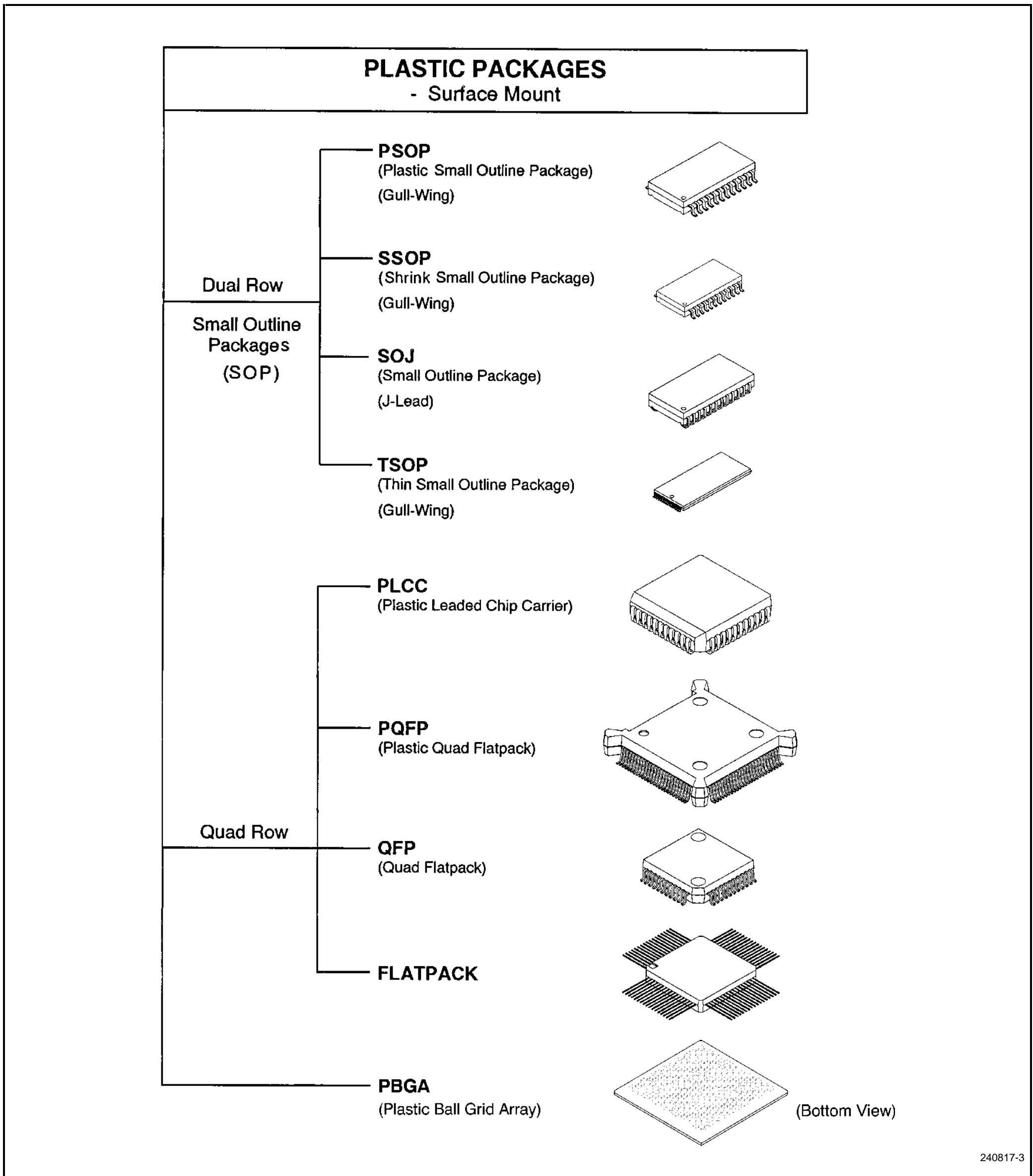
1.3.3. Glass-Sealed Packages



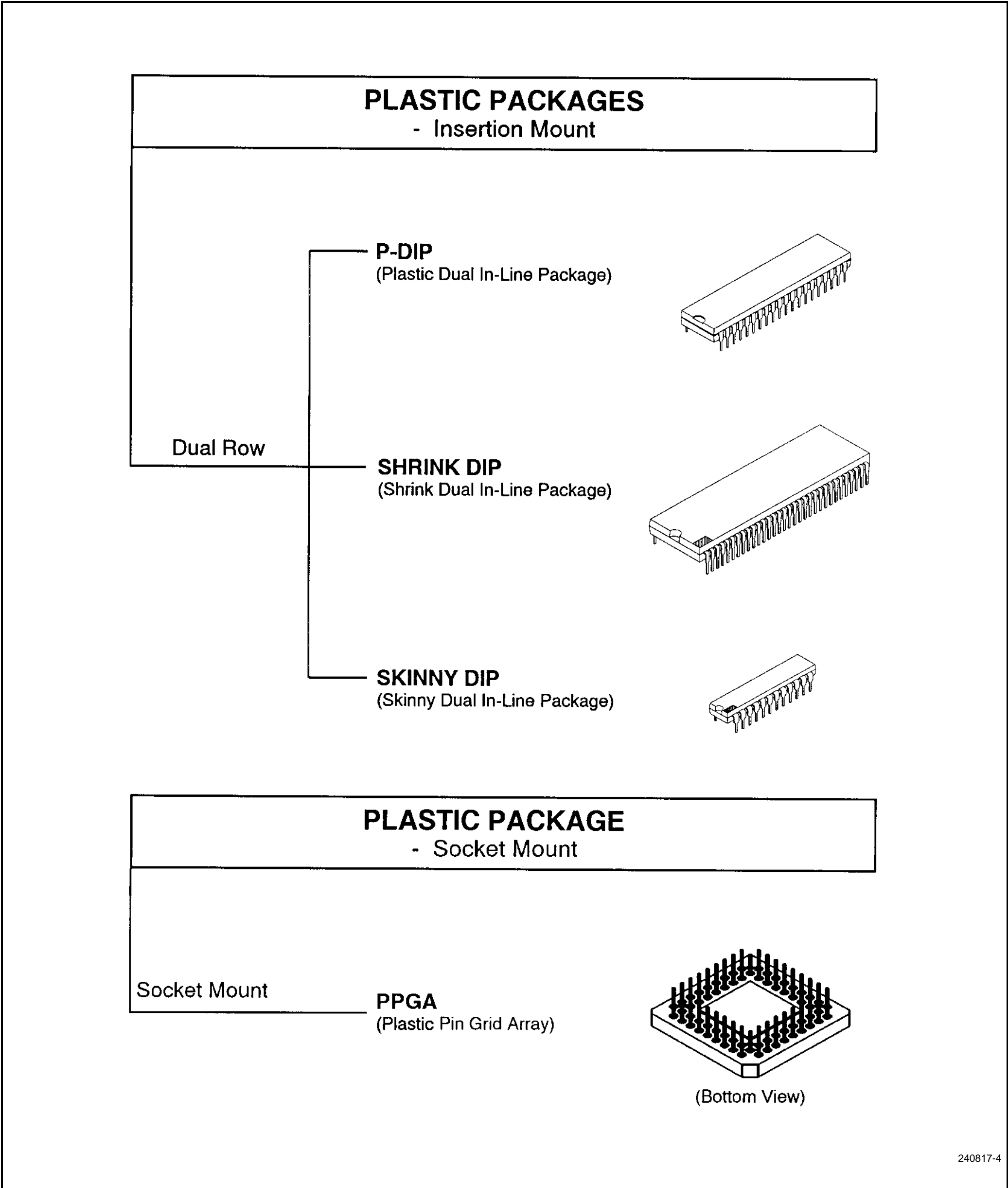
1.3.4. Modules



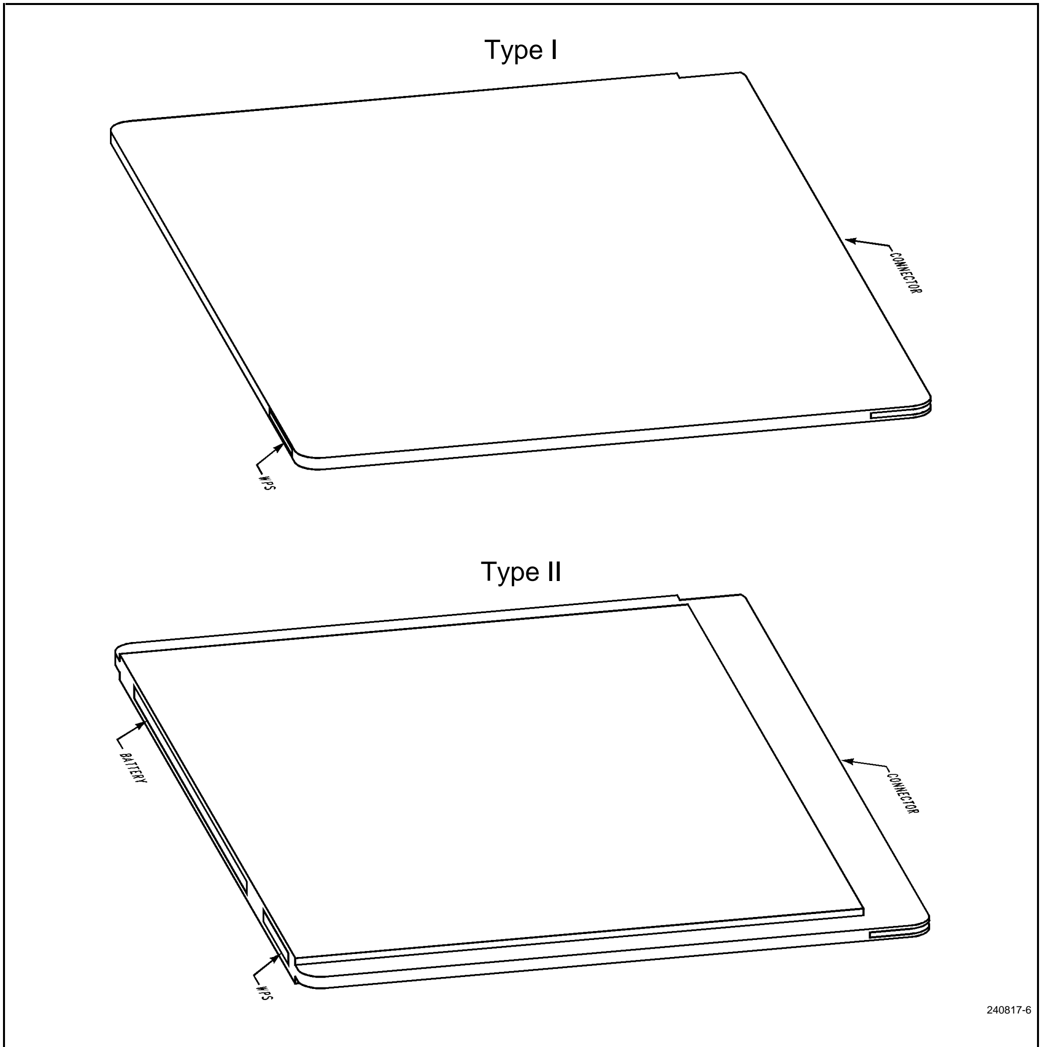
1.3.5. Plastic Packages - Surface Mount



1.3.6. Plastic Packages - Insertion Mount/Socket Mount



1.3.7. PCMCIA PC Card - Type 1 and Type 11



1.4. PACKAGE ATTRIBUTES

1.4.1. Ceramic Package Attributes

Table 1-1. Ceramic Dual In-Line Package (C-DIP)

Lead Count	16	18	22	24	28	32	40	48
Sq./Rect.	R	R	R	R	R	R	R	R
Pitch (Inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (Inches)	0.109	0.109	0.109	*0.132 0.100	*0.132 0.102	0.120	*0.154 0.123	*0.172 0.142
Weight (gm)	1.41	1.62	1.89	2.22	4.56			8.43
Max. Footprint (Inches)	0.810	0.910	1.115	1.215	1.415	1.614	2.020	2.420
UV Erasable				X	X	X	X	X
Shipping Media Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X
Desiccant Package								
Comments/Footnotes	* EPROM LID							

Table 1-2. Leadless Chip Carrier (LCC)

Lead Count	18	20	28	32	44	68	68
Sq/Rect.	R	R	S	R	S	S	S
Pitch (Inches)	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (inches)	0.68	0.68	0.073	*0.080 0.108	*0.092 0.120	0.096	0.130
Weight (gm)		0.70	1.18	1.02	2.33	4.67	4.67
Max. Footprint (Inches)	0.440	0.440	0.460	0.560	0.665	0.960	0.960
UV Erasable	x	x	x	See Note	See Note		x
Shipping Media Tubes Tape & Reel Trays	x	x	x	x	x	x	x
Desiccant Pack							
Comments/Footnotes	32L--0.080 = Solid Lid, Non-UV 32L--0.108 = EPROM Lid, UV 44L--0.092 = Solid Lid, Non-UV 44L--0.120 = EPROM Lid, UV						

Table 1-3. Ceramic Pin Grid Array

Lead Count	68	68	68	88	88	88	132	168	208	240-280	272-320	387
Sq/Rect.	S	S	*S	S	S	*S	S	S	S	S	S	R
Pitch (Inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.105	0.110	0.125	0.105	0.110	0.125	0.110	0.110	0.110	0.110	0.110	0.110*
Weight (gm)	8.69	8.69	8.69	10.43	10.43	10.43	16.07	23.3				84
Max. Footprint (Inches)	1.180	1.180	1.180	1.380	1.380	1.380	1.480	1.780	1.780	1.980	2.170	2.670
UV Erasable			x			x						
Shipping Media												
Tubes												
Tape & Reel												
Trays	x	x	x	x	x	x	x	x	x	x	x	x
Desiccant Pack												
Comments/ Footnotes	* With EPROM											

Without heatspreader

Table 1-4. Ceramic Quad Flatpack (CQFP)

Lead Count	68	164	196
Sq/Rect.	S	S	S
Pitch (Inches)	0.050	0.025	0.025
Package Thickness (inches)			
Weight (gm)	12*	12*	17*
Max. Footprint (Inches)	0.970	2.520	2.520
UV Erasable	x		
Shipping Media			
Carrier	x	x	x
Tape & Reel			
Trays			x
Desiccant Pack			
Comments/Footnotes	*Weighed with tie bar attached.		

Table 1-5. CERDIP

Lead Count	16	18	20	22	24	28	32	40	42
Sq/Rect.	R	R	R	R	R	R	R	R	R
Pitch (Inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.157	0.157	0.153	0.165	0.165	0.167	0.167	0.167	0.167
Weight (gm)	2.1		2.87	4.39	6.69	8.68	9.81	12.03	
Max. Footprint (Inches)	0.785	0.915	0.995	1.095	1.285	1.485	1.680	2.085	2.185
UV Erasable	X	X	X	X	X	X	X	X	X
Shipping Media									
Tubes	x	x	x	x	x	x	x	x	x
Tape & Reel									
Trays									
Desiccant Pack									
Comments/ Footnotes	Available with or without UV Window. Weights are without UV Window.								

Table 1-6. Ceramic QuadPack (CERQUAD)

Lead Count	44	52	68
Sq/Rect.	S	S	S
Pitch (Inches)	0.050	0.050	0.050
Package Thickness (inches)	0.172	0.172	0.172
Weight (gm)	2.85	3.59	7.14
Max. Footprint(Inches)	0.695	0.795	.995
UV Erasable	x	x	x
Shipping Media			
Tubes	x	x	x
Tape & Reel			
Trays			
Desiccant Pack			
Comments/Footnotes	Available with or without UV Window		

1.4.2. Plastic Package Attributes

Table 1-7. Plastic Dual In-Line (PDIP)

Lead Count	16	18	20	24	28	32	40	48	64
Sq/Rect.	R	RR	R	R	R	R	R	R	R
Pitch (Inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.132	0.132	0.132	0.152	0.152	0.150	0.160	0.162	0.167
Weight (gm)	1.045	1.248	1.418	1.67	1.94	4.815	6.128	7.912	12.05
Max. Footprint (Inches)	0.780	0.920	1.050	1.260	1.470	1.655	2.070	2.440	2.290
UV Erasable									
Shipping Medi Tubes Tape & Reel Trays	x	x	x	x	x	x	x		x
Desiccant Pack									
Comments/ Footnotes	Some pin counts available in; Half lead, Wide body, Wide Body; and Standard Type P								

Table 1-8. Plastic (Flatpack)

Lead Count	68
Sq/Rect.	S
Pitch (Inches)	0.050
Package Thickness (inches)	0.168
Weight (gm)	5.6
Max. Footprint (Inches)	1.780
UV Erasable	
Shipping Media Tubes Tape & Reel Trays	 x
Desiccant Pack	
Comments/Footnotes	Through Hole Use Only

Table 1-9. Plastic Quad Flatpack (PQFP)

Lead Count	84	100	132	164	196
Sq/Rect.	S	S	S	S	S
Pitch (Inches)	0.025	0.025	0.025	0.025	0.025
Package Thickness (inches)	0.170	0.170	0.170	0.170	0.170
Weight (gm)	2.07	2.8	4.2	6.1	8.55
Max. Footprint (Inches)	0.790	0.890	1.090	1.290	1.490
UV Erasable					
Shipping Media					
Tubes	x	x	x	x	x
Tape & Reel	x	x	x	x	x
Trays	x	x	x	x	x
Desiccant Pack	x	x	x	x	x
Comments/ Footnotes	All PQFPs are “Gull Wing” with bumpers *MM-PQFP				

Table 1-10. Quad Flatpack

Lead Count	44	48	64	80	80	100	100	128	144	160	176	208
Sq/Rect.	S	S	S	S	R	S	R	S	S	S	S	S
Pitch (Inches)	0.800	0.800	0.650	0.500	0.800	0.50	0.80	0.80	0.5	0.65	0.5	0.500
Package Thickness (inches)	2.35	2.55	2.55	1.66	3.15	1.66	3.15	3.65	1.5	3.65	1.5	3.56
Weight (gm)	0.42		0.71	0.50	1.65	0.64	1.65					5.18 10.85*
Max. Footprint (Inches)	0.503	0.610	0.618	0.562	0.720	0.641	0.720	1.275	.881	1.220	1.039	1.220
UV Erasable												
Shipping Media												
Tubes												
Tape & Reel												
Trays	X	X	X	X	X	X	X	X	X	X	X	X
Desiccant Pack	X	X	X	X	X	X	X	X	X	X	X	X
Comments/ Footnotes	Gull Wing lead Configuration, non-bumped											

* With heat slug

Table 1-11. Plastic Leaded Chip Carrier (PLCC)

Lead Count	20	28	28	32	44	52	68	84
Sq/Rect.	S	S	R	R	S	S	S	S
Pitch (Inches)	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (inches)	0.152	0.152	0.108	0.108	0.148	0.150	0.150	0.150
Weight (gm)	0.705	1.15	0.85	1.1	2.31	3.17	4.8	6.2
Max. Footprint (Inches)	0.395	0.495	See Note	See Note	0.695	0.795	0.995	1.195
UV Erasable								
Shipping Media Tubes Tape & Reel Trays	 X X X	 X X X	 X X X	 X X X	 X X X	 X X	 X X X	 X X X
Desiccant Pack	X	X	X	X	X	X	X	X
Comments/ Footnotes	All PLCC's are "J" Lead 28R--0.39 x 0.59 32R--0.48 x 0.59							

Table 1-12. Small Outline Package J-Lead (SOJ)

Lead Count	20	24
Sq/Rect.	R	R
Pitch (Inches)	1.27	1.27
Package Thickness (inches)	0.105	0.113
Weight (gm)	0.50	0.62
Max. Footprint (Inches)	0.680	0.637
UV Erasable		
Shipping Media Tubes Tape & Reel Trays	 x x	 x x
Desiccant Pack	x	x
Comments/Footnotes	"J" Configuration	

Table 1-13. Plastic Small Outline Package (PSOP)

Lead Count	44
Sq/Rect.	R
Pitch (Inches)	1.27
Package Thickness (inches)	2.95
Weight (gm)	1.89
Max. Footprint (Inches)	0.640
UV Erasable	
Shipping Media Tubes Tape & Reel Trays	 x x x
Desiccant Pack	x
Comments/Footnotes	Gull Wing Lead Configuration

Table 1-14. Thin Small Outline Package (TSOP)

Lead Count	32	40	48	56
Sq/Rect.	R	R	R	R
Pitch (Inches)	0.50	0.50	0.50	0.50
Package Thickness (inches)	0.0392	0.039	0.039	0.039
Weight (gm)	0.37	0.46	0.56	0.63
Max. Footprint (Inches)	0.795	0.795	0.795	0.795
UV Erasable				
Shipping Media Tubes Tape & Reel Trays	 x x	 x x	 x x	 x x
Desiccant Pack	x	x	x	x
Comments/ Footnotes	TSOP is “Gull Wing” Configuration			

Table 1-15. Shrink Small Outline Package (SSOP)

Lead Count	56
Sq/Rect.	R
Pitch (Inches)	0.80
Package Thickness (inches)	0.050
Weight (gm)	1.15
Max. Footprint (Inches)	0.642
UV Erasable	
Shipping Media Tubes Tape & Reel Trays	 x x
Desiccant Pack	x
Comments/Footnotes	Gull Wing Lead Configuration

1.4.3. Module Attributes

Table 1-16. Single In-Line Leaded Memory Module (SIP)

Lead Count	30
Sq/Rect.	R
Pitch (Inches)	2.54
Package Thickness (inches)	2.00
Weight (gm)	
Max. Footprint (Inches)	3.105
UV Erasable	
Shipping Media Tubes Tape & Reel Trays	 x
Desiccant Pack	
Comments/Footnotes	Insertable Module

Table 1-17. Single In-Line Leadless Memory Module (SIMM)

Lead Count	30	80
Sq/Rect.	R	R
Pitch (Inches)	0.100	0.050
Package Thickness (inches)	0.20	0.33
Weight (gm)		15.7
Max. Footprint (Inches)	3.505	4.655
UV Erasable		
Shipping Media		
Tubes		x
Tape & Reel	x	
Trays		
Desiccant Pack		
Comments/Footnotes	JEDEC Standard Insertable Module	

1.5. PACKAGE/MODULE/PC CARD SELECTION GUIDE

Table 1-18. Package/Module/PC Card Selection Guide

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
	16	C	
	18	C	
Ceramic Dual-In-Line (C-DIP). 0.100” Pitch,	22	C	
Socket or Insertion Mount			
24, 28, 40, 48 C-DIP’s Available with EPROM or	24		
Solid Lid		C	
32 C-DIP Available with EPROM (lid) Only	28		
	32	C	
	40	C	
	48	C	
		C	
	18	R	
	20	R	
Ceramic Leadless Chip Carrier (LCC), 0.050”	28	R	
Pitch, Socket or Surface Mount			
32, 44, and 68 LCC’s Available with EPROM or	32	R	
Solid Lid		R	
	44	R	
	68	R	
	68	A	
	88	A	
Ceramic Pin Grid Array (CPGA), 0.100” Pitch,	88	A	Cavity Down
Socket or Insertion Mount			
	132	A	Cavity Down
68L and 88L “Cavity Up” Available with EPROM	168	A	Cavity Down
or Solid Lid			
	208	A	Cavity Down
	240-280	A	Cavity Down
	272-320	A	Cavity Down
	387	G	Cavity Down
Ceramic Quad Flatpack (CQFP), 68L Available	68	Q	Flat Leads
in 0.050” Pitch. 164L and 196L Available in 0.025”	164	K	Flat Leads
Pitch, Socket or Surface Mount	196	K	Flat Leads

Table 1-18. Package/Module/PC Card Selection Guide (Contd.)

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
Ceramic DIP (CERDIP), 0.100" Pitch, Socket or Insertion Mount	16 18 20 22 24 24 28 28 32 40 42	D D D D DP D DP D D D D	 300 Mil 300 Mil
CERQUAD, 0.50" Pitch, Socket Mount, All Leadcounts Offer UV Window	44 52 68	J J J	
Plastic Dual-In-Line (PDIP); 9\0.100" Pitch, 64L "Shrink DIP" has a 0.070" Pitch Socket and Insertion Mount	16 18 20 24 24 28 28 32 40 48 64	P P P P PD P PD P P P U	 300 Mil 300 Mil Shrink
Plastic Flatpack (PFP), 0.050" Pitch Shipped in Carrier with flat Lead, Through-Hole Mount	68	FP	
Plastic Leaded Chip Carrier (PLCC), 0.050: Pitch Surface or Surface Mount 28L is Available in a Square and Rectangular Package Body 32L is Available in a Rectangular Package Body Only	20 28 32 44 52 68 84	N N N N N N N	Sq. Sq,/Rect. Rect. Sq. Sq. Sq. Sq.

Table 1-18. Package/Module/PC Card Selection Guide (Contd.)

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
Plastic Quad Flatpack (PQFP), .0.025" Pitch, Surface Mount Some Packages Available in a Variety of Options: Die UP, Die Down, and Die Down with Heatspreader	84 100 132 164 196	KD KD, KU, NG KD, KU, NG KU KU	
Quad Flatpack (QFP), Variable Lead Pitch Surface Mount. Quad Flatpack (QFP), Surface Mount, Copper Lead Frame	44 48 64 80 100 128 144 160 176 208 208	S S S SB, S SB,S S SB S SB SB SB	Sq./Rect. Sq./Rect.
Plastic Ball Grid Array	208 272 324 352	FW FW FW GC	Sq
Plastic Pin Grid Array	296	FV	Sq
Small Outline J-Lead (SOJ), 1.27mm Pitch Surface Mount	20 24	PE PE	
Plastic Small Outline Package (PSOP), 1.27 mm Pitch, Surface Mount	44	PA	
Shrink Small Outline Package (SSOP), 0.80 mm Pitch, Surface Mount	56	DA	
Thin Small Outline Package (SSOP) Pitch, Surface Mount Available in Die Up or Die Down (32, 40 only)	32, 40 48 56	E, R E E, DD	
Single In-Line Leaded Memory Module (SIP), 2.54mm Pitch, Socket or Insertion Mount	30	GB	
Single In-Line Leadless Memory Module (SIMM) 0.100" Pitch, Socket Mount	30 80	SM SM	

1.6. REVISION SUMMARY

- Added PPGA Package Type
- Updated Package/Module/PC Card Selection Guide