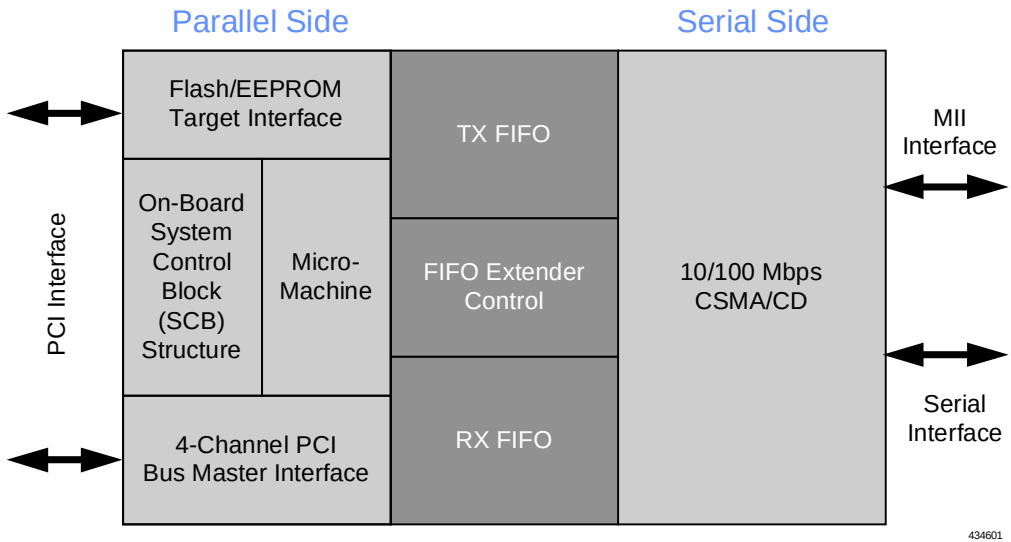
INTEL 82557 FAST ETHERNET PCI BUS CONTROLLER

- **Optimum Integration for Lowest Cost Solution**
  - **IEEE 802.3 10Base-T and 100Base-T compatible**
  - **Glueless 32-bit PCI bus master interface**
  - **Flash support up to 1 Mbyte**
- **High Performance Networking Functions**
  - **Chained memory structure similar to the 82596 controller**
  - **Improved dynamic transmit chaining**
  - **Programmable transmit threshold**
  - **Early receive interrupt**
  - **Large, 3 Kbyte internal receive and transmit FIFOs**
  - **Back to back transmit at 100 Mbps, within minimum IFS**
- **Ease of Use**
  - **Built-in interface to MII compliant physical layer devices**
  - **Standard seven pin ENDEC interface to serial device such as the Intel 82503 for 10 Mbps only designs**
  - **Full or half duplex capable at 10 or 100 Mbps**
  - **EEPROM support**
  - **Internal counters for network management**



Intel 82557 Block Diagram

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1.0. INTRODUCTION

1.1. 82557 Overview

The 82557 is Intel's first highly integrated 32-bit PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. The 82557 offers a high performance LAN solution while maintaining low-cost through its high-integration. It contains a 32-bit PCI Bus Master interface to fully utilize the high bandwidth available (up to 132 Mbytes per second) to masters on the PCI bus. The bus master interface can eliminate the intermediate copy step in Receive (RCV) and Transmit (XMT) frame copies, resulting in faster processing of these frames. It maintains a similar memory structure to the Intel 82596 LAN Co-processor, however, these memory structures have been streamlined for better network operating system (NOS) interaction and improved performance.

The 82557 contains two large receive and transmit FIFOs (3 Kbytes each) which prevent data overruns or underruns while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960 nanosecond inter frame spacing. Full support for up to 1 Mbyte of FLASH enables network management support via Intel FlashWorks utilities as well as remote boot capability (a BIOS extension stored in the FLASH which could allow a node to boot itself off of a network drive). For 100 Mbps applications, the 82557 contains an IEEE MII compliant interface to the Intel 82553 serial interface device (or other MII compliant PHYs) which will allow connection to 100/10 Mbps networks. For 10 Mbps networks, the 82557 can be interfaced to a standard ENDEC device (such as the Intel 82503 Serial Interface), while maintaining software compatibility with 100 Mbps solutions.

The 82557 is designed to implement cost effective, high performance PCI add-in adapters, PC motherboards, or other interconnect devices such as hubs or bridges. Its combination of high integration and low cost make it ideal for these applications.

1.2. Features and Enhancements

The following list summarizes the main features of the Intel 82557 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like Chained Memory Structure
- Improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- FLASH support up to 1Mbyte
- Large on-chip receive and transmit FIFOs (3 Kbytes each)
- On-chip counters for network management
- Back to back transmit at 100 Mbps
- EEPROM support
- Support for both 10 Mbps and 100 Mbps Networks
- Interface to MII compliant PHY devices, including Intel 82553 Physical Interface component for 10/100 Mbps designs
- IEEE 802.3u 100Base-T, TX, and T4 compatible
- Interface to Intel 82503 or other serial device for 10 Mbps designs: IEEE 802.3 10Base-T compatible
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Full or half duplex-capable at 10 and 100 Mbps
- 160-Lead QFP package

1.3. Compliance to Industry Standards

The 82557 has two interfaces. The host system PCI bus interface and the serial or network interface. The network interface complies to the IEEE standard for 10BASET-T, TX, and T4 and 100Base-T, TX, and T4 Ethernet interfaces. The 82557 also complies to the PCI Bus Specification, Revision 2.1.

1.3.1. Other Literature

This data sheet provides complete pin identification, definitions and electrical specifications. It also provides an overview of each main subsystem within the component. Most of this information is aimed at hardware design engineers.

Software engineers and others who are designing interfaces or writing device drivers for this component, should refer to the *82557 User's Manual*. This document provides more detailed information on feature sets, register descriptions and implementation steps for various functions.

2.0. PIN DEFINITIONS

Figure 1 shows pin numbering and signal identification for the 82557. Sections 2.1 through 2.5 describe the signals.

2.1. PCI Bus Interface Signals

The following sections describe the 82557 pins and signals by function.

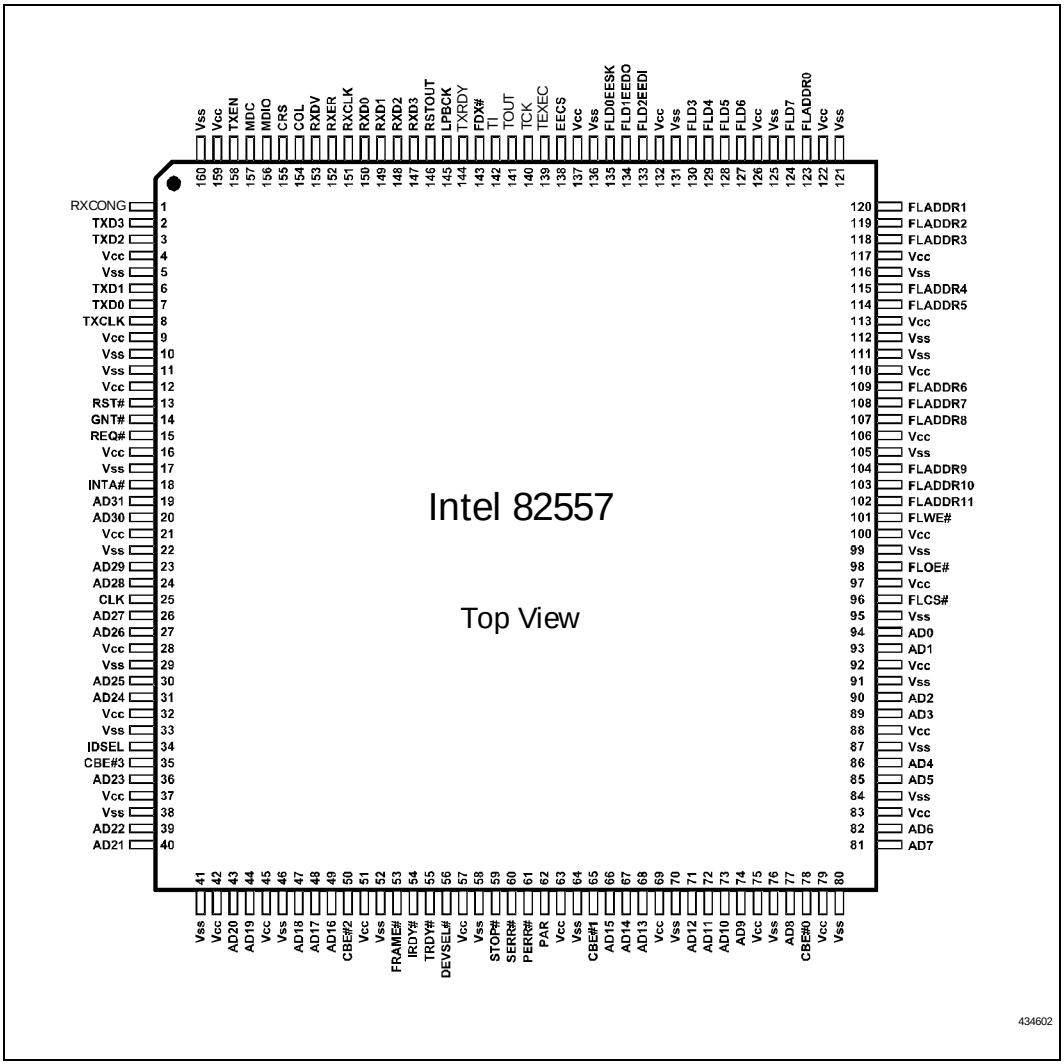

Figure 1. Device Pinout, Top View

2.1.1. SIGNAL TYPE DEFINITION

IN	Input is a standard input-only signal
OUT	Totem Pole Output is a standard active driver.
TS	Tri-State is a bi-directional, tri-state input/output pin.
STS	Sustained Tri-State is an active low tri-state signal owned and driven by the 82557. When the 82557 drives this pin low, it must drive it high for at least one clock before letting it float.
OD	Open Drain allows multiple devices to share as a wired-OR.

2.1.2. ADDRESS AND DATA PINS

Symbol	Pin	Type	Name and Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31	94 93 90 89 86 85 82 81 77 74 73 72 71 68 67 66 49 48 47 44 43 40 39 36 31 30 27 26 24 23 20 19	TS	Address and Data are multiplexed on the same PCI pins by the 82557. A bus transaction consists of an address phase followed by one or more data phases.The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD0-31 contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, a DWORD address. The 82557 uses ‘Little Endian’ byte ordering. During data phases AD0-7 contain the least significant byte (LSB) and AD24-31 contain the most significant byte (MSB).

Symbol	Pin	Type	Name and Function
CBE#0 CBE#1 CBE#2 CBE#3	78 65 50 35	TS	Bus Command and Byte Enables are multiplexed on the same PCI pins by the 82557. During the address phase of a transaction, C/BE0-3# define the bus command. During the data phase C/BE0-3# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte 0 (LSB) and C/BE3# applies to byte 3 (MSB).
PAR	62	TS	Parity is even parity across AD0-31 and C/BE0-3#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82557 is a bus master, it drives PAR for address and write data phases. As a slave, it drives PAR for read data phases.

2.1.3. INTERFACE CONTROL PINS

Symbol	Pin	Type	Name and Function
FRAME#	53	STS	Frame# is driven by the 82557 to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
IRDY#	54	STS	Initiator Ready# indicates the ability of the 82557 (as a bus mastering device) to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock in which both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD0-31. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82557 drives IRDY# when acting as a master, and samples it when acting as a slave.
TRDY#	55	STS	Target Ready# indicates the ability of the 82557 (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock in which both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD0-31. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both TRDY# and IRDY# are asserted together. The 82557 drives TRDY# when acting as a slave, and samples it when acting as a master.
STOP#	59	STS	Stop# indicates the current target is requesting the master to stop the current transaction. As a slave, the 82557 drives STOP# to inform the bus master to stop the current transaction. As a bus master, the 82557 receives STOP# from the slave and stops the current transaction.
IDSEL	34	IN	Initialization Device Select is used by the 82557 as a chip select during configuration read and write transactions.

Symbol	Pin	Type	Name and Function
DEVSEL#	56	STS	Device Select#, when actively driven by the 82557 as a slave, indicates to the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

2.1.4. ERROR REPORTING PINS

Symbol	Pin	Type	Name and Function
SERR#	60	OD	System Error# is used by the 82557 to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR#	61	STS	Parity Error# is used by the 82557 for reporting data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the 82557 after receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected.

2.1.5. INTERRUPT PIN

Symbol	Pin	Type	Name and Function
INTA#	18	OD	Interrupt A# is used to request an interrupt by the 82557. This is an active low, level-triggered interrupt signal.

2.1.6. ARBITRATION PINS

Symbol	Pin	Type	Name and Function
REQ#	15	TS	Request# indicates to the arbiter that the 82557 desires use of the bus. This is a point-to-point signal. Every master has its own REQ#.
GNT#	14	IN	Grant# indicates to the 82557 that access to the bus has been granted. This is a point to point signal.

2.1.7. SYSTEM PINS

Symbol	Pin	Type	Name and Function
CLK	25	IN	Clock provides timing for all transactions on the PCI bus and is an input to the 82557. All other PCI signals, except RST# and the INT# lines are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge.

Symbol	Pin	Type	Name and Function
RST#	13	IN	Reset# is used to bring PCI-specific registers, sequencers and signals to a consistent state. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be tri-stated. SERR# (open drain) is floated. To prevent AD, C/BE# and PAR signals from floating during reset, the central device may drive these lines during reset (bus parking) only to a logic low level; they may not be driven high.

2.2. Local Memory Interface

Symbol	Pin	Type	Name and Function
EECS	138	OUT	EEPROM Chip Select. Used to assert chip select to the serial EEPROM. EECS is active-high.
FLD0EESK	135	TS	Multiplexed pin. During flash access, this pin acts as FLASH Data 0 input/output. During EEPROM access it acts as EEPROM SHIFT CLOCK output to shift data into and out of the serial EEPROM.
FLD1EEDO	134	TS	Multiplexed pin. During flash access, this pin acts as FLASH Data 1 input/output. During EEPROM access, this pin acts as the input EEPROM DATA OUT.
FLD2EEDI	133	TS	Multiplexed pin. During flash access, this pin acts as FLASH Data 2 input/output. During EEPROM access, this pin acts as the output EEPROM DATA IN.
FLD3 FLD4 FLD5 FLD6 FLD7	130 129 128 127 124	TS	FLASH Data 7 to 3 input/outputs.
FLADDR0 FLADDR1 FLADDR2 FLADDR3 FLADDR4 FLADDR5 FLADDR6 FLADDR7 FLADDR8 FLADDR9 FLADDR10 FLADDR11	123 120 119 118 115 114 109 108 107 104 103 102	OUT	FLASH Address 11 to 0 work in conjunction with an external 8-bit Address Latch to control the FLASH addressing up to 1Mbyte. The 8 most significant FLASH address pins (FLADDR11 to 4) should be connected to both the Address Latch and to Address Pins 11 to 4 of the FLASH. The Address Latch provides the upper 8-bits, 19 to 12, of address to the FLASH and is loaded by assertion of the FLCS# pin.

Symbol	Pin	Type	Name and Function
FLCS#	96	OUT	FLASH Chip Select will normally be high to disable access to the FLASH. Whenever a FLASH high address is to be latched, FLCS# will go low, thus latching the data in the latch and enabling the FLASH. FLCS# should be connected to both the ENABLE pin on the external address latch and the CE# pin on the FLASH.
FLOE#	98	OUT	FLASH Output Enable provides the active low Output Enable control to the FLASH.
FLWE#	101	OUT	FLASH Write Enable provides the active low Write Enable control to the FLASH.

2.3. Serial Interface Pins

Symbol	Pin	Type	Name and Function
RXCLK	151	IN	Receive Clock operates at either 25 MHz, 2.5 MHz (MII Mode), or 10 MHz (10 Mbps-only mode).
RXD0 RXD1 RXD2 RXD3	150 149 148 147	IN	Receive Data 0 - 3: nibble-wide data inputs in MII mode. In 10 Mbps only mode, RXD0 is the serial receive data input.
RXDV	153	IN	Receive Data Valid indicates that valid data is present on the RXD lines. This is used for MII mode only. When this pin is inactive (low), receive data is not sampled by the 82557.
RXER	152	IN	Receive Data Error indicates that an invalid symbol has been detected inside a receive packet. This is used in MII mode only.
RXCONG	1	OUT	Receive Congestion is used in duplex mode and is asserted when the receive FIFO is full and unable to accept any more data packets. Please refer to the National Semiconductor Corporation PHY implementation.
CRS	155	IN	Carrier Sense indicates traffic on the wire.
TXCLK	8	IN	Transmit Clock operates at either 25 MHz, 2.5 MHz (MII Mode), or 10 MHz (10 Mbps only mode).
TXD0 TXD1 TXD2 TXD3	7 6 3 2	OUT	Transmit Data 0 - 3 nibble wide transmit data outputs in MII mode. In 10 Mbps only mode TXD0 is the serial transmit data output.
RTS/TXEN	158	OUT	Request To Send indicates that the 82557 has a frame pending for transmission (10 Mbps-only mode) Transmit Enable indicates that the 82557 is transferring data to the PHY (MII mode).
COL	154	IN	Collision Detect indicates a collision has been detected on the wire. In Full Duplex mode, assertion of COL indicates a Congestion condition has occurred.

Symbol	Pin	Type	Name and Function
TXRDY	144	IN	Transmit Ready is used in duplex mode for flow control. Please refer to the National Semiconductor Corporation PHY implementation.
RSTOUT	146	OUT	Reset Out signal to the PHY is driven high during H/W reset of the 82557.
LPBCK	145	OUT	Loopback controls the PHY into loopback mode.
FDX#	143	IN	Full Duplex is an input from the physical layer component indicating if it has switched into or out of full duplex mode. FDX# is active low.
FULHAL	6	OUT	Full/Half Duplex. When active, indicates 82557 is in full duplex mode. This pin is multiplexed with the TXD1 pin and operates only when in 10 Mbps-only mode.
MDIO	156	TS	Management Data Input/Output is a bi-directional signal between the 82557 and an MII-compatible PHY. It is used to transfer control and status information between the 82557 and the PHY. Control information is driven by the 82557 on the MDIO synchronously to MDC and sampled synchronously by the PHY. Status information is driven synchronously by the PHY and sampled synchronously by 82557.
MDC	157	OUT	Management Data Clock provides timing reference for transfer of control information and status on the MDIO signal. The frequency of this clock is up to 2.5 MHz.

2.4. Power and Ground

Symbol	Pin	Type	Name and Function
V_{CC}	4, 9, 12, 16, 21, 28, 32, 37, 42, 45, 51, 57, 63, 69, 75, 79, 83, 88, 92, 97, 100, 106, 110, 113, 117,122, 126, 132, 137, 159	In	Power: +5V ± 5%.
V_{SS}	5, 10, 11, 17, 22, 29, 33, 38, 41, 46, 52, 58, 64, 70, 76, 80, 84, 87, 91, 95, 99, 105, 111, 112, 116, 121, 125, 131, 136, 160	In	Ground: 0V.

2.5. Test Access Port (TAP)

The 82557 Test Access Port consists of four pins: TI, TOUT, TCK, and TEXEC. The following table summarizes the signal descriptions for these pins. For more information about the TAP, refer *to Application Note 375.*

Symbol	Pin	Type	Name and Function
TI	142	I	Test Input port is a serial input of test command data.
TOUT	141	O	Test Output port is a serial output of test com-mand data. TOUT is determined according to the last test command executed.
TCK	140	I	Test Input Clock. The clock of the test access port logic. TI data is sampled into the test command logic.
TEXEC	139	I	Load Instruction Test Register. Issues the new test command when asserted. The command is loaded serially via the TI input and then sam-pled to the Instruction Test Register.

3.0. 82557 ARCHITECTURE OVERVIEW

The figure on the cover shows a high level block diagram of the 82557 part. It is divided into three main subsystems: a parallel subsystem, a FIFO subsystem and the 10/100 Mbps CSMA/CD unit.

3.1. Parallel Subsystem Overview

The parallel subsystem is broken down into several functional blocks: a PCI Bus Master Interface, a Micro Machine processing unit and its corresponding microcode ROM, and a PCI Target Control/FLASH/EEPROM interface. The parallel subsystem also interfaces to the FIFO subsystem, passing data (XMT, RCV and Configuration), command and status parameters between these two blocks.

The PCI Bus Master Interface provides a complete interface to a PCI bus and is compliant with revision 2.1 of the PCI Bus Specification. No external logic is required to interface the 82557 to a PCI bus. The 82557 provides 32 bits of addressing and data, as well as the complete control interface to operate on a PCI bus. As a PCI target, it follows the PCI Configuration format which allows all accesses to the 82557 (control register, FLASH accesses, boot, etc.) to be automatically mapped into free memory and I/O space upon initialization of a PCI system. For processing of XMT and RCV frames, the 82557 operates as a master on the PCI bus, initiating zero wait state transfers for accessing these data parameters.

The PCI Bus Master Interface consists of three units. The Bus Interface Unit (BIU) controls the access to the PCI bus according to the bus protocol. The BIU controls such actions as initiating when to request or relinquish the external PCI bus and handles internal direct memory access (DMA) channel arbitration. The Data Interface Unit (DIU) routes data into and out of the 82557 at high speed data transfers. The DMA unit controls the addressing for four separate DMA channels.

The 82557 Control/Status Register Block is contained as part of the PCI target element. The Control/Status Register Block consists of the following 82557 internal control registers: System Control Block (SCB), PORT, FLASH control register, EEPROM control register and Management Data Interface (MDI) Control register. Refer to the 82557 User's Manual for more information on the Control/Status Register Block.

The Micro Machine is an embedded processing unit contained in the 82557. The Micro Machine accesses the 82557 microcode ROM working its way through the op-codes (or instructions) contained in the ROM to perform its functions. Parameters accessed from memory such as Transmit Buffer Descriptor fields or pointers to data buffers are also used by the micro machine during processing of RCV or XMT frames by the 82557. A typical function of the Micro Machine would be to take a data buffer pointer field and load it into the 82557 DMA unit for direct access to the data buffer. The Micro Machine is divided into two units, a Receive Unit and a Command Unit (including XMT functions). These two units operate independently and concurrently. Control is switched between the two units according to the microcode instruction flow.

The independence of the Receive and Command units of the Micro Machine allows the 82557 to execute commands and receive incoming frames simultaneously, with no real-time CPU intervention.

The 82557 contains an interface to both an external FLASH memory and an external serial EEPROM. The FLASH interface, which could also be used to connect to any standard 8-bit EPROM device, provides up to 1 Mbyte of addressing to the FLASH. It utilizes a multiplexed address scheme that works in conjunction with an LS373 or compatible latch to de-multiplex the address. Without the latch, up to 16 Kbytes can be addressed. Both Read and Write accesses are supported. The FLASH may be used for remote boot functions, network statistical and diagnostics functions, etc. The FLASH is mapped into host system memory (anywhere within the 32-bit memory address space) for software accesses. It is also mapped into an available boot expansion ROM location during boot time of the system. For more information on the FLASH interface, see Section 4.1.3. The EEPROM is used to store relevant information for a LAN connection such as Node Individual Address, as well as board manufacturing and configuration information. Both Read and Write accesses to the EEPROM are supported by the 82557. For more information on the EEPROM interface, see Section 4.1.3.

3.2. FIFO Subsystem Overview

The 82557 FIFO subsystem consists of a 3 Kbyte transmit FIFO and 3 Kbyte receive FIFO. Each FIFO is unidirectional and independent of the other. The FIFO subsystem serves as the interface between the 82557 parallel side and the serial CSMA/CD unit. It provides a temporary buffer storage area for frames as they are either being received or transmitted by the 82557. This allows for several important features in the 82557:

- Transmit frames can be queued within the XMT FIFO, allowing back to back transmission within the minimum Inter Frame Spacing (IFS)
- The storage area in the FIFO area allows the 82557 to withstand long PCI Bus latencies without losing incoming data or corrupting outgoing data.
- The 82557 XMT FIFO Threshold allows the transmit start threshold to be tuned to eliminate underruns while concurrent transmits are being performed.
- The FIFO subsection allows extended PCI 0 Wait State burst accesses to or from the 82557 for both RCV and XMT frames, since the transfer is to the FIFO storage area as opposed to directly to the serial link.
- Transmissions resulting in errors (CDT, Underrun) are retransmitted directly from the 82557 FIFO, increasing performance and eliminating the need to reaccess this data from the host system.
- Incoming Runt RCV Frames (less than the legal minimum frame size) can be discarded automatically by the 82557 without transferring this faulty data to the host system.

3.3. 10/100 Mbps Serial CSMA/CD Unit Overview

The CSMA/CD unit of the 82557 allows it to be connected to either a 10 or 100 Mbps Ethernet network. The 82557 interfaces to either an IEEE 802.3 10/100 Mbps MII compatible PHY device or a 10 Mbps-only IEEE 802.3 PHY. In the case of the MII compatible PHY, the 82557 can switch automatically between 10 or 100 Mbps operation depending on the speed of the network. The CSMA/CD unit performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc. The CSMA/CD unit can also be placed in a Full Duplex mode which allows for simultaneous transmission and reception of frames. The CSMA/CD unit accepts data from the 82557 XMT FIFO and converts it to either serial or nibble-wide (MII Compatible mode) data for transmission on the link. During reception, the CSMA/CD unit converts data from either serial or nibble-wide data to a byte-wide format and transfers it to the RCV FIFO of the 82557. The CSMA/CD unit contains a Management Data Interface (MDI) to an MII compliant PHY. This allows control and status parameters to be passed between the 82557 and the PHY (parameters specified by software) by one serial pin and a clocking pin, reducing the number of control pins needed for PHY mode control.

4.0. THE 82557 HARDWARE INTERFACE

4.1. PCI Bus Interface

The PCI bus interface enables the 82557 to interact with the host system via the PCI bus. It provides the control, address and data interface to implement a PCI compliant device. The 82557 operates as both a master and slave on the PCI bus. As a master, the 82557 interacts with the system main memory to access data for transmission or deposit received data.

As a slave, some 82557 control structures are accessed by the host CPU which reads or writes to these on-chip registers. The CPU provides the 82557 with the necessary action commands, control commands and pointers which enable the 82557 to process RCV and XMT data. The PCI bus interface also provides the means for configuring PCI parameters in the 82557. Refer to the *PCI Bus Interface Specification* for more details specific to the PCI bus.

4.1.1. PCI CONFIGURATION

The configuration process in a PCI system starts before anything else. The 82557 is actually disconnected from the PCI bus until it is configured. At this stage it responds to configuration cycles only. This subsection provides a detailed description of the PCI configuration process from software and hardware points of view. Specifically, it defines the programming model and usage rules for the configuration register space of the 82557.

The 82557 supports all mandatory required registers along with specific registers that are needed for its operation. Mainly, it implements several Base Address registers. These registers and their purpose will be described in detail later on. For more concise information refer to the *PCI System Design Guide.*

4.1.1.1. PCI Configuration Space Organization

The organization of configuration space registers as defined in the PCI specification is shown Table 1. This region consists of fields that uniquely identify the 82557 and allow it to be generically controlled. The This region consists of fields that uniquely identify the 82557 treats configuration space write operations to reserved registers as no-ops (the data written is ignored). Read accesses to reserved or undefined registers will always return a data value of all zeros. For all accesses to the PCI Configuration Registers, the 82557 will disconnect from the bus following each access. In other words, no burst accesses may be made to these registers.

Table 1 shows the layout of the 64 byte predefined header portion of the 256-byte configuration space that every PCI device must support. These registers are known as the PCI Configuration Registers in the 82557. Devices must place any necessary device specific registers only in locations 64 through 255. Currently, the 82557 does not implement any register beyond the 64 byte predefined header portion. All multibyte numeric fields follow *little-endian* ordering. That is, lower addresses contain the least significant parts of the field. Software must take care to deal correctly with bit-encoded fields that have some bits reserved for future use.

On reads, software must use appropriate masks to extract the defined bits, and may not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and the data then written back. Section 4.1.2 describes the registers in the predefined header portion of the configuration space. It also specifies which registers are reserved and which ones are implemented.

The predefined header portion of the configuration space is divided into two parts. The first 16 bytes are defined the same for all types of PCI compliant devices. The 82557 B-step, as a PCI compliant device, supports the Vendor ID, Device ID, Command and Status fields in the header. The C-step (available in March 1997) will also include the Sub-vendor ID and Device ID. Implementation of the other registers is optional (i.e., they can be treated as reserved registers). The specific implementation of these resisters in the 82557 is described in Section 4.1.2.

Table 1. PCI Configuration Registers

Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
CSR Mem Mapped Base Addr Register				10h
CSR I/O Mapped Base Addr Register				14h
Flash Mem Mapped Base Addr Register				18h
Reserved Base Addr Register				1Ch
Reserved Base Addr Register				20h
Reserved Base Addr Register				24h
Reserved				28h
SubSystem ID		SubSystem Vendor ID		2Ch
Expansion ROM Base Addr				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

4.1.1.2. PCI Configuration Registers

This section lists and describes all PCI registers defined in the predefined header portion of the configuration space that are supported and implemented in the 82557. All reserved registers are also specified.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions. Its use should be restricted to initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers. The PCI configuration registers are described while partitioned into several groups according to their functionality.

Device Identification Registers

Five fields (seven in the C-step part) in the predefined header deal with device identification. The 82557, as a PCI compliant device, implements them as required. These registers (fields) enable generic configuration software to easily determine what devices are available on the system's PCI bus. All of these registers are read-only. The description of their functionality and their assigned value in the 82557 is given in Table 2. Their location (offset) in the PCI configuration space is given in Table 1.

Table 2. Device Identification Registers

Register	Description
Vendor ID	This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. The vendor ID value for the 82557 is always 8086 and is read-only.
Device ID	This field identifies the particular device. This identifier is allocated by the vendor. The device ID for the 82557 is 1229 and is read-only.
Revision ID	This read-only register specifies the 82557 stepping.
Header Type	This byte identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. The 82557 Header Type of 00h specifies the layout shown in Figure 3 and indicates a single function device. This field is read-only.
Class Code	The Class Code register is read-only and is used to identify the generic function of the device and (in some cases) a specific register-level programming interface. The register is broken into three byte-size fields. The upper byte, 02h is a base class code and specifies the 82557 as a Network Controller. The middle byte is a sub-class code, 00h which specifies Ethernet Controller. The lower byte identifies a specific register-level programming interface and the 82557 always returns 00h in this field.

PCI Command Register

The PCI Command Register (04h) provides control over the 82557's ability to generate and respond to PCI cycles. When a 0 is written to this register, the 82557 is logically disconnected from the PCI bus for all accesses except configuration accesses. Figure 2 shows the layout of the register and Table 3 explains the meanings of the different bits in the Command register. Table 3 also gives the default value of this register upon power up and the specific implementation of individual bits in the 82557 (i.e., R/O or R/W).

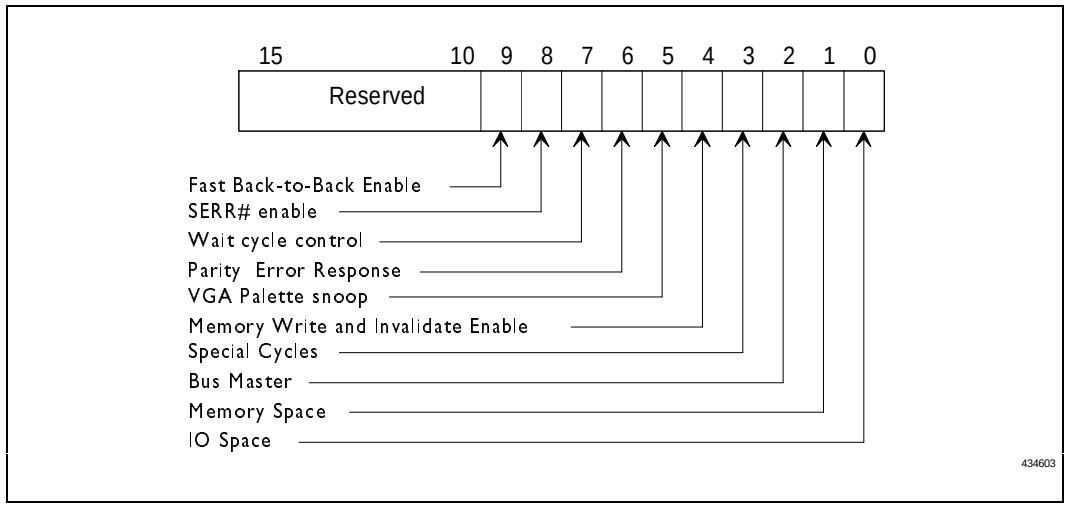

Figure 2. PCI Command Register Layout

Table 3. PCI Command Register Bits

Bit #	Bit Name	Description
0	IO Space	This bit controls a device's response to I/O space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O space accesses. The specific implementation of this bit in the 82557 is configurable with default value 0 .
1	Mem Space	This bit controls a device's response to memory space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to memory space accesses. This bit is configurable in the 82557 with a default value 0.
2	Bus Master	This bit controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. This bit is configurable in the 82557 with a default value 0.
3	Special Cycle	This bit controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. This bit is always set to 0 in the 82557.
4	Mem WR & Invalidate En	This is an enable bit for using the Memory Write and Invalidate command. This bit is always set to 0 in the 82557 (disabled).
5	VGA Palette Snoop	This bit controls how VGA compatible devices handle accesses to their palette registers. This bit is always set to a 0 in the 82557 (disabled).
6	Parity Error Response	This bit controls the 82557's response to parity errors. When the bit is set, the 82557 takes its normal action when a parity error is detected. When the bit is reset, the 82557 ignores any parity errors that it detects and continues normal operation. This bit must be set to 0 after RST#. This bit is configurable in the 82557 with a default value 0.
7	Wait Cycle Control	This bit, when set to a 1, is used to control whether or not a device does address/data stepping. This bit is always set to 0 in the 82557 (disabled).
8	Serr Enable	This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. This bit (and bit 6, PERR# Enable) must be on to report address parity errors. This bit is configurable in the 82557 with a default value of 0.
9	Fast Back to Back Enable	This bit controls whether or not a master can do fast back-to-back transactions to different devices. This bit is set to a 0 in the 82557, fast back-to-back transactions are only allowed to the same agent.
10-15	Reserved	Reserved. These bits are hardwired to 0 in the 82557.

PCI Status Register

The PCI Status Register is used to record status information for PCI bus related events. The definition of each of the bits is given in Table 4 and the layout of the register is shown in Figure 3. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

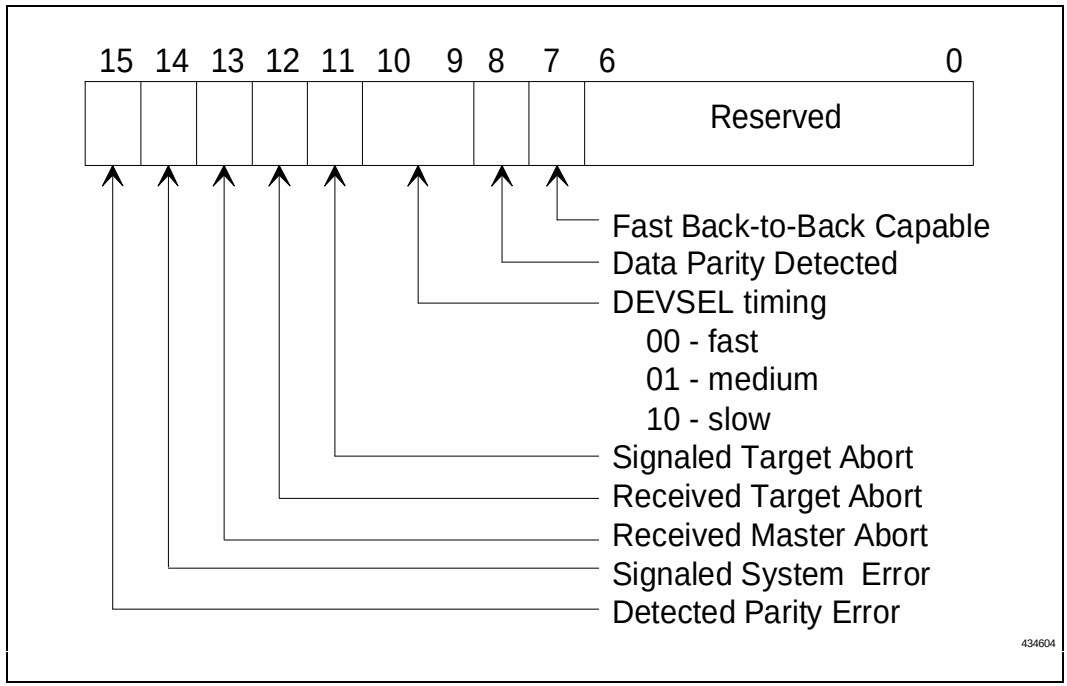

Figure 3. PCI Status Register Layout

Table 4. PCI Status Register Bits

Bit #	Bit Location	Description
0-6	Reserved	These bits are hardwired to 0 in the 82557.
7	Fast Back to Back Capable	This read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. The value of this bit in the 82557 is 1 (Fast Back to Back Capable).
8	Data Parity Detected	This bit is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; 3) the Parity Error Response bit (Command Register) is set. The initial value of this bit in the 82557 is 0.
9-10	DEVSEL# Timing	These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL#. These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). The value of these bits are always set to 01 (medium).
11	Signaled Target Abort	This bit must be set by a target device whenever it terminates a transaction with target-abort. The value of this bit is always 0.
12	Received Target Abort	This bit must be set by a master device whenever its transaction is terminated with target-abort. The initial value of this bit in the 82557 is 0.
13	Received MasterAbort	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with master-abort. The initial value of this bit in the 82557 is 0.
14	Signaled SystemError	This bit must be set whenever the device asserts SERR#. The initial value of this bit in the 82557 is 0.
15	Detected Parity Error	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register). The initial value of this bit in the 82557 is 0.

Miscellaneous PCI Configuration Registers

This section describes the registers that are device independent and only need to be implemented by devices that provide the described function. The specific implementation of each register for the 82557 is provided in Table 5.

Table 5. Miscellaneous PCI Configuration Bits

Register	Description
Cache Line Size	This register is not implemented in the 82557. The value of this field is fixed to 0.
Latency Timer	The 82557, as a master device, implements this register to limit the size of very long burst cycles. The initial value is 0 and is then programmed by system BIOS at initialization time.
Built-in Self Test (BIST)	This optional register is used for control and status of BIST. The 82557 will not provide PCI BIST and the value of this field is always set to 0.
Interrupt Line	The Interrupt Line register is an 8-bit register used to communicate interrupt line routing information. This register is configurable in the 82557. POST software will write the routing information into this register as it initializes and configures the system. The value in this register defines which input of the system interrupt controller(s) the device's interrupt pin is connected to. Device drivers and operating systems can then use this information to determine priority and vector information.
Interrupt Pin	The Interrupt Pin register tells which interrupt pin the device (or device function) uses. This eight bit register is always set to a 1 in the 82557, indicating INTA# is used.
MIN_GNT/ MAX_LAT	These read-only byte registers are used to specify the devices desired settings for Latency Timer values. For both registers, the value specifies a period of time in units of ¼ microsecond. MIN_GNT is used for specifying how long a burst period the device needs assuming a clock rate of 33 MHz. MAX_LAT is used for specifying how often the device needs to gain access to the PCI bus. The values of these registers are 8h (2 microseconds) for MIN_GNT and 38h (14 microseconds) for MAX_LAT.

Base Address Registers

One of the most important functions for enabling superior configurability and ease of use is the ability to relocate PCI devices in the address spaces. At system power-up device independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM.

The 82557 contains three Base Address Registers (BAR), two requesting memory mapped resources and one requesting I/O mapping. Each register is 32-bits wide. The least significant bit in BAR determines whether it represents an I/O or memory space. Figure 4 and Figure 5 show the layout of a BAR for both I/O and memory mapping. After determining this information, power-up software can map the I/O and memory controllers into available locations and proceed with system boot. In order to do this mapping in a device independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space. Device drivers can then access this configuration space to determine the mapping of a particular device.

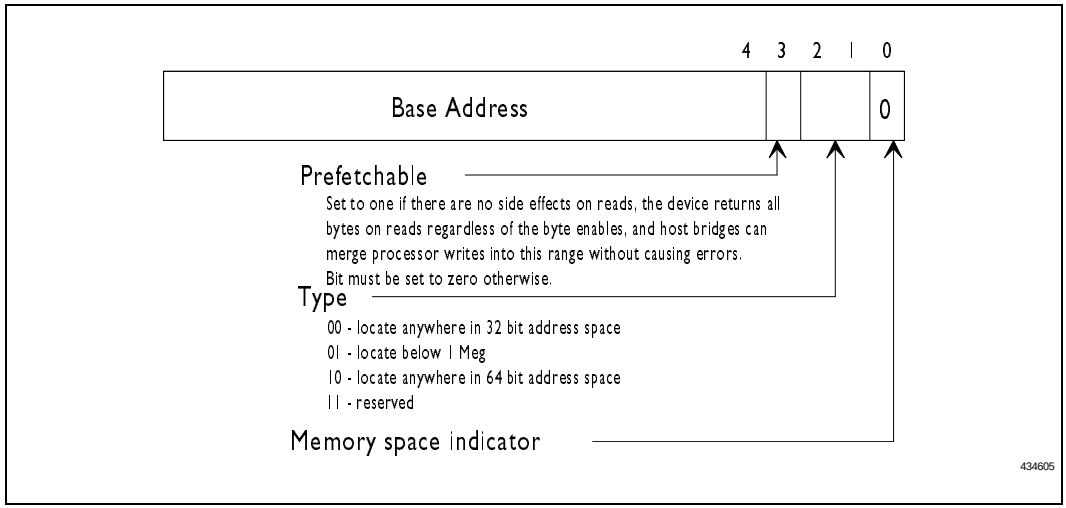

Figure 4. Base Address Register for Memory Mapping

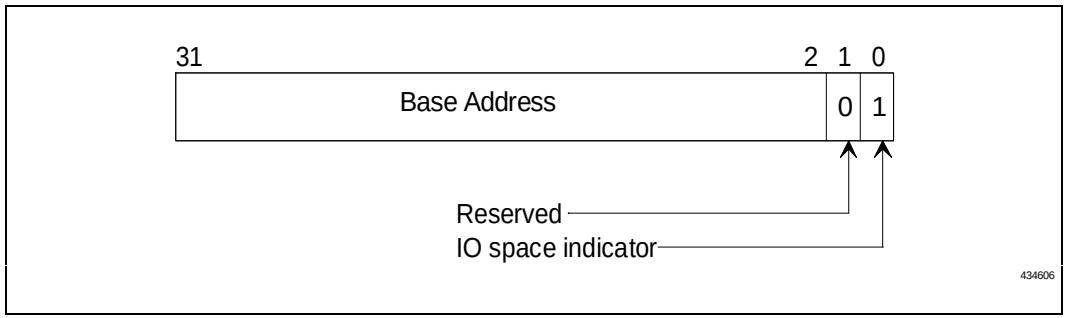

Figure 5. Base Address Register for I/O

Bit 0 in all base registers is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a 0 in bit 0. Base registers that map to I/O space must return a 1 in bit 0.

Base registers that map into I/O space are always 32 bits with bit 0 hardwired to a 1, bit 1 is reserved and must return 0 on reads, and the other bits are used to map the device into I/O space.

The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For example, a device that wants a 1 Mbyte memory address space would set the most significant 12 bits of the base address register to be configurable, setting the other bits to 0.

For its Control/Status Registers (CSR), the 82557 requires one Base Address Register to I/O Map these registers, and one Base Address Register to Memory Map these registers anywhere within the 32-bit memory address space. It is up to the software driver to determine which Base Address Register (I/O or Memory) to use to access the 82557 Control/Status registers. Both are always requested by the 82557. The 82557 requires one Base Address Register to map the accesses to an optional FLASH memory. The size of the space requested is 1 Mbyte, and it is always mapped anywhere in the 32-bit memory address space. Table 6 describes the implementation of the Base Address Registers in the 82557.

Table 6. 82557 Base Address Registers

Register Location	Description
10h	Memory space for the 82557 Control/Status Registers. The size of this space is 4 Kbytes. It will be marked as a prefetchable space and is mapped anywhere in the 32-bit memory address space.
14h	I/O space for 82557 Control/Status Registers. The size of this space is 32 bytes.
18h	Memory space for the 82557 flash buffer for accesses above 1 Mbyte. The size of this space is 1 Mbyte. It will be marked as a non-prefetchable space and is mapped anywhere in the 32-bit address space.
1C-27h	Reserved. 82557 returns 0.

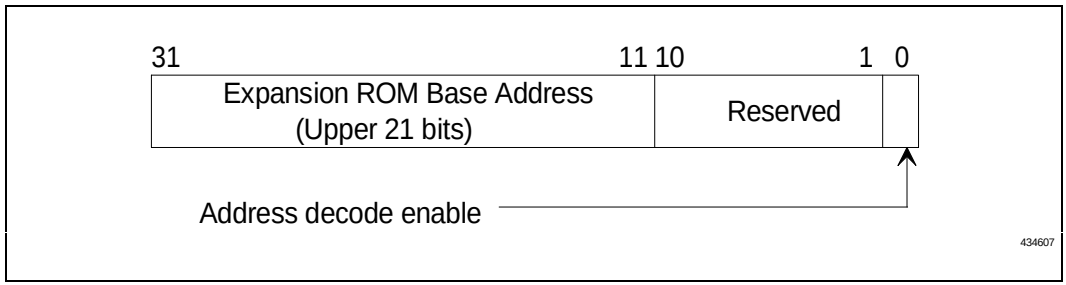

Figure 6. Expansion ROM Base Address Register Layout

Table 7. 82557 Expansion ROM Base Address Register Format

31 20	19 1	0
Read/Write	Reserved (all 0's)	En

Expansion ROM Base Address Register

The 82557 provides an interface to a local FLASH (or EPROM) which can be used as an expansion ROM. A 32-bit Expansion ROM Base Address Register at offset 30h in the configuration space is defined to handle the address and size information for boot-time access to the FLASH. Figure 6 shows how this register is organized. The register functions exactly like a 32-bit Base Address register except that the encoding (and usage) of the bottom bits is different. (The upper 21 bits correspond to the upper 21 bits of the Expansion ROM base address.) The 82557 allows its Expansion ROM to be mapped on any 1Mbyte boundary. The most significant 12 bits are configurable to indicate the 1Mbyte size requirement.

Bit 0 in the register is used to control whether or not the device accepts accesses to its expansion ROM. When this bit is reset, the devices Expansion ROM address space is disabled. This bit is programmed at initialization time by the system BIOS. The Memory Space bit in the Command register has precedence over the Expansion ROM enable bit. A device responds to accesses to its expansion ROM only if both the Memory Space bit and the Expansion ROM Base Address Enable bit are set to 1 (it is reset to 0 on Reset).

PCI Configuration Cycles

As already mentioned, the PCI definition provides for totally software driven initialization and configuration via a separate configuration address space. This section provides a description of the PCI commands for accessing the PCI configuration space. For more concise information please refer to the latest revision of the *PCI Local Bus Specification.*

For normal accesses (i.e., memory or I/O), each device decodes its own addresses. In configuration accesses, the device selection decoding is done externally, and signaled to the PCI device via the IDSEL pin. The 82557 becomes the target of a configuration command (RD or WR) only if its IDSEL is asserted and AD0-1 are 00 during the address phase of the command. The addressed register in the configuration space is determined by AD2-7 and BE0-3# lines. The 82557 will support non-burst configuration accesses of a BYTE, WORD, or DWORD. Read and Write configuration cycles are shown in Figure 7 and Figure 8 respectively.

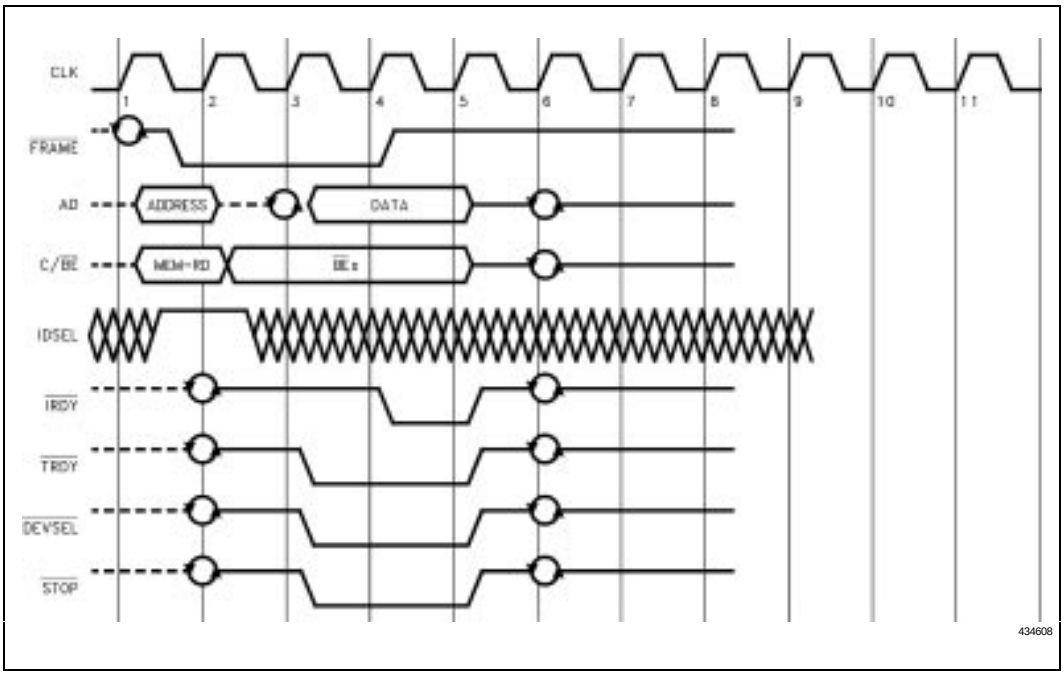

Figure 7. Configuration Read Cycle

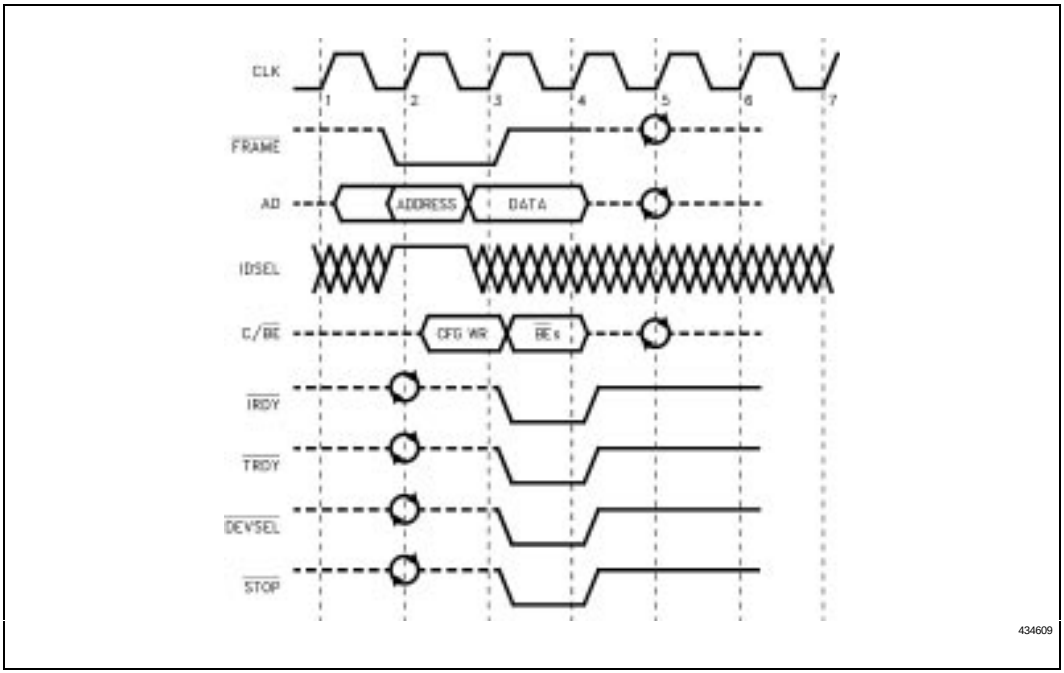

Figure 8. Configuration Write Cycle

4.1.2. 82557 BUS OPERATIONS

4.1.2.1. General Overview

After configuration, the 82557 is ready for its normal operation. As a Fast Ethernet Controller, the role of the 82557 is to access transmitted data or deposit received data. In both cases the 82557, as a bus master device, will initiate memory cycles via the PCI bus to fetch/deposit the required data.

In order to perform these actions, the 82557 is controlled and examined by the CPU via its control and status structures and registers. Some of these control and status structures reside on chip and some reside in system memory. For access to its Control/Status Registers (CSR), the 82557 serves as a slave (target). The 82557 serves as a slave also while the CPU accesses its 1 Mbyte Flash buffer or its EEPROM. The next subsection describes the 82557 slave operation. It is followed by a description of the 82557 operation as a bus master (initiator).

82557 Slave Bus Operation

The 82557 serves as a Slave in one of the following cases:

- CPU accesses to the 82557 SCB control and status structures (CSR).
- CPU accesses to the EEPROM through its control register (CSR).
- CPU accesses to the 82557 PORT address (CSR).
- CPU accesses to the MDI control register (CSR).
- CPU accesses to the FLASH control register (CSR)
- CPU accesses to the 1 Mbyte FLASH

The CSR and the 1 Mbyte Flash buffer are considered by the 82557 as two totally separated memory spaces. The 82557 provides separate Base Address Registers in the configuration space to

distinguish between them. The size of the control and status registers memory space is 32 bytes in the I/O space and 4 Kbytes in the memory space. The 82557 treats accesses to these memory spaces differently. For more information, refer to the *82557 User's Manual*.

Control/Status Registers (CSR) Accesses

The 82557 supports zero wait state single cycle I/O or memory mapped accesses to its CSR space. Separate base address registers request 32 bytes of both memory and I/O space to accomplish this. Based on its needs, the software driver will use either I/O or memory mapping to access these registers.

The 82557 provides 32 valid bytes of CSR, which include the following elements:

1. SCB.
2. PORT.
3. FLASH control register.
4. EEPROM control register.
5. MDI Control register.

Figure 9 and Figure 10 show CSR read and write cycles. They show general zero wait state I/O read and write cycles. In the case of accessing the Control and Status structures, the CPU is the initiator and the 82557 is the target of the transaction.

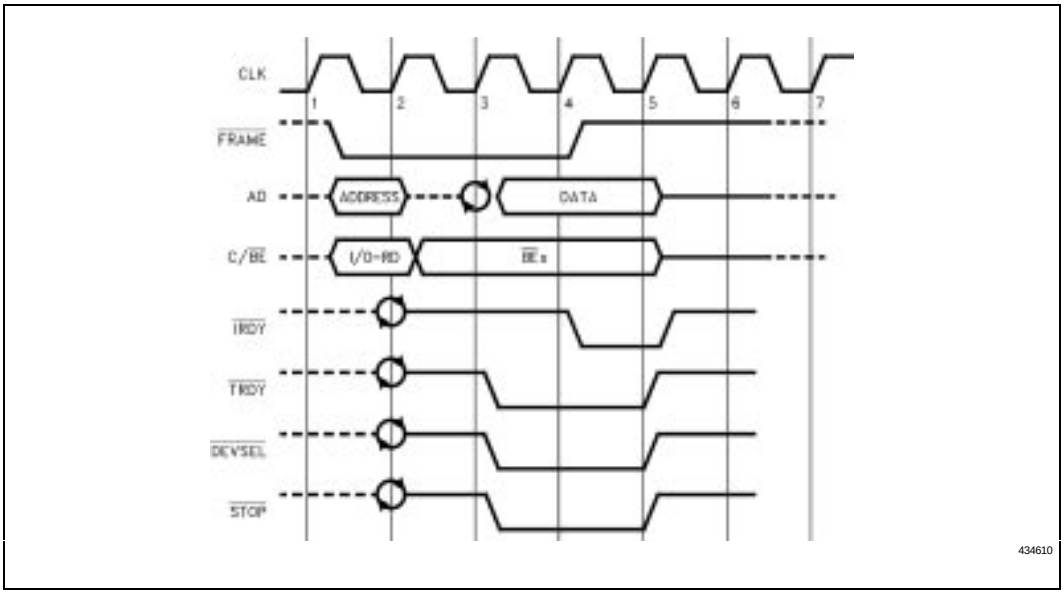

Figure 9. CSR Read Cycles

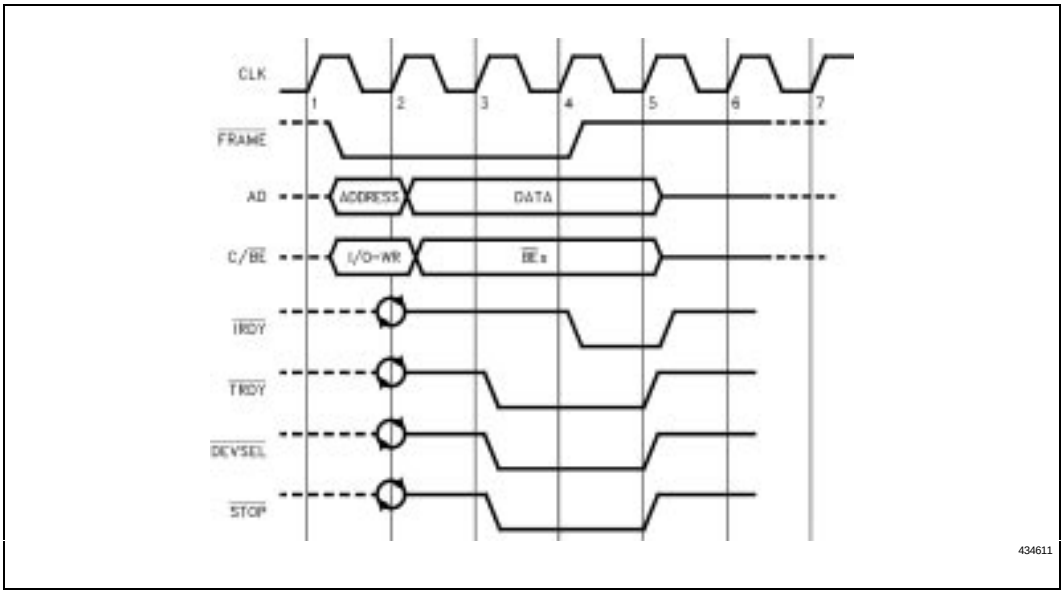

Figure 10. CSR Write Cycle

Read Accesses: The CPU, as the initiator, drives the address lines AD0-31, the command and byte enable lines C/BE0-3# and the control lines IRDY# and FRAME#. As a slave, the 82557 controls the TRDY# signal and provides valid data on each data access. The 82557 allows the CPU to issue only one read cycle when it accesses the Control and Status registers, generating a disconnect by asserting the STOP# signal. The CPU can insert wait states by deasserting IRDY# when it is not ready.

Write Accesses: The CPU, as the initiator, drives the address lines AD0-31, the command and byte enable lines C/BE0-3# and the control lines IRDY# and FRAME#. It also provides the 82557 with valid data on each data access immediately after asserting IRDY#. The 82557 controls the TRDY# signal and asserts it from the data access. As for read cycles, the 82557 allows the CPU to issue only one I/O write cycle to the Control & Status registers, generating a disconnect by asserting the STOP# signal. This is true for both memory mapped and I/O mapped accesses.

FLASH Buffer Accesses

The CPU accesses to the Flash Buffer are very slow. For this reason the 82557 issues a *target-disconnect* at the first data access. The 82557 asserts the STOP# signal to indicate a *target-disconnect*. Figures 14 and 15 show memory CPU read and write accesses to the 1 Mbyte Flash Buffer. The longest Burst cycle to the Flash Buffer contains one data access only.

Read Accesses: The CPU, as the initiator, drives the address lines AD0-31, the command and byte enable lines C/BE0-3# and the control lines IRDY# and FRAME#. The 82557 controls the TRDY# signal and deassrets it for a certain number of clocks until valid data can be read from the Flash Buffer. When TRDY# is asserted, the 82557 drives valid data on the AD0-31 lines. The CPU can also insert wait states by deasserting IRDY# until it is ready. Flash buffer read accesses can be byte or word length. See NOTE in section 4.2.1.1 for additional information.

Write Accesses: The CPU, as the initiator, drives the address lines AD0-31, the command and byte enable lines C/BE0-3# and the control lines IRDY# and FRAME#. It also provides the 82557 with valid data immediately after asserting IRDY#. The 82557 controls the TRDY# signal and deasserts it for a certain number of clocks until valid data is written to the Flash Buffer. By asserting TRDY#, the 82557 signals the CPU that the current data access is completed. Flash buffer write accesses can be byte length only. See NOTE in section 4.2.1.1 for additional information.

Error Handling

Data Parity Errors: The 82557 checks for data parity errors while it is the target of the transaction. If an error was detected, the 82557 always sets the Detected Parity Error bit (PCI Status Register, bit 15). The 82557 also asserts PERR#, if the Parity Error Response bit is set (PCI Command Register, bit 6). The 82557 does not attempt to terminate a cycle in which a parity error was detected. This gives the initiator of the access, at each hardware or software level, the option of recovery.

Target-Disconnect: The 82557 will use premature termination in the following cases:

- After accesses to the 1 Mbyte Flash buffer.
- After accesses to its CSR
- After accesses to the configuration space

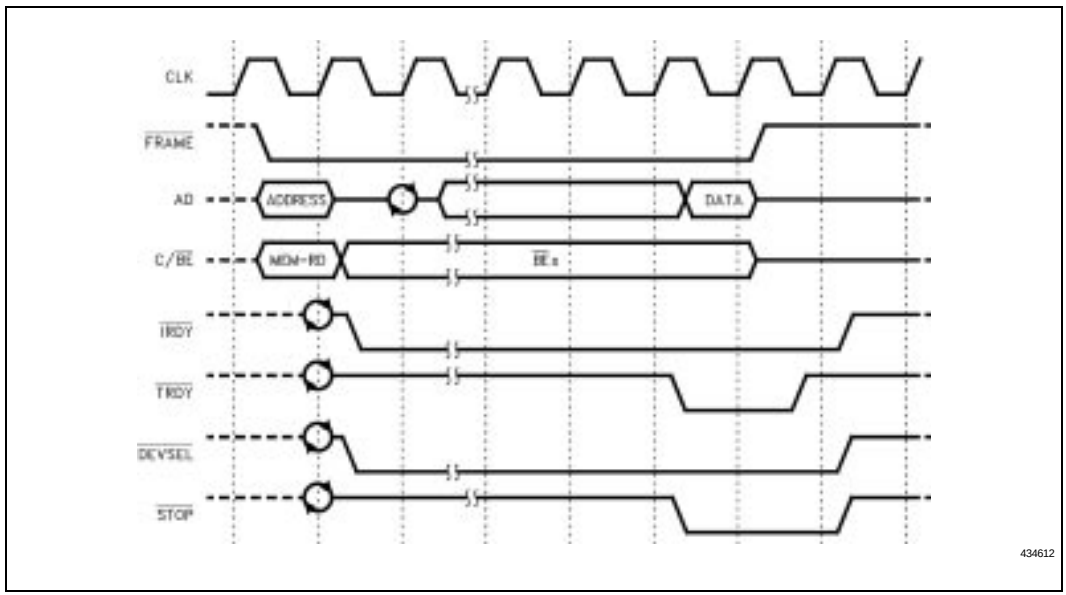

Figure 11. Flash Buffer Read Cycles

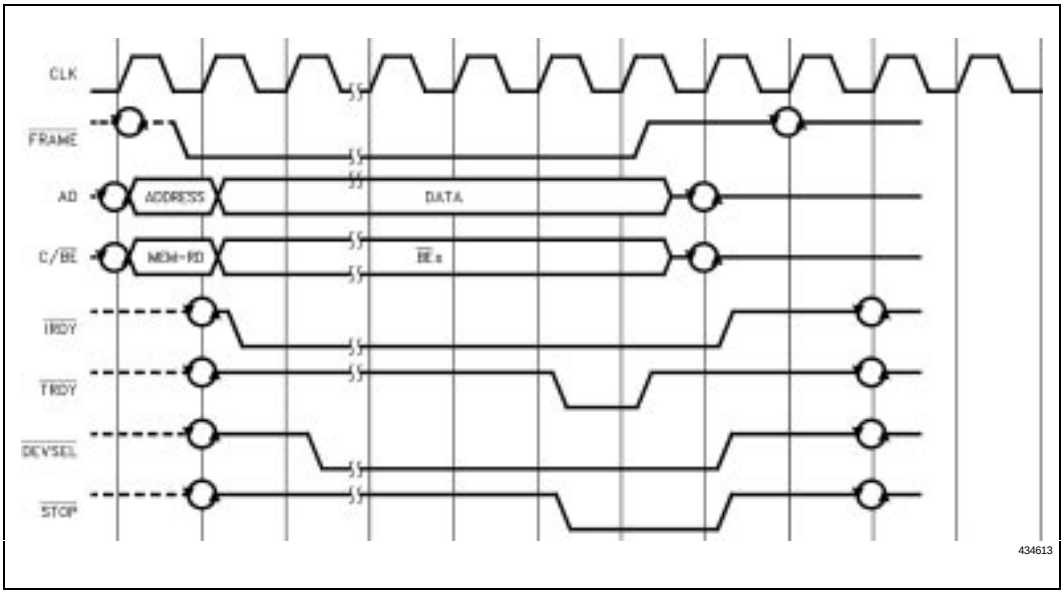

Figure 12. Flash Buffer Write Cycle

System Error: The 82557 reports parity error on address phase using the SERR# pin. If the SERR# Enable bit (in the PCI-configuration command register) or the Parity Error Response bit are not set, the 82557 only sets the Detected Parity Error bit (PCI Status Register, bit 15). If SERR# Enable and Parity Error Response bits are both set, the 82557 sets the Signaled System Error bit (PCI Status Register, bit 14) as well as the Detected Parity Error bit and asserts SERR# for one clock.

The 82557, when detecting system error, will claim the cycle if it was the target of the transaction and continue the transaction as though the address was correct.

NOTE

The 82557 will report a system error for any parity error on address phase, whether or not it is involved in the current transaction.

82557 Bus Master Operation

As a PCI Bus Master, the 82557 initiates memory cycles to fetch data for transmission or deposit received data and for accessing the memory resident control structures. The 82557 performs zero wait state burst read and write cycles to the host main memory. Figure 13 and Figure 14 depict memory read and write burst cycles. For bus master cycles, the 82557 is the initiator and the host main memory (or the PCI Host Bridge depending on the configuration of the systems) is the target.

The CPU provides the 82557 with action commands and pointers to the data buffers that reside in host main memory. The 82557 independently manages these structures and initiates burst memory cycles to transfer data to and from them. The 82557 uses MEM-RD Multiple for burst accesses to data buffers and MEM-RD LINE for burst accesses to control structures (commands, pointers, etc.). For all write burst accesses to either data or control, the 82557 uses the MEM-WR command only.

Read Accesses: The 82557 performs block transfers from host system memory in order to perform frame transmission on the serial link. In this case, the 82557 initiates zero wait state memory read burst cycles for these accesses. The length of a burst is bounded by the system and also by the 82557 internal FIFO. The length of a read burst may also be bounded by the TX DMA MAXIMUM BYTE COUNT in the Configuration command.

The 82557, as the initiator, drives the address lines AD0-31, the command and byte enable lines C/BE0-3# and the control lines IRDY# and FRAME#. The

82557 asserts IRDY# to support zero wait state burst cycles. The target signals the 82557 that valid data is ready to be read by asserting the TRDY# signal.

Write Accesses: The 82557 performs block transfers to host system memory during frame reception. In this case, the 82557 initiates memory write burst cycles to deposit the data, usually without wait states. The length of a burst is bounded by the system and also by the 82557 internal FIFO threshold. The length of a write burst may also be bounded by the RX DMA MAXIMUM BYTE COUNT in the Configuration command.

The 82557, as the initiator, drives the address lines AD0-31, the command and byte enable lines C/BE0-3# and the control lines IRDY# and FRAME#. The 82557 asserts IRDY# to support zero wait state burst cycles. The 82557 also drives valid data on AD0-31 lines during each data phase (from the first clock and on). The target controls the length and signals completion of a data phase by deassertion and assertion of TRDY#.

Cycle Completion: The 82557 completes (terminates) its initiated memory burst cycles in the following cases:

- Normal Completion: all data involved in the transaction has been transferred to or from the target (i.e., host main memory).
- Backoff: the Latency Timer has expired and the arbiter has removed the 82557 bus grant signal (GNT#), indicating that the 82557 has been preempted by another bus master.
- TX or RX DMA MAXIMUM BYTE COUNT: the 82557 burst has reached the length specified in the TX or RX DMA MAXIMUM BYTE COUNT field in the configuration block. Refer to the *82557 User's Manual* for more detailed information.
- Target Termination: the target may request to terminate the transaction with target-disconnect, target-retry, or target-abort. In the first two cases, the 82557 initiates the cycle again. In the case of a Target Abort, the 82557 sets the Received Target Abort bit in the PCI Status field (PCI Status Register, bit 12) and does not reinitiate the cycle.
- Master Abort: the target of the transaction has not responded to the address initiated by the 82557 (DEVSEL# has not been asserted). The 82557 simply deasserts FRAME# and IRDY# as in the case of normal completion.
- Error Condition: in the event of parity or any other system error detection, the 82557 completes its current initiated transaction. Any further action taken by the 82557 depends on the type of error and other conditions.

Data Parity Errors: As an initiator, the 82557 checks and detects data parity errors that occur during a transaction. If the Parity Error Response bit is set (PCI Command Register, bit 6), the 82557 also asserts PERR# and sets the Data Parity Detected bit (PCI Status Register, bit 8). In addition, if the error was detected by the 82557 during read cycles, it sets the Detected Parity Error bit (PCI Status Register, bit 15).

4.2. FLASH/EEPROM Interface

The local memory interface consists of an interface to a FLASH (or EPROM) and an interface to a serial EEPROM. The 82557 provides address decoding and control to allow access to up to 1 Mbyte of FLASH. The EEPROM is used to store information such as Node Individual Address and board configuration.

4.2.1. FLASH INTERFACE OPERATION

The FLASH (or Boot EPROM) is read from or written to whenever the host CPU performs a read or a write operation to a memory location that is within the FLASH mapping window. All accesses to the FLASH, except read accesses, require the appropriate command sequence for the device used. Refer to the specific FLASH data sheet for more details on reading from or writing to FLASH. The accesses to the FLASH are based on a direct decode of CPU accesses to a memory window defined in either the 82557 FLASH Base Address Register (PCI Control Register at offset 18h) or the Expansion ROM Base Address Register (PCI Control Register at offset 30h). The 82557 asserts control to the FLASH when it decodes a valid access.

NOTE

FLASH accesses must always be assembled or disassembled by the 82557 to or from the FLASH whenever the access is greater than a byte-wide access. This is due to slow access times to a typical FLASH and in order to avoid

violating PCI bus holding specifications (no more than 16 wait states inserted for any cycles which are not system-initiation cycles). Write commands should be byte accesses, and read commands should be byte or word accesses for any cycles that occur after system initialization. Boot ROM shadowing is an exception to the 16 clock rule.

Flash registers are described in the *82557 User's Manual*.

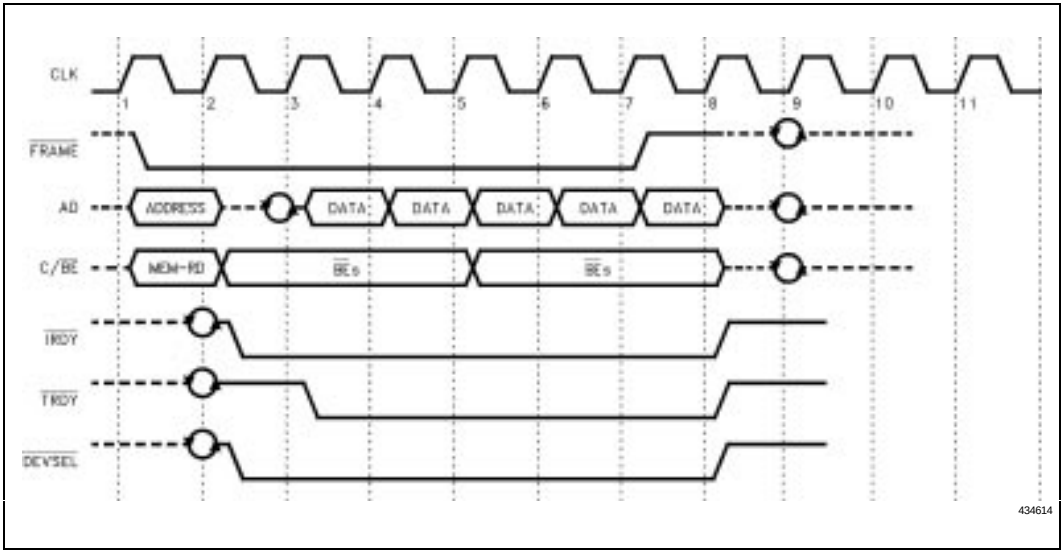

Figure 13. Memory Read Burst Cycles

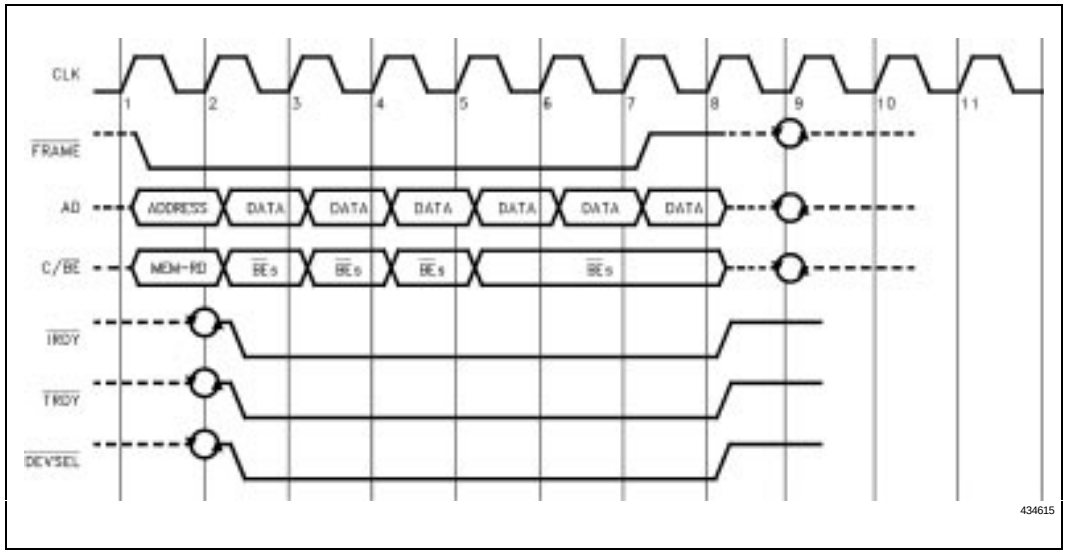

Figure 14. Memory Write Burst Cycle

4.2.2. SERIAL EEPROM INTERFACE

The Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82557. The EEPROM is a serial in/serial out device. Serial EEPROMs range in size from 16 to 256 registers of 16 bits per register. All accesses, either read or write, are preceded by a command instruction to the device. The command instructions, begin with a logical 1 as a start bit, two op code bits (indicating RD, WR, Erase, etc.) and n-bits of address. The address field varies with the size of the EEPROM, for example 6 bits for a 64 register EEPROM, or 8 bits for a 256 register device, etc. The end of the address field is indicated by a dummy 0 bit from the EEPROM which indicates the entire address field has been transferred to the device. A command is issued by asserting the CS signal and clocking the data into the EEPROM on its Data In input relative to the SK (Shift Clock) input. The Chip Select signal is deasserted after completion of the EEPROM cycle (Command, Address and Data). Figure 15 shows the EEPROM timing diagram.

The *82557 User's Manual* describes EEPROM access port and instruction sets.

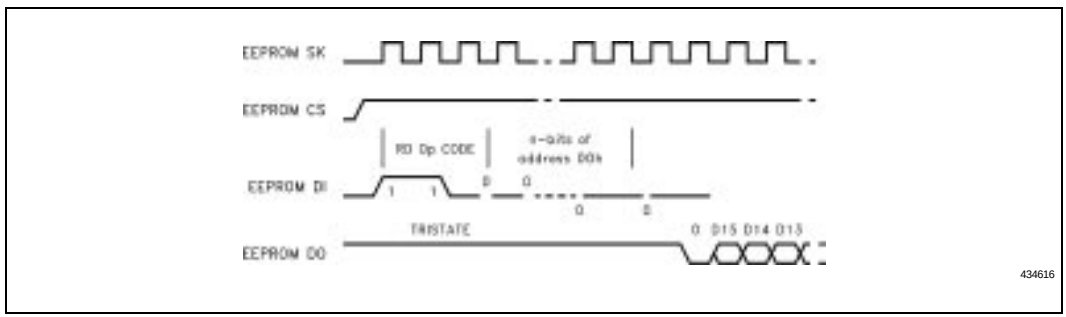

Figure 15. 82557 EPROM Timing Diagram (Example Read from Address 0)

4.3. 10/100 Mbps CSMA/CD Unit

The 82557 CSMA/CD unit implements both the IEEE802.3 10 Mbps and IEEE802.3u Fast Ethernet 100 Mbps standards. It performs all the CSMA/CD protocol functions such as transmission, reception, collision handling, etc. The 82557 CSMA/CD unit operates in two modes of operation; a 10/100 Mbps MII compatible mode, in which the data stream is nibble-wide and the serial clocks run at either 25 or 2.5 MHz, or a 10 Mbps-only mode, in which the data stream is bit-wide and the clocking is at 10 MHz. Selection of either MII compatible mode or 10 Mbps-only mode is by configuration.

The MII compatible mode, along with an MII-compatible 10/100 Serial PHY, switches automatically between either 10 or 100 Mbps operation depending on the speed of the network to which it is attached. During frame transmission, byte wide data is accepted from the 82557 internal FIFO block. The CSMA/CD unit builds the IEEE 802.3 frame format and depending on the mode, the frame is either transmitted as a bit stream (10 Mbps-only mode) or as a nibble stream (10/100 Mbps MII mode). During frame reception the CSMA/CD unit converts the bit stream (10 Mbps-only mode) or nibble stream (10/100 Mbps MII mode) to a byte wide format, strips off the frame delimiters, such as the preamble and SFD and then passes the data to the 82557 internal FIFO block from where it is deposited into host system memory via the 82557 PCI Bus Master interface.

4.3.1. 10/100 MBPS MII COMPATIBLE INTERFACE

The CSMA/CD unit provides the functional interface to any MII compatible serial PHY. The data path consists of a separate nibble-wide stream for both transmit and receive activities. Data transfers are clocked by the 25 MHz transmit and receive clocks in 100 Mbps operation, or by 2.5 MHz clocks in 10 Mbps operation. These clock inputs are driven by the PHY.

4.3.1.1. 10/100 Mbps MII Transmission

When the 82557 has a frame ready for transmission, it samples the link for activity. If the CRS signal is inactive (no activity on the link), frame transmission begins. The data is transmitted via pins TXD0-3, clocked on the rising edge of TXC. The signal TXEN is asserted at this same time. The CRS signal is expected to be asserted before one slot time has elapsed, however the transmission will complete successfully even if CRS is not asserted (the absence of CRS will be reported in a status bit). In the case of a collision, the PHY asserts the COL signal on the 82557 which will then stop transmitting the frame within four clock times and append a JAM sequence onto the link.

After the end of a collided transmission, the 82557 will back off and attempt to retransmit once the backoff timer expires. Note that the retransmission is done from the data stored internally in the 82557 FIFO block, so no re-access to the data in host memory is performed. In the case of a successful transmission, the 82557 is ready to transmit any other frames queued in its FIFO block within the minimum inter frame spacing (IFS) of the link.

4.3.1.2. 10/100 Mbps MII Reception

Frame reception starts with the assertion of CRS (while the 82557 is not transmitting) by the PHY. Once RXDV is asserted, 82557 will begin sampling incoming data on pins RXD0-3 on the rising edge of RXC. There is a minimum of four RXC clock periods from assertion of CRS until the 82557 samples the first RCV data nibble from the PHY. The 82557 accepts frames which pass its address filtering mechanism, passing the frame in a byte-wide format to its internal FIFO block. Reception ends when CRS is deasserted by the PHY. The last nibble sampled by the 82557 is the nibble present on RXD0-3 on the RXCLK rising edge in which RXDV deassertion is detected and CRS is still asserted.

During reception the RXDV (Receive Data Valid) signal is asserted to the 82557. If the 82557 detects the assertion of RXER while RXDV is asserted, it will designate this frame as a corrupted frame by setting an error bit in the status field of the frame. The 82557 will continue to receive the incoming frame regardless of the RXER signal. RXDV should remain deasserted while no reception is taking place.

4.3.2. 10/100 MII MBPS FULL DUPLEX OPERATION

When operating in full duplex mode the 82557 can transmit and receive frames simultaneously. In full duplex mode the CRS signal is associated with received frames only and has no affect on transmitted frames. Similarly, COL is associated with transmission only and does not affect received frames.

Transmission starts when TXEN goes active. Transmission starts regardless of the state of CRS. Reception starts when the CRS signal is asserted indicating traffic on the RCV pair of the PHY.

4.3.3. 10 MBPS-ONLY INTERFACE

The 10 Mbps mode is fully compliant with the IEEE 802.3 CSMA/CD standard. It interfaces to 10 Mbps-only PHY devices such as the Intel 82503. The 10 Mbps serial interface is bit wide. Transmission is performed on the TXD0 pin and reception on RXD0. Serial data is clocked on the rising edge of the clock; TXCLK for transmission and RXCLK for reception. These clocks operate at 10 MHz and are both driven by the PHY.

4.3.3.1. 10 Mbps Transmission

When the 82557 has a frame ready for transmission, it samples the link for activity. If the CRS signal is inactive (no activity on the link), frame transmission begins. The data is transmitted via TXD0 and is clocked on the rising edge of TXC. The RTS signal is asserted at this time. The CRS signal is expected to be asserted before one slot time has elapsed, however the transmission will complete successfully even if CRS is not asserted (the absence of CRS will be reported in a Lost CSR status bit). In the case of a collision, the PHY asserts the COL signal to the 82557 which will then stop transmitting the frame within four clock times and append a JAM sequence onto the link. After the end of a collided transmission the 82557 will back off and attempt to transmit once again when the back off timer expires. Note that the retransmission is done from the data stored internally in the 82557 FIFO block, so no re-access to the data in host memory is performed. In the case of a successful transmission, the 82557 is ready to transmit any other frames queued in its FIFO block within the minimum IFS of the link.

4.3.3.2. 10 Mbps Reception

Frame reception starts with the assertion of CRS by the PHY. The 82557 will then start sampling incoming data on RXD0 on the rising edge of RXC. There is a PHY-dependant delay of two or more clock cycles between the assertion of CRS and the first data bit the 82557 samples. The 82557 accepts frames which pass its address filtering mechanism and passes the frame in a byte-wide format to its internal FIFO block. Reception ends when CRS is deasserted by the PHY. The last bit sampled by the 82557 is the bit present on RXD0 on the RXCLK rising edge in which CRS deassertion is detected.

4.3.3.3. 10 Mbps Full Duplex Operation

In 10 Mbps-only mode, when the 82557 is placed in Full Duplex mode transmission will begin regardless of the state of CRS or the 82557 receive unit. The 82557 receiver accepts incoming frames regardless of the transmitters operation. The 82557 does not accept the COL input in this mode. Frame delineation is by CRS deassertion.

4.4. MII Management Interface

The MII management interface allows the CPU to have direct control over an MII-compatible PHY device via a control register in the 82557. This allows the driver software to place the PHY in specific modes such as Full Duplex, Loopback, Power Down, etc., without the need for specific hardware pins to select the desired mode. This structure allows the 82557 to query a PHY device for status of the link. This register, called the MDI Control Register, resides at offset 10h in the 82557 CSR. The CPU writes commands to this register and the 82557 reads or writes control/status parameters to the PHY device via a serial, bi-directional data pin called MDIO. These serial data transfers are clocked by the MDC clock output from the 82557.

The *82557 User's Manual* describes the structure of the MDI control register and the MDI read and write cycle bit streams.

4.4.1. MDI CYCLES

The MDI protocol consists of a bit stream that is driven or sampled by the 82557 on each rising edge of the MDC pin. The bit stream consists of the following elements:

```
<PREAMBLE><ST><OP><PHYAD><REGAD><TA>
<DATA><IDLE>
```

where:

PREAMBLE At the beginning of each transaction, the 82557 sends a sequence of 32 contiguous logic one bits on the MDIO pin with corresponding cycles on the MDC clock pin for synchronization by the PHY.

ST A Start of Frame pattern of 01.

OP An Operation Code which can assume one of two values:

10 Read

01 Write

PHYAD A 5 bit address of the PHY device which provides support for 32 unique PHY addresses. The 82557 will drive the value written into the PHYAD portion of the MDI register in this field.

REGAD A 5 bit address of the specific register within the PHY device. This provides support for 32 unique registers. The desired register address is specified by the value written to the MDI register.

TA A two-bit turnaround time during which no device actively drives the MDIO signal on a read cycle. During a read transaction the PHY should not drive MDIO in the first bit time and drive a 0 in the second bit time. During a write transaction the 82557 will drive a '10' pattern to fill this time.

DATA 16 bits of data driven by the PHY on read transactions or by the 82557 on write transactions. This data is either control or status parameters passed between the 82557 and the PHY.

IDLE The IDLE condition on MDIO is a high impedance state. The MDIO driver is disabled, and the PHY should pull-up the MDIO line to a logic one.

5.0. 82557 SOFTWARE INTERFACE

5.1. The Shared Memory Communication Architecture

The 82557 establishes a shared memory communication system with the host CPU. This shared memory is divided into three parts: the Control/Status Registers (CSR), the Command Block List (CBL), and the Receive Frame Area (RFA). The CSR resides on-chip and can be accessed by either I/O or memory cycles, while the rest of the 82557 memory structures reside in system (host) memory.

The first 8 bytes of the CSR is called the System Control Block (SCB). The SCB serves as a central communication point for exchanging control and status information between the host CPU and the 82557.

The host software controls the state of the 82557 Command Unit (CU) and Receive Unit (RU) (i.e., Active, Suspended or Idle) by writing commands to the SCB. The 82557 posts the status of the CU and RU in the SCB Status word and indicates status changes with an interrupt. The SCB also holds pointers to a linked list of action commands called the CBL and a linked list of receive resources called the RFA. Figure 16 shows this type of structure.

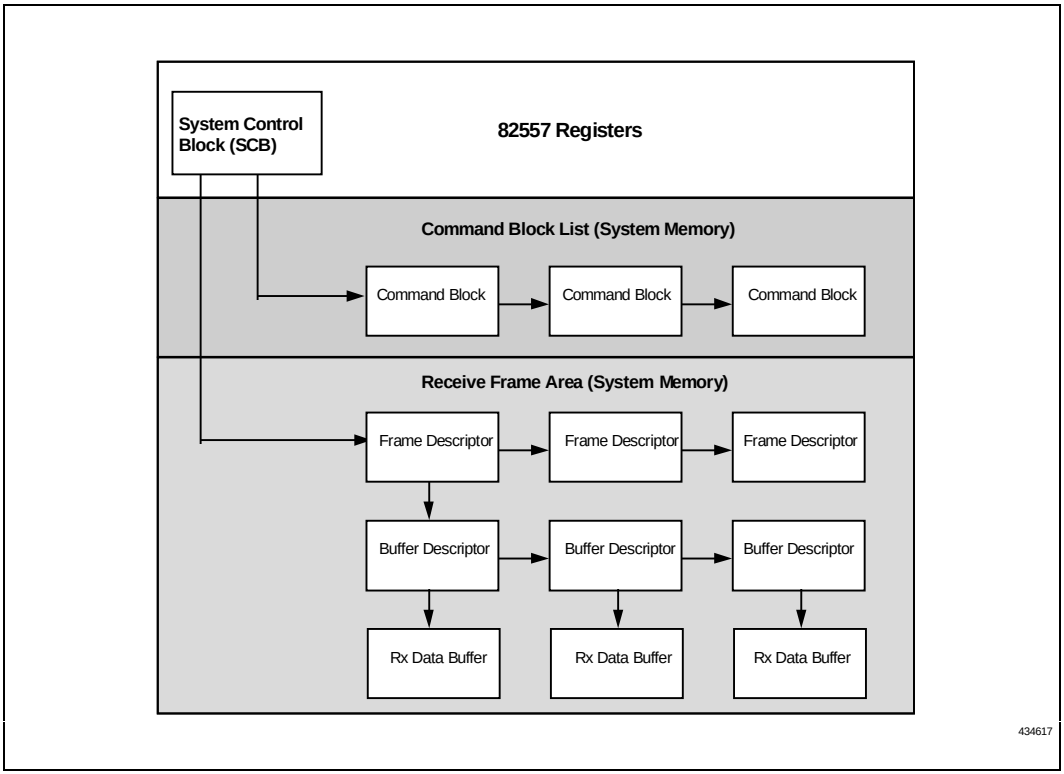

Figure 16. 82557 Shared Memory Structure

The CBL consists of a linked list of individual action commands in structures called Command Blocks (CBs). The CBs contain command parameters and status of the action commands. Action commands are categorized as follows:

- Non-Tx commands: This category includes commands such as NOP, Configure, IA Setup, Multicast Setup, Dump and Diagnose.
- Tx command: This includes Transmit Command Blocks (TxCB).

Transmit commands can be programmed in Simplified or Flexible memory modes. In the Simplified memory model, the TxCB contains the full transmit frame, immediately following the header information. In the Flexible memory model, each TxCB can be associated with a list of 0 or more Transmit Buffer Descriptors (TBD). Each TBD points to a data buffer fragment. All the data fragments associated with a TxCB (including data in the optional data area of the TxCB) comprise the full transmit frame.

The RFA consists of a list of Receive Frame Descriptors (RFD) and a list of user-prepared or NOS provided buffers. Two memory models are supported. In the Simplified memory model, the data buffer immediately follows the RFD. In the Flexible memory model, each RFD can be associated with an array of zero or more Receive Buffer Descriptors (RBD). Each RBD points to a data buffer fragment. The 82557 RU fills the buffers when it receives frames and updates the status in the RFD (and RBDs if applicable).

The 82557 also provides read/write access to external EEPROM, Flash memory and MDI (Management Data Interface) registers. This is achieved through the EEPROM Control Register, Flash Control Register, and the MDI Control Register respectively. These three registers make up the last eight bytes (0Ch - 14h) of the CSR.

Table 8. Summary of Reset Commands

RESET Operation	Effect On 82557
Hardware reset	Resets all internal registers. A full initialization sequence is needed to make the 82557 operational.
Software reset***** (issued as PORT RESET****** command)	Resets all internal registers except the PCI configuration registers. A full initialization sequence is needed to make the 82557 operational.
Selective Reset (issued as PORT SELECTIVE RESET****** command)	Maintains configuration information. All other setup information is lost.
Self Test (issued as a PORT SELF TEST****** command) or PORT DUMP command	Resets all internal registers. A Selective Reset is issued internally before the command is executed. A Software Reset is issued internally after the command is completed. A full initialization sequence is needed to make the 82557 operational.

NOTES:

* Software reset will be used throughout this manual to indicate a complete reset using the PORT reset command.
** PORT commands are discussed in detail in the *82557 User's Manual.*

5.2. Initializing the 82557

A power-on or software reset prepares the 82557 for normal operation. Because the PCI specification already provides for auto-configuration of many critical parameters such as I/O, memory mapping and interrupt assignment, the 82557 is set to an operational default state after reset. However, the 82557 cannot transmit or receive frames until a Configure command is issued. Refer to the *82557 User's Manual* for additional information. Table 6 lists the different reset options.

5.3. Controlling the 82557

The CPU issues control commands to the Command Unit (CU) and Receive Unit (RU) through the SCB, which is part of the CSR (described below). The CPU instructs the 82557 to Activate, Suspend, Resume or Idle the CU or RU by placing the appropriate control command in the CU or RU control field. A CPU write access to the SCB causes the 82557 to read the SCB, including the Status word, Command word, CU and RU Control fields, and the SCB General Pointer. Activating the CU causes the 82557 to begin executing the CBL. When execution is completed the 82557 updates the SCB with the CU status then interrupts the CPU, if configured to do so. Activating the RU causes the 82557 to access the RFA and go into the READY state for frame reception. When a frame is received the RU updates the SCB with the RU status and interrupts the CPU. It also automatically advances to the next free RFD in the RFA. This interaction between the CPU and 82557 can continue until a software reset is issued to the 82557, at which point the initialization process must be executed again. The CPU can also perform certain 82557 functions directly through a CPU PORT interface.

5.3.1. THE 82557 CONTROL/STATUS REGISTER (CSR)

The 82557 has eight Control/Status registers which make up the CSR space. These are the SCB Command word, SCB Status word, SCB General Pointer, PORT interface, EEPROM Control register, Flash Control register, MDI Control register, and the Early Receive Interrupt Byte Control register. The CSR space is six DWORDs in length and is shown in Table 9. The 82557 CSR can be accessed as either an I/O mapped or memory mapped PCI slave.

Table 9. Control/Status Register

31 Upper Word 16	15 Lower Word 0	Offset
SCB Command Word	SCB Status Word	Base + 0h
SCB General Pointer		Base + 4h
PORT		Base + 8h
EEPROM Control Register	Flash Control Register	Base + Ch
MDI Control Register		Base + 10h
Early RCV Interrupt Rx Byte Count (RXBC) Register		Base + 14h

SCB Command word: The CPU places commands for the CU and RU and acknowledges interrupts in this register.

SCB Status word: The 82557 places the status of its CU and RU (and interrupt indications in this register) for the CPU to read.

SCB General Pointer: This points to various data structures in main memory depending on the current SCB Command word.

PORT Interface: This special interface allows the CPU to reset the 82557, force the 82557 to dump information to main memory, or perform an internal Self-Test.

EEPROM Control Register: This register allows the CPU to read and write to an external EEPROM.

Flash Control Register: This register allows the CPU to enable writes to an external Flash.

MDI Control Register: This register allows the CPU to read and write information from Physical Layer components via the Management Data Interface.

Early Receive Int. Count: This register allows the CPU to read the current value in the RX DMA byte count register. The RX DMA byte count register is a counter that keeps track of how many bytes of receive data have been passed into host memory via DMA.

5.3.1.1. Statistical Counters

The 82557 provides information for network management statistics by providing on-chip statistical counters that count a variety of events associated with both transmit and receive. The counters are updated by the 82557 when it completes the processing of a frame (when it has completed transmitting a frame on the link or when it completed receiving a frame). The Statistical Counters are reported to the software on demand by issuing the *Dump Statistical Counters* command or *Dump and Reset Statistical Counters* command in the SCB Command Unit Command (CUC) field.

Table 10. Statistical Counters

ID	Counter	Description
0	Transmit good frames	This counter contains the number of frames that were transmitted properly on the link. It is updated only after the actual transmission on the link is completed, and not when the frame was read from memory as is done for the TxCB status.
4	Transmit Maximum Collisions (MAXCOL) Errors	This counter contains the number of frames that were not transmitted since they encountered the configured maximum number of collisions.
8	Transmit late collisions (LATECOL) Errors	This counter contains the number of frames that were not transmitted since they encountered a collision later than the configured slot time.
12	Transmit Underrun Errors	A DMA underrun occured because the system bus did not keep up with the transmission. This counter contains the number of frames that were either not transmitted or retransmitted due to a TxDMA underrun. If the 82557 is configured to retransmit on underrun, this counter may be updated multiple times for a single frame.
16	Transmit Lost carrier sense (CRS)	Transmission was not successful due to lost Carrier Sense. This counter contains the number of frames that were transmitted by the 82557 despite the fact that it detected the deassertion of CRS during the transmission.
20	Transmit Deferred	During the transmission attempt the 82557 had to defer to traffic on the link. This counter contains the number of frames that were deferred before transmission due to activity on the link.
24	Transmit Single Collisions	This counter contains the number of transmitted frames that encountered one collision.
28	Transmit Multiple Collisions	This counter contains the number of transmitted frames that encountered more than one collision.
32	Transmit Total Collisions	This counter contains the total number of collisions that were encountered while attempting to transmit. This count includes late collisions and frames that encountered MAXCOL.
36	Receive Good Frames	This counter contains the number of frames that were received properly from the link. It is updated only after the actual reception from the link is completed and all the data bytes are stored in memory.
40	Receive CRC Errors	This counter contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the RU state. If the RX_ER pin is asserted during a receive frame, the CRCERRS counter will increment (only once per receive frame). The CRCERRS counter is mutually exclusive to the ALNERRS and SHRTFRM counters.

Table 10. Statistical Counters (Contd.)

44	Receive Alignment Errors	This counter contains the number of frames that are both misaligned (i.e., where CRS deasserts on a nonoctal boundary) and contain a CRC error. The counter is updated, if needed, regardless of the RU state. The ALNERRS counter is mutually exclusive to the CRCERRS and SHRTFRM counters.
48	Receive Resource Errors	This counter contains the number of good frames discarded because there were no resources available. Frames intended for a host whose RU is in the No Resources state fall into this category. If the 82557 is configured to Save Bad Frames and the status of the received frame indicates that it is a bad frame, the RSCERRS counter is not updated.
52	Receive Overrun Errors	This counter contains the number of frames known to be lost because the local system bus was not available. If the traffic problem persists for more than one frame, the frames that follow the first are also lost; however, because there is no lost frame indicator, they are not counted.
56	Receive Collision Detect (CDT) Errors	This counter contains the number of frames that encountered collisions during frame reception.
60	Receive Short Frame Errors	This counter contains the number of received frames that are shorter than the minimum frame length. The SHRTFRM counter is mutually exclusive to the ALNERRS and CRCERRS counters and has a higher priority (i.e., a short frame will always increment only the SHRTFRM counter).
64	Dump Counters Completion Status	

The Statistical Counters are initially set to zero by the 82557 after reset. They cannot be preset to anything other than zero. The 82557 increments the counters by internally reading them, incrementing them and writing them back. This process is invisible to the CPU and PCI bus. Refer to the *82557 User's Manual* for additional information.

6.0. ELECTRICAL SPECIFICATIONS AND TIMINGS

For more information on the quality and reliability of the 82557, refer to the *Components Quality and Reliability Handbook*, order number 210997.

6.1. Absolute Maximum Ratings

Case temperature under bias	0°C to +85°C
Storage temperature	-65°C to +140°C
All output and supply voltages	-0.5V to +7V
All input voltages	-1.0V to 6.0V

WARNING

Stressing the device beyond the 'Absolute Maximum Ratings' may cause permanent damage. These are stress ratings only. Operation beyond the 'Operating Conditions' is not recommended and extended exposure beyond the 'Operating Conditions' may affect device reliability.

6.2. DC Specifications

Table 11. General DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CC}	Supply Voltage		4.75		5.25	V	
I_{CC}	Power Supply			300		mA	

Table 12. PCI Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{ih}	Input High Voltage		2.0	V_{cc}+0.5	V	
V_{il}	Input Low Voltage		-0.5	0.8	V	
I_{ih}	Input High Leakage Current	V_{in} = 2.7		70	µA	1
I_{il}	Input Low Leakage Current	V_{in} = 0.5		-70	µA	1
V_{oh}	Output High Voltage	I_{out} = -2 mA	2.4		V	
V_{ol}	Output Low Voltage	I_{out} = 3 mA, 6 mA		0.55	V	2
C_{in}	Input Pin Capacitance			10	pF	3
C_{clk}	CLK Pin Capacitance		5	12	pF	3
C_{IDSEL}	IDSEL Pin Capacitance			8	pF	3
Lpin	Pin Inductance			20	nH	3

NOTES:

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pull-up resistors have 3 mA low output current. Signals requiring pull-up have 6 mA; the latter include, **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#**, **SERR#** and **PERR#.**
3. Characterized, not tested.

Table 13. MII and 10 Mbps PHY Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{ih}	Input High Voltage		2.0	V_{cc}+0.5	V	
V_{il}	Input Low Voltage		-0.5	0.8	V	
I_{il}	Input Low Leakage Current	$0 < V_{in} < V_{cc}$		±20	µA	
V_{oh}	Output High Voltage	I_{out} = -4 mA	2.4		V	
V_{ol}	Output Low Voltage	I_{out} = 4 mA		0.4	V	3
C_{in}	Input Pin Capacitance			8	pF	1

NOTES:

1. Characterized, not tested.
2. To drive an MII cable (Z0 = 68Ω ± 15%, Length @ 0.5m) a 40Ω ± 10% resistor should be connected in series to each MII output.
3. For pins LPBCK and RSTOUT, I_{ol} = 1mA.

Table 14. FLASH/EEPROM Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{ih}	Input High Voltage		2.0	V_{cc}+0.5	V	
V_{il}	Input Low Voltage		-0.5	0.8	V	
I_{il}	Input Low Leakage Current	$0 < V_{in} < V_{cc}$		±20	µA	
V_{oh}	Output High Voltage	I_{out} = -1 mA	2.4		V	
V_{ol}	Output Low Voltage	I_{out} = 1 mA		0.4	V	
C_{in}	Input Pin Capacitance			10	pF	1

NOTES:

1. Characterized, not tested.

6.3. AC Specifications

6.3.1. PCI INTERFACE

Table 15. AC Specifications for PCI Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{oh(AC)}$	Switching	$0 < V_{out} \leq 1.4$	-44		mA	1, 2
	Current High	$1.4 < V_{out} < 2.4$	$-44+(V_{out}-1.4)/0.024$	Eqt'n A	mA	1, 2
	(Test Point)	$V_{out} = 3.1$		-142	mA	1, 2
$I_{ol(AC)}$	Switching	$V_{out} \geq 2.2$	95		mA	2
	Current Low	$2.2 > V_{out} > 0.55$	$V_{out}/0.023$	Eqt'n B	mA	1, 2
	(Test Point)	$V_{out} = 0.71$		206	mA	2
I_{cl}	Low Clamp Current	$-5 < V_{in} \leq -1$	$-25+(V_{in}+1)/0.015$		mA	2
t_r	Unloaded Output Rise Time	0.4V to 2.4V	1	5	V / ns	1, 4
t_f	Unloaded Output Fall Time	2.4V to 0.4V	1	5	V / ns	2, 4

NOTES:

1. Not relevant to SERR# or INTA#, which are open drain outputs.
2. Characterized, not tested.

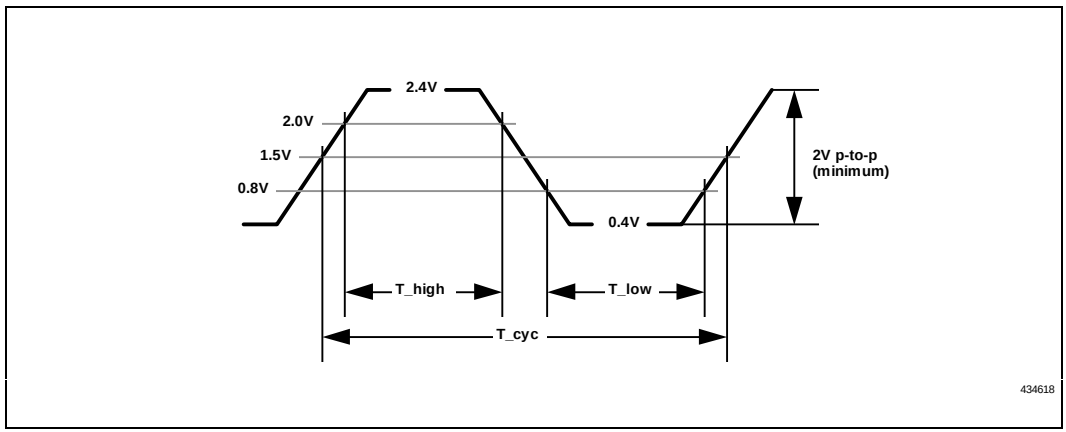

Figure 17. Clock Waveforms

6.4. Timing Specification

6.4.1. CLOCK SPECIFICATIONS

6.4.1.1. PCI Interface Clock

The 82557 uses the PCI clock. Figure 17 shows the clock waveform and required measurement points for the PCI clock signal. Table 16 summarizes the PCI clock specifications. This clock waveform should be treated as the minimum for the 82557.

6.4.1.2. MII Interface Clock

The 82557 uses two clocks on the MII interface: transmit clock (TXCLK) and receive clock (RXCLK). Table 17 shows timings for each clock.

6.4.1.3. 10 Mbps Serial Interface Clock

The 82557 uses two clocks on the serial interface: transmit clock TXC and receive clock RXC. Table 17 shows timings for both clocks.

Table 16. PCI Clock Specifications

	Symbol	Parameter	Min	Max	Units	Notes
T1	t_{cyc}	CLK Cycle Time	30		ns	1
T2	t_{high}	CLK High Time	11		ns	
T3	t_{low}	CLK Low Time	11		ns	
T4	-	CLK Slew Rate	1	4	V/ns	2

NOTES:

1. The 82557 will work with any PCI clock frequency up to 33 MHz.
2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate should be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 17.

Table 17. MII Clock Specifications

	Symbol	Parameter	Min	Typical	Max	Units	Notes
T5	t_{cyc100}	TXC/RXC Cycle Time @ 100 Mbps operation		40		ns	1, 2, 3
T6	t_{cyc10}	TXC/RXC Cycle Time @ 10 Mbps operation		400		ns	1, 2, 3
T7	DC	TXC/RXC Duty Cycle	35		65	%	1, 2, 3

NOTES:

1. Either high or low times of RXCLK may be extended at the event of switching it from recovered clock to TXCLK, or vice versa.
2. No specific phase relationship is assumed between TXCLK and RXCLK.
3. When RXDV is active, the frequency difference between TXCLK and RXCLK should not exceed ± 200 ppm.

Table 18. Serial Interface Clock Specifications

	Symbol	Parameter	Min	Typical	Max	Units	Notes
T8	t_{cycTXC}	TXC Cycle Time	99.99		100.01	ns	
T9	t_{hi_loTXC}	TXC Duty Cycle	35	50	65	%	
T10	t_{r_fTXC}	TXC rise/fall Time			5	ns	
T11	t_{cycRXC}	RXC Cycle Time		100		ns	
T12	t_{hi_loRXC}	RXC Duty Cycle	35		65	%	
T13	t_{r_fRXC}	RXC rise/fall Time			5	ns	

NOTES:

1. No specific phase relationship is assumed between TXC and RXC.

6.4.2. TIMING PARAMETERS

6.4.2.1. PCI Timings

Table 19 provides the timing parameters for the 82557 PCI interface.

Table 19. PCI Timing Parameters

	Symbol	Parameter	Min	Max	Units	Notes
T14	t_{val}	CLK to Signal Valid Delay: bused signals	2	11	ns	1, 2, 3
T15	$t_{val}(ptp)$	CLK to Signal Valid Delay: point to point	2	12	ns	1, 2, 3
T16	t_{on}	Float to Active Delay	2		ns	1
T17	t_{off}	Active to Float Delay		28	ns	1
T18	t_{su}	Input Set up Time to CLK: bused signals	7		ns	3, 4
T19	$t_{su}(ptp)$	Input Set up Time to CLK: point to point	10		ns	3, 4
T20	t_{h}	Input Hold Time from CLK	0		ns	4
T22	$t_{rst-clk}$	Reset Active Time After CLK Stable	100		µs	5
T23	$t_{rst-off}$	Reset Active to Output Float delay		40	ns	5, 6

NOTES:

1. See timing measurement conditions diagram in this section.
2. Minimum times are specified with 0 pF equivalent load; maximum times are specified with 50 pF equivalent load. Actual test capacitance may vary, but results are correlated to these specifications.
3. REQ# and GNT# are point-to-point signals, and have different output valid delay and input setup times than do bused signals. All other signals are bused.
4. See timing measurement conditions in this section.
5. RST# is asserted and deasserted asynchronously with respect to CLK.
6. All PCI bus output drivers are floated when RST# is active.

6.4.2.2. MII and 10 Mbps Interface Timings

Table 20 provides the timing parameters for MII and serial interface signals.

Table 20. MII and Serial Interface Timing Parameters

	Symbol	Parameter	Min	Max	Units	Notes
T24	t_{valTX}	TX Synchronous Signals Valid Time	0	15	ns	1, 3
T25	t_{suRX}	RX Synchronous Signals Setup Time	10		ns	2, 3
T26	t_{hRX}	RX Synchronous Signals Hold Time	10		ns	2, 3
T27	$t_{hiloMDC}$	MDC high/low Time	200		ns	5, 7
			310		ns	5, 8
T28	t_{valMD}	MDC to MDIO Valid Delay	50	440	ns	6, 7
			50	580	ns	6, 8
T29	TsuMDIO	MDIO Setup Time	120		ns	6, 7
			120		ns	6, 8
T30	t_{hMDIO}	MDIO Hold Time	0		ns	6

NOTES:

1. TX Synchronous Signals are: TXD0-3 and TXEN (RTS in serial interface).
2. RX Synchronous Signals are: RXD0-3, RXDV and RXER.
3. The timing reference is the rising edge of TXCLK, for transmit, or RXCLK, for receive.
4. To drive an MII cable (Z_0 = 68Ω ± 15%, Length @ 0.5m) a 40Ω ± 10% resistor should be connected in series with each MII output (TXD0-3, TXEN, MDC and MDIO).
5. MDC is an aperiodic signal.
6. Referenced to rising edge of MDC.
7. These timings apply when the PCI clock rate is 33 MHz. As the PCI clock rate references the MDC/MDIO interface, these timngs scale accordingly.
8. These timings apply when the PCI clock rate is 25 MHz. As the PCI clock rate references the MDC/MDIO interface, these timngs scale accordingly.
9. The MDC/MDIO timings are specified as measured at the 82557, and as required or supplied by the 82557.
10. CRS and COL (CLD in serial interface) are asynchronous with regard to either RXCLK or TXCLK.

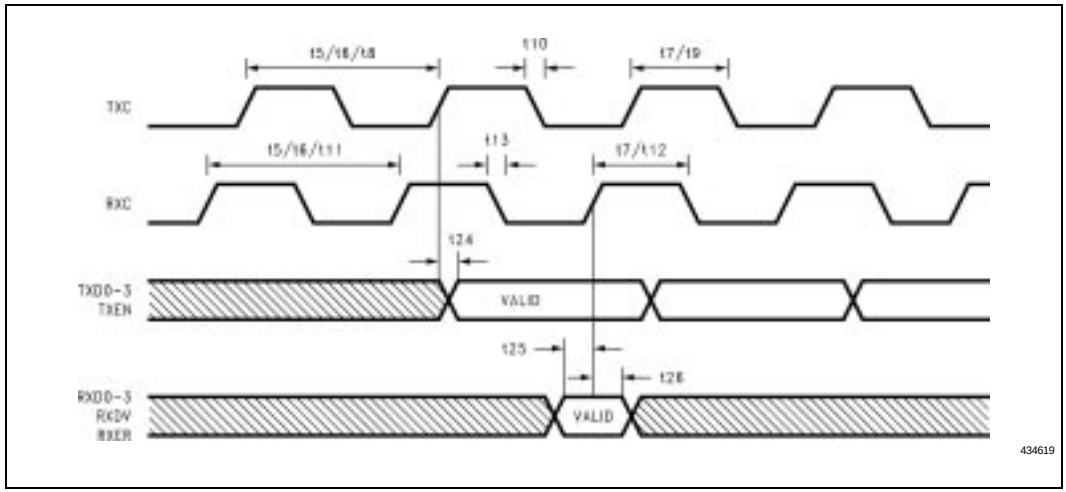

Figure 18. Transmit Timings

6.4.2.3. Collision Parameters

Symbol	Parameter	Typical	Units
Tcol	Collision Active to Jam Start	4	TXCLK periods

Table 21. FLASH Interface Timing Parameters

	Symbol	Parameter	Min	Max	Units	Notes
T31	t_{flrwc}	Read/Write Cycle Time	150		ns	1, flash t_{AVAV}=150ns
T32	t_{flacc}	FLADDR to Read FLD Setup Time	150		ns	1, flash t_{AVQV}=150ns
T33	t_{flce}	FLCS# to Read FLD Setup Time	150		ns	1, flash t_{ELQV}=150ns
T34	t_{floe}	FLOE# Active to Read FLD Setup Time	120		ns	1, flash t_{GLQV}=55ns
T35	t_{fldf}	FLOE# Inactive to FLD Driven Delay Time		50	ns	1, flash t_{GHQZ}=35ns
T36	t_{flas}	FLWE# Active Delay after FLADDR Stable	5		ns	2, flash t_{AVWL}=0ns
T37	t_{flah}	FLADDR Stable after FLWE# Active	100		ns	2, flash t_{WLAX}=60ns
T38	t_{flcs}	FLWE# Active Delay after FLCS# Active	20		ns	2, flash t_{ELWL}=20ns
T39	t_{flch}	FLCS# Inactive Delay after FLWE# Inactive	0		ns	2, flash t_{WHEH}=0ns
T40	t_{flds}	FLWE# Inactive Delay after FLD Stable	50		ns	2, flash t_{DVWH}=50ns
T41	t_{fldh}	FLD Delay after FLWE# Inactive	10		ns	2, flash t_{WHDX}=10ns

Table 21. FLASH Interface Timing Parameters (Contd.)

	Symbol	Parameter	Min	Max	Units	Notes
T42	t_{flwp}	Write Pulse Width	120		ns	2, flash t_{WLWH}=60ns
T43	t_{flwph}	Write Pulse Width High	25		ns	2, flash t_{WHWL}=20ns
T44	t_{lasu}	FLADDR Setup Time before FLCS#	4		ns	3, latch t_{SU}=2ns
T45	t_{lah}	FLADDR Hold Time after FLCS#	4		ns	3, latch t_{H}=1.5ns

NOTES:

1. These timing specifications apply to FLASH read cycles. The flash timings referenced are 28F020-150 timings.
2. These timing specifications apply to FLASH write cycles. The flash timings referenced are 28F020-150 timings.
3. These timing specifications apply to all FLASH cycles.

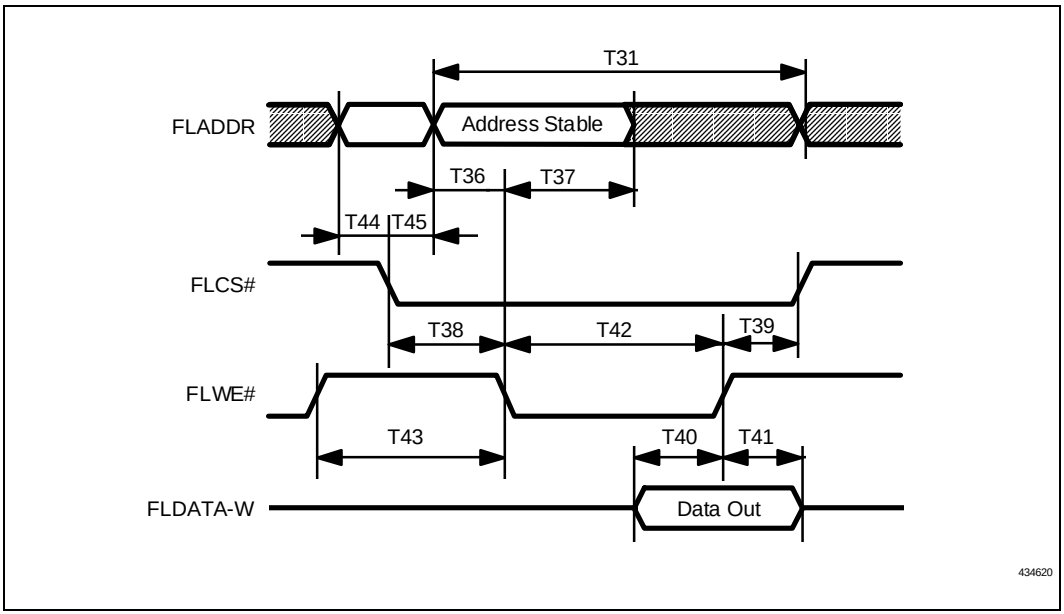

Figure 19. FLASH Timings: Write Cycle

6.4.2.4. FLASH Interface Timings

- The 82557 is designed to support FLASH access times up to 150 nanoseconds.
- The Vpp signal in FLASH implementation should be connected permanently to12V. Thus, writing to the FLASH is controlled only by the **WE#** signal.

Table 21 provides the timing parameters for FLASH interface signals. The timing parameters are illustrated in Figure 19 and Figure 20.

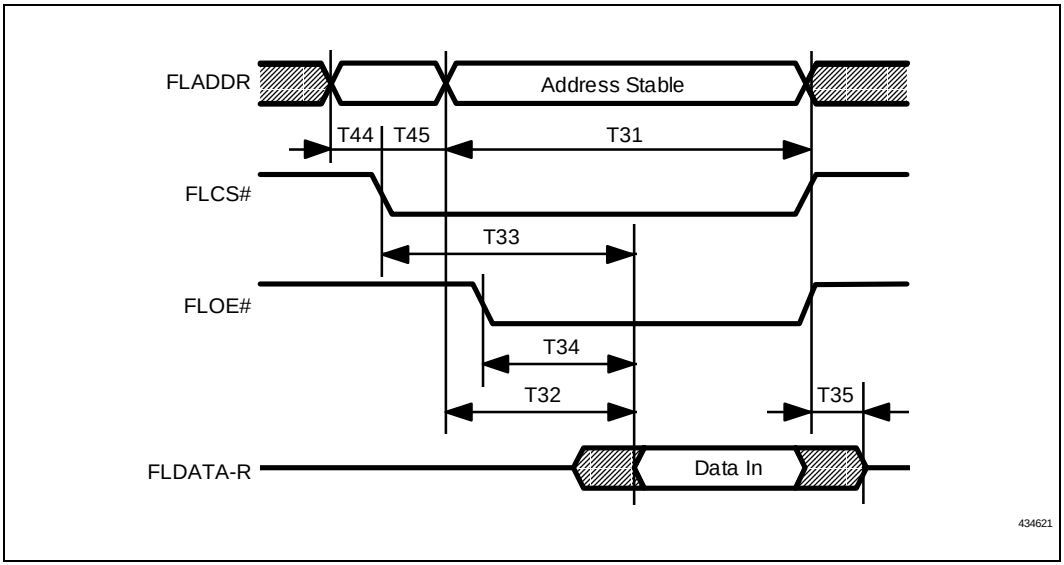

Figure 20. FLASH Timings: Read Cycle

Table 22. Intel 82557 Package Attributes

Attribute	Value
Lead Count	160
Square or Rectangle?	Square
Pitch (mm)	0.65
Package Thickness (mm)	3.65
Weight (gm)	6.0 (approx.)
Shipping Media	Trays
Desiccant Pack	Yes
Comments	Gull wing lead configuration, non-bumpered

7.0. PHYSICAL ATTRIBUTES AND DIMENSIONS

This section provides the physical packaging information for the 82557. The 82557 is a 160-lead plastic quad flatpack (PQFP) device. Package attributes are provided in Table 22 and dimensions are shown in Figure 21 and Figure 22. Table 23 shows the dimensions for the figures. For more information on Intel device packagaging, refer to the *Intel Packaging Handbook*, available from Intel Literature or your local sales office.

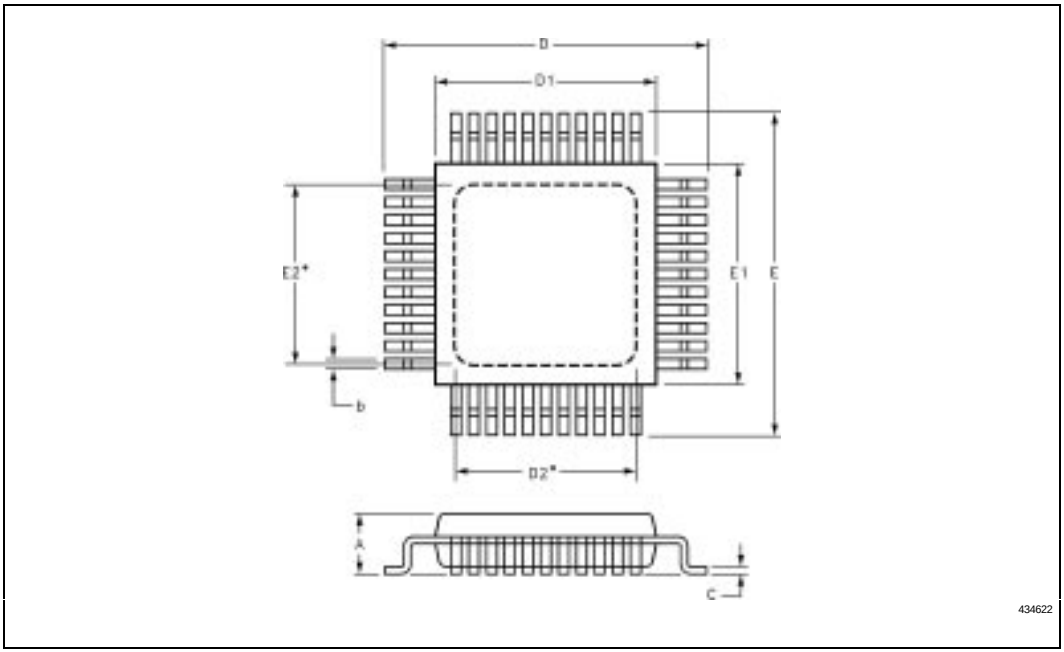

Figure 21. Dimensions Diagram for Table 23

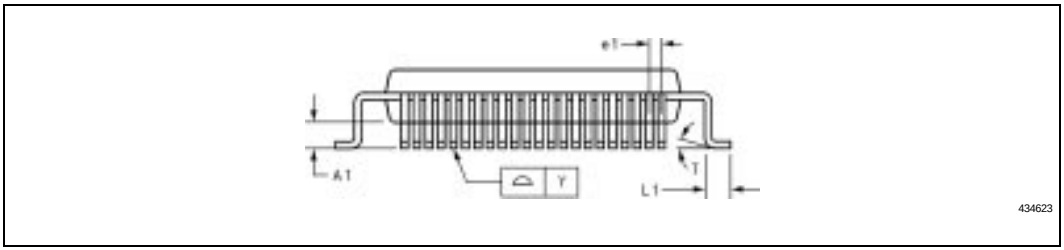

Figure 22. Terminal Dimensions for Table 23

Table 23. Quad Flatpack Dimensions*

Symbol	Description	Minimum	Maximum
A	Overall Height	3.25	3.75
A1	Standoff	0	0.30
b	Lead Width	0.20	0.40
c	Lead Thickness	0.150	0.188
D	Terminal Dimension	30.2	31.0
D1	Package Body	27.9	28.1
E	Terminal Dimension	30.2	31.0
E1	Package Body	27.9	28.1
e1	Lead Pitch	0.55	0.75
L1	Foot Length	0.60	1.0
T	Lead Angle	0°	10°
Y	Coplanairty	0.1	
Note: Dimensions are in millimeters.			

* These apply to Figure 21 and Figure 22.

8.0. REVISION HISTORY

The following chart outlines important changes made to the data sheet.

Date of Change	Section Number	Description
11-95	2.5	Added TAP information.
7-96	2.0	Figure 2 revised, Section 2.3 revised.
10-96	4.1.1.1	Figure 3 revised.
10-96	5.3.1.1	Table 7 revised to include ID numbers.