INTEL PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY MOBILE MODULE

- **Intel mobile Pentium® processor MMX™ technology with internal/bus frequencies of 133/66, 150/60 or 166/66 MHz**
- **Second-level cache of pipeline burst SRAM**
  - **Burst read/write at 3-1-1-1; back-to-back burst reads at 3-1-1-1-1-1-1-1**
  - **Supports up to 64MB of cacheable system memory (non-PCI memory)**
- **Supports ZZ snooze mode power management**
- **Processor (host) reference clock generation**
  - **Flexible clocking architecture provides system manufacturers with two clock modes**
- **Processor core voltage regulation supports input voltages**
  - **Above 90 percent peak efficiency**
- **Thermal transfer plate for heat dissipation**
- **Intel 430TX PCIset system controller**
  - **DRAM controller supports EDO and SDRAM at 3.3V**
  - **Provides PCI CLKRUN# signal to control memory clock on the PCI bus**
  - **SDRAM clock enable support and self refresh of EDO or SDRAM during Suspend mode**
  - **Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management; E_SMRAM mode supports write-back cacheable SMRAM up to 1MB**
  - **3.3V PCI bus control, Rev 2.1 compliant**
- **Active thermal feedback (ATF) sensing**
  - **Internal A/D - digital signaling (SMBUS) across the module interface**
  - **Programmable trip point interrupt or poll mode for reading temperature**

The Intel Pentium® processor with MMX™ technology Mobile Module is a small, highly integrated assembly containing an Intel mobile processor and its immediate system-level support. Specifically, the power supply for the processor's unique voltage requirements, the system Level 2 cache memory and the core logic required to bridge the processor to the standard system buses are on the module. The module interfaces electrically to its host system via a 3.3-volt PCI bus, a 3.3-volt memory bus and some Intel 430TX PCIset control signals.

The Intel Pentium processor with MMX technology may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Such errata are not covered by Intel's warranty. Current characterized errata are available on request.

February 1997

Order Number: 243328-001

CONTENTS

1.0. INTRODUCTION

The Intel Pentium® processor with MMX™ technology Mobile Module is the fundamental building block for a system manufacturer to incorporate into a notebook system. The Intel Mobile Module incorporates an Intel mobile Pentium processor, second-level cache, Intel 430TX PCIset Northbridge system controller, voltage regulator, and thermal sensor on a single printed circuit board.

Intel's PCIset architecture allows for physical partitioning at both the PCI and DRAM interfaces; therefore the electrical interconnect defined for the Intel Mobile Module includes the PCI bus, DRAM memory bus and some PCIset sideband signals. An onboard voltage regulator provides the DC conversion from the system manufacturer's system DC voltage to the processor's core voltage. This isolation of the processor voltage requirements allows the system manufacturer to incorporate Intel Mobile Modules with different processor variants into a notebook system.

Building around this modular design gives the system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards
- No requirement for manufacturing capabilities of Tape Carrier Package (TCP) processors
- Future Intel Mobile Modules provide an upgrade path for notebook designs using a standard interface

The 430TX PCIset (Northbridge) is one of two physical VLSI devices that constitute the Intel 430TX PCIset controller. The second 430TX device (Southbridge) is known as the PIIX4 ISA bridge. The system manufacturer's I/O Module, which connects to the Intel Mobile Module, must include a PIIX4 ISA bridge device. The PIIX4 ISA bridge provides extensive power management capabilities and is designed to support both the 430TX PCIset for current mobile Pentium processors and the next Northbridge device for the next generation of Intel mobile processors.

1.1. Architecture Overview

The Intel Mobile Module is a small, highly integrated assembly containing the Pentium processor with MMX technology with internal/bus frequencies of 133/66, 150/60 or 166/66 MHz and its immediate system-level support. The module interfaces electrically to its host system via a 3.3V PCI bus, a 3.3V memory bus and the Intel 430TX PCIset system controller.

The Intel Mobile Module includes a second-level cache of pipeline burst SRAM with capabilities to burst read/write at 3-1-1-1 and back-to-back burst reads at 3-1-1-1-1-1-1-1. The module supports up to 64 MB of cacheable system memory (non-PCI memory) and ZZ snooze mode power management.

The Intel Mobile Module contains key features of the Intel 430TX PCIset system controller. The DRAM controller supports EDO at 3.3V with a burst read at 5-2-2-2 (66 MHz, 60 ns) and SDRAM at 3.3V with a burst read at 6-1-1-1 (66 MHz, CL=2). The system controller provides a PCI CLKRUN# signal to control memory clock on the PCI bus as well as the internal clock control (also known as Chip Standby or Gated Clock). The SDRAM clock enables support and self refresh of EDO or SDRAM during Suspend mode and is fully compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management; E_SMRAM mode supports write-back cacheable SMRAM up to 1 MB. The Intel 430TX PCIset system controller is a 3.3V PCI bus control which is compliant with PCI Rev 2.1 specifications.

The processor core voltage regulation supports input voltages from 5V to 20V (+5 percent) enabling an above 90 percent peak efficiency and decouples processor voltage requirements from the system.

The Intel Mobile Module incorporates Active thermal feedback (ATF) sensing, ACPI Rev 0.95 compliant by including an internal A/D - digital signaling (SMBUS) across the module interface and a programmable trip point interrupt or poll mode for reading temperature.

A thermal transfer plate for heat dissipation from the processor provides a standard thermal attach point to which the system manufacturer connects a system heat pipe and heat spreader plate.

Figure 1 illustrates the block diagram of the Intel Mobile Module.

1.2. Intel Mobile Module Revision Identification

The Intel Mobile Module provides four dedicated connector pins for the sole purpose of identifying the revisions. These four pins allow up to 16 unique revision levels. The I/O Module can use these pins to determine a particular revision level of a Intel Mobile Module. System manufacturer software can query these revision ID bits, along with the 430TX PCIset, to provide complete revision level identification.

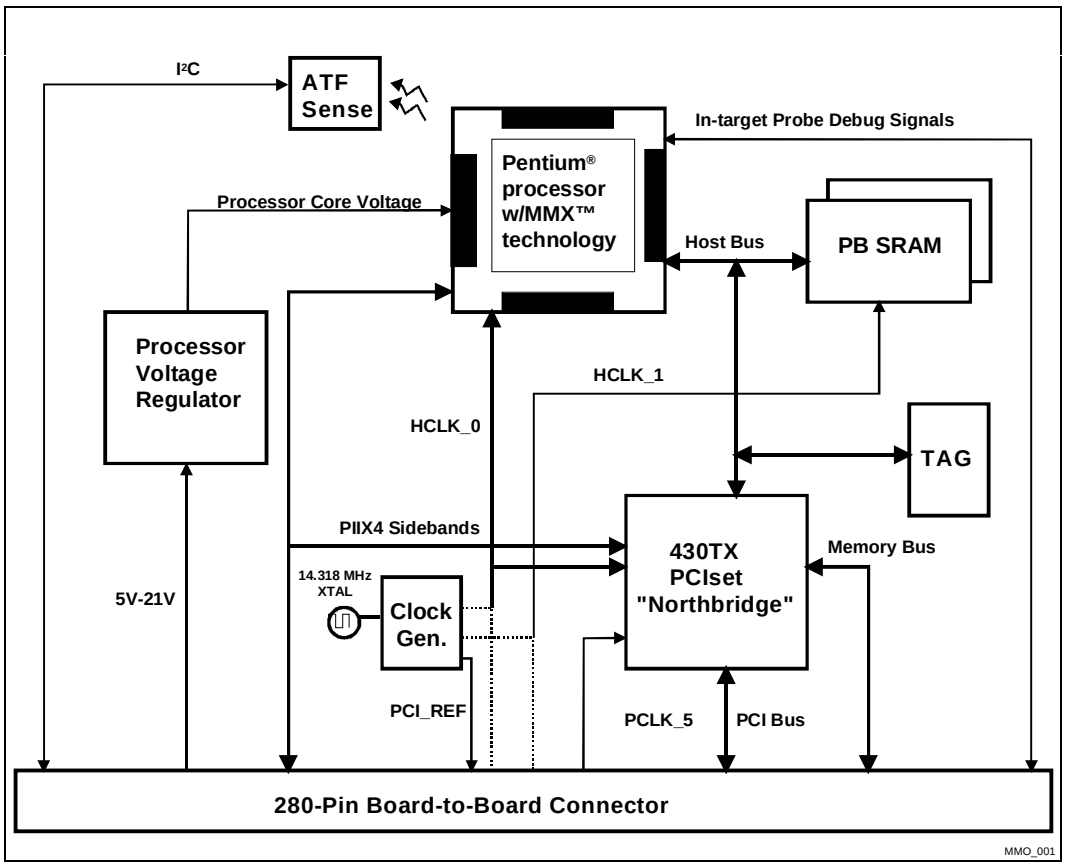

Figure 1. Block Diagram for the Intel Mobile Module

2.0. MODULE CONNECTOR INTERFACE

2.1. Signal Definitions

The Intel Mobile Module connector signals are defined with the intention of supporting future modules. Table 1 provides a list of signals by category and the corresponding number of signals in each category.

Table 1. Module Connector Signal Summary

Signal Group	Number
Memory	108
PCI	56
Processor/PIIX4 ISA bridge Sideband	9
Power Management	9
Clocks	8
Voltage: V_DC	10
Voltage: V_3S	20
Voltage: V_5S	1
Voltage: V_3	5
Voltage: V_CPUIO	3
ITP/JTAG	7
Misc. & Module ID	5
Ground	32
Reserved	7
Total	280

2.1.1. MEMORY (108 SIGNALS)

Table 2 lists the Intel Mobile Module memory interface signals. Some signals are defined as reserved for future use. Signals marked with an * are terminated with a 22Ω series resistor.

Table 2. Memory Signal Descriptions

Name	Type	Voltage	Description
MPD[7:0]	I/O	V_3S	**Memory Parity Data:** These signals connect to the DRAM parity. These pins are not implemented in the430TX PCIset and are reserved.
*RAS[5:0]# or CS[5:0]#	O	V_3S	**Row Address Strobe (EDO):** These pins select the DRAM row. **Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
*CAS[7:0]# or DQM[7:0]	O	V_3S	**Column Address Strobe (EDO):** These pins select the DRAM column. **Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
*MA[13:0]	O	V_3S	**Memory Address (EDO/SDRAM):** This is the row and column address for DRAM. These buffers now include programmable size selection, as controlled by the DRAMEC[MAD] bit. The 430TX PCIset implements (and the Intel Mobile Module supports) only MA[13:0]. See Figure 3 for more details.
*MWE[A,B]#	O	V_3S	**Memory Write Enable (EDO/SDRAM):** MWE[A,B]# should be used as the write enable for the memory data bus. Each copy is intended to support four rows, for loading purposes.
*SRAS[A,B]#	O	V_3S	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge. Each copy is intended to support four rows, for loading purposes. The SRASA signal is used to configure the Mobile Mode of the430TX PCIset. When the RST# signal is active, SRASA is an input. The Intel Mobile Module has a pull-down resistor so that SRASA is sampled low at the rising edge of RST#; thereby configuring the 430TX PCIset in Mobile Mode.
*SCAS[A,B]#	O	V_3S	**SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Each copy is intended to support four rows, for loading purposes.
*CKE[A,B]#	O	V_3S	**SDRAM Clock Enable (SDRAM):** SDRAM clock enable pin. When these signals are de-asserted, SDRAM enters power-down mode. Each copy is intended to support four rows, for loading purposes.
MD[63:0]	I/O	V_3S	**Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the Intel Mobile Module and it is recommended that the I/O Module provide series termination of 33Ω.

2.1.2. PCI (56 SIGNALS)

Table 3 lists the Intel Mobile Module's PCI interface signals.

Table 3. PCI Signal Descriptions

Name	Type	Voltage	Description
AD[31:0]	I/O	V_3S	**Address/Data:** The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
C/BE[3:0]#	I/O	V_3S	**Command/Byte Enable:** The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	I/O	V_3S	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O	V_3S	**Device Select:** This signal is driven by the 430TX PCIset when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O	V_3S	**Initiator Ready:** Asserted when the initiator is ready for data transfer.
TRDY#	I/O	V_3S	**Target Ready:** Asserted when the target is ready for a data transfer.
STOP#	I/O	V_3S	**Stop:** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O	V_3S	**Lock:** Used to establish, maintain and release resource locks on PCI.
REQ[3:0]#	I	V_3S	**PCI Request:** PCI master requests for PCI.
GNT[3:0]#	O	V_3S	**PCI Grant:** Permission is given to the master to use PCI.
PHLD#	I	V_3S	**PCI Hold:** This signal comes from the expansion bridge; it is the bridge request for PCI. The 430TX PCIset will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHLD# protocol has been modified to include support for passive release.
PHLDA#	O	V_3S	**PCI Hold Acknowledge:** This signal is driven by the 430TX PCIset to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR	I/O	V_3S	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]
SERR# (RESERVED)	O	V_3S	**System Error:** This signal is not implemented in the 430TX PCIset and is reserved for future modules.
CLKRUN#	I/O	V_3S	**Clock Run:** An open-drain output and also an input. The 430TX PCIset requests the central resource (PIIX4 ISA bridge) to start or maintain the PCI clock by asserting CLKRUN#. The 430TX PCIset tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset). An external 2.7K pullup resistor is required.
PCI_RST#	I	V_3S	**Reset:** When asserted, this signal asynchronously resets the 430TX PCIset. The PCI signals also tri-state, compliant with PCI Rev 2.0 and 2.1 specifications.

2.1.3. PROCESSOR/PIIX4 ISA BRIDGE SIDEBAND (9 SIGNALS)

Table 4 lists the Intel Mobile Module's processor and PIIX4 ISA bridge sideband signals at the connector interface. The voltage level for these signals is determined by V_CPUIO, which is supplied by the Intel Mobile Module. These signals are open-drain and should have a pullup resistor on the I/O Module.

Table 4. Processor/PIIX4 ISA Bridge Sideband Signal Descriptions

Name	Type	Voltage	Description
FERR#	O	V_CPUIO	**Numeric Coprocessor Error:** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4 ISA bridge.
CPURST	I	V_CPUIO	**Processor Reset:** The PIIX4 ISA bridge asserts CPURST to reset the processor. The PIIX4 ISA bridge asserts CPURST# during power-up and when a hard reset sequence is initiated through the RC register.
IGNNE#	I	V_CPUIO	**Ignore Error:** This signal is connected to the ignore error pin on the processor and is driven by the PIIX4 ISA bridge.
INIT#	I	V_CPUIO	**Initialization:** INIT is asserted by the PIIX4 ISA bridge to the processor for system initialization. **NOTE:** The system manufacturer should provide a pull up/pull down option on this pin, and connect this PIIX4 ISA bridge input to the Intel Mobile Module connector PIN BB38.
INTR	I	V_CPUIO	**Processor Interrupt:** INTR is driven by the PIIX4 ISA bridge to signal the processor that an interrupt request is pending and needs to be serviced.
NMI	I	V_CPUIO	**Non-Maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4 ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed.
A20M#	I	V_CPUIO	**Address Bit 20 Mask:** When enabled, this causes the processor to emulate the address wraparound at one Mbyte which occurs on the Intel 8086 processor.
SMI#	I	V_CPUIO	**System Management Interrupt:** SMI# is an active low synchronous output that is asserted by the PIIX4 ISA bridge in response to one of many enabled hardware or software events. The SMI# signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK.
STPCLK#	I	V_CPUIO	**Stop Clock:** STPCLK# is an active low synchronous output that is asserted by the PIIX4 ISA bridge in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCLK. When the processor samples STPCLK# asserted it responds by stopping its internal clock.

2.1.4. POWER MANAGEMENT (9 SIGNALS)

Table 5 lists the Intel Mobile Module's Power Management signals. The SM_CLK and SM_DATA signals refer to the two-wire serial SMBus interface.

Although this interface is currently used solely for the digital thermometer thermal sensor, there are reserved serial addresses for future use.

Table 5. Power Management Signal Descriptions

Name	Type	Voltage	Description
*OEM_PU	I	V_3	**OEM Pull-up:** A pullup resistor of 10K ohms is required on OEM_PU.
*L2_ZZ	I	V_CPUIO	**Low-Power Mode For Cache SRAM:** This pin is used to power down the L2 cache SRAMs . See PIIX4 ISA Bridge External Architecture Specification (Order Number XXXXXX) on ZZ. The I/O module is required to provide a pull up on this signal.
SUS_STAT#	I	V_3	**Suspend Status:** SUS_STAT# indicates the power supply state during Suspend-to-RAM (STR) mode.
VR_ON	I	V_3S	**VR_ON:** Voltage regulator on. This 3.3V signal controls the operation of the Intel Mobile Module's voltage regulator. This is generated from the PIIX4 ISA bridge SUSB# signal for controlling the "Suspend State B" voltage planes.
VR_PWRGD	O	V_3S	**VR_PWRGD:** Driven by the Intel Mobile Module to indicate the voltage regulator is stable. Can be used in some combination to generate the system PWRGOOD signal.
SM_CLK	I	V_3	**Serial Clock:** Clock signal used on the SMBUS - SMBus interface to the digital thermometer.
SM_DATA	I/O	V_3	**Serial Data:** Data signal on the SMBUS - SMBus interface to the digital thermometer.
*ATF_INT#	O	V_3	**ATF Interrupt:** Output signal of the digital thermometer. See National Semiconductor LM75 specification for pull up values.

NOTES:

Signals marked with an * are Open Drain and require the I/O module to Pull them up. The Intel Mobile Module does not provide a pullup or pulldown on these signals!

2.1.5. CLOCK (8 SIGNALS)

Table 6 lists the Intel Mobile Module's clock signals.

Table 6. Clock Signal Descriptions

Name	Direction	Voltage	Description
*OEM_PD	I	V_3	**OEM Pull-Down:** A pull-down resistor of 1K ohms is required on OEM_PD.
PCLK	I	V_3S	**PCI Clock In:** PCLK is an input to the module from the CKDM66-M clock source and is one of the system's PCI clocks. This clock is used by all of the 430TX PCIset logic in the PCI clock domain.This clock is stopped when the PIIX4 ISA bridge PCI_STP# signal is asserted.
HCLK[1:0]	I	V_CPUIO	**Host Clock In:** These pins are used solely for CKDM66-M Host clocking. This clock is used by the processor, 430TX PCIset and L2. This clock is stopped when the PIIX4 ISA bridge PCI_STP# signal is asserted.
SUSCLK	I	V_3	**Suspend Clock:** 32 KHz input for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh during suspend and non-suspend states is performed based on this clock.
FQS[1:0]	0	V_3S	**Frequency Status:** Provides status of the host clock frequency to the I/O Module. These signals are static and are pulled either low or high to the V_3S voltage. **FQS1 FQS0 Frequency** 0 0 60 MHz 0 1 66 MHz 1 0 Reserved 1 1 Reserved
CPU3.3_2.5#	O	V_CPUIO	**Clock Voltage Select:** Provides status to the I/O module about the voltage level at which the CKDM66-M clock generator should be operating.

2.1.6. VOLTAGES (36 SIGNALS)

Table 7 lists the Intel Mobile Module's voltage signal definitions.

Table 7. Voltage Descriptions

Name	Type	Number	Description
V_DC	I	10	**DC Input:** 5 - 20V +5%
V_3S	I	20	**Switched 3.3V:** Power-managed 3.3 voltage supply. An output of the I/O Module's voltage regulator.
V_5S	I	1	**Switched 5V:** Power-managed 5V voltage supply. An output of the I/O Module's voltage regulator.
V_3	I	2	**Non-Switched 3.3V:** 3.3 voltage supply that is always on. Used to power the refresh machine in the 430TX PCIset during Suspend-to-RAM (STR) mode.
V_CPUIO	O	3	**Processor I/O Ring:** Driven by the Intel Mobile Module to power processor interface signals such as the PIIX4 ISA bridge open-drain pullups for the processor/PIIX4 ISA bridge sideband signals.

2.1.7. ITP/JTAG (7 SIGNALS)

Table 8 lists the Intel Mobile Module's In-target Probe (ITP)/JTAG signals, which the I/O Module can use to implement a processor debug port. The system manufacturer can use debug port signals on development-level boards, or on production boards for manufacturing testability.

Refer to the *Intel Mobile Module Design Guide* (Order Number 243339) for further details on recommendations and requirements for a debug port.

Termination for the ITP signals must be done on the I/O Module. The Intel Mobile Module does not provide series termination for these signals.

Table 8. ITP/JTAG Pins

Name	Type	Voltage	Description
TDO	O	V_CPUIO	**JTAG Test Data Out:** Serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	V_CPUIO	**JTAG Test Data In:** Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	V_CPUIO	**JTAG Test Mode Select:** Controls the TAP controller change sequence.
TCLK	I	V_CPUIO	**JTAG Test Clock:** Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	V_CPUIO	**JTAG Test Reset:** Asynchronously resets the TAP controller in the processor.
ITP(1:0) ITP1: PRDY ITP0: R/S#	 O I	V_CPUIO	**Debug Port Signals:** Currently defined for the generation of Pentium® processors. Future uses are not yet defined.

NOTE:
ITP(1:0) are used to define two pins for the debug port. At this time, these signals are defined as follows for Pentium® processors:

ITP1: PRDY
ITP0: R/S#

2.1.8. MISCELLANEOUS (49 SIGNALS)

Table 9 lists the Intel Mobile Module's miscellaneous signal pins.

Table 9. Miscellaneous Pins

Name	Type	Number	Description
Module ID	O	4	Module Revision ID
PPP_PP#	O	1	Pentium® Pro processor or Pentium processor present. A high on this signal indicates to the PIIX4 ISA bridge CONFIG1 pin that the processor is based on the Pentium Pro architecture, a low indicates that it is of the Pentium processor family. This signal is not connected on Pentium Pro processor modules and grounded on Pentium processor modules; the system electronics should provide a pull up.
Ground	I	32	Ground
Reserved	RSVD	10	Unallocated Reserved Pins

2.2. Connector Pin Assignments

Table 10 lists the signals for each pin of the connector from the Intel Mobile Module to the I/O Module. Refer to Section 2.3 for the pin assignments of the pads on the connector.

Table 10. Connector Pin Assignments

Pin#	Row AA	Row AB	Row BA	Row BB
1	Gnd	Gnd	Gnd	Gnd
2	MD00	MD32	MID0	MID1
3	MD01	MD33	Reserved	Reserved
4	MD02	MD34	V_DC	V_DC
5	MD03	MD35	V_DC	V_DC
6	V_3S	V_3S	V_DC	V_DC
7	MD04	MD36	V_DC	V_DC
8	MD05	MD37	V_DC	V_DC
9	MD06	MD38	Reserved	Reserved
10	MD07	MD39	MID2	MID3
11	Gnd	Gnd	Gnd	Gnd
12	CAS0#/DQM0	CAS4#/DQM4	AD00	FRAME#
13	CAS1#/DQM1	CAS5#/DQM5	AD01	LOCK#
14	MA00	MA01	AD02	DEVSEL#
15	CKEA	CKEB	AD03	IRDY#
16	V_3S	V_3S	V_3S	V_3S
17	MA02	MA04	AD04	TRDY#
18	MA03	MA05	AD05	STOP#
19	MD08	MD40	AD06	PHLD#
20	MD09	MD41	AD07	PHLDA#
21	Gnd	Gnd	Gnd	Gnd
22	MD10	MD42	AD08	PCI_RST#
23	MD11	MD43	AD09	PAR
24	MD12	MD44	AD10	SERR#
25	MD13	MD45	AD11	REQ0#

Table 10. Connector Pin Assignments (Continued)

Pin	Row AA	Row AB	Row BA	Row BB
26	V_3S	V_3S	V_3S	REQ1#
27	MD14	MD46	AD12	REQ2#
28	MD15	MD47	AD13	REQ3#
29	SRASA#	SCASA#	AD14	GNT0#
30	SRASB#	SCASB#	AD15	GNT1#
31	Gnd	Gnd	Gnd	Gnd
32	MWEA#	MPD0	AD16	GNT2#
33	MWEB#	MPD4	AD17	GNT3#
34	RAS0#/CS0#	MPD1	AD18	L2_ZZ
35	RAS1#/CS1#	MPD5	AD19	Reserved
36	V_3S	V_3S	V_3S	V_3S
37	MD16	MPD2	AD20	Reserved
38	MD17	MPD6	AD21	PPP_PP#
39	MD18	MPD3	AD22	CLKRUN#
40	Gnd	Gnd	Gnd	Gnd
41	MD19	MPD7	RAS2#/CS2#	SM_CLK
42	MD20	MD48	RAS3#/CS3#	SM_DATA
43	MD21	MD49	RAS4#/CS4#	ATF_INT#
44	MD22	MD50	RAS5#/CS5#	SUSCLK
45	V_3S	V_3S	V_3	V_3
46	MD23	MD51	AD23	SUS_STAT#
47	MA06	MD52	AD24	V_3
48	MA07	MD53	AD25	OEM_PU
49	MA08	MD54	AD26	VR_ON
50	Gnd	Gnd	Gnd	Gnd
51	MA09	MD55	AD27	VR_PWRGD
52	CAS2#/DQM2	CAS6#/DQM6	AD28	V_3
53	CAS3#/DQM3	CAS7#/DQM7	AD29	V_3

Table 10. Connector Pin Assignments (Continued)

Pin#	Row AA	Row AB	Row BA	Row BB
54	MA10	RAS4#/CS4#/MA12	AD30	Reserved
55	V_3S	V_3S	V_3S	Reserved
56	MA11	RAS5#/CS5#/MA13	AD31	INIT#
57	MD24	MD56	C/BE0#	V_CPUIO
58	MD25	MD57	C/BE1#	INTR
59	MD26	MD58	C/BE2#	CPURST
60	Gnd	Gnd	Gnd	Gnd
61	MD27	MD59	C/BE3#	STPCLK#
62	MD28	MD60	IGNNE#	SMI#
63	MD29	MD61	FERR#	NMI
64	MD30	MD62	A20M#	V_5S
65	MD31	MD63	V_CPUIO	V_CPUIO
66	V_3S	V_3S	TDO	TRST#
67	OEM_PDPCI_REF	PCLK	ITP0	TDI
68	FQS0	FQS1	ITP1	TMS
69	HCLK1	HCLK0	CPU2.5_3.3# CPU3.3_2.5#	TCLK
70	Gnd	Gnd	Gnd	Gnd

NOTE:

Pins AB54 and BA43 are connected together on the Intel Mobile Module, and Pins AB56 and BA44 are connected together on the Intel Mobile Module. Future PCIsets will independently drive address and RAS signals separately, so caution should be taken when connecting to this interface.

2.3. Connector Footprint

This section contains the 280-pin connector pad assignment.

2.3.1. PIN AND PAD ASSIGNMENT

Figure 2 shows the connector pad assignments for the system manufacturer I/O Module. This footprint is viewed from the primary side of the I/O Module (the side of the printed circuit board on which the 280-pin connector is soldered). For orientation of the connector with respect to the Intel Mobile Module, refer to the *Intel Mobile Module Design Guide* (Order Number 243339).

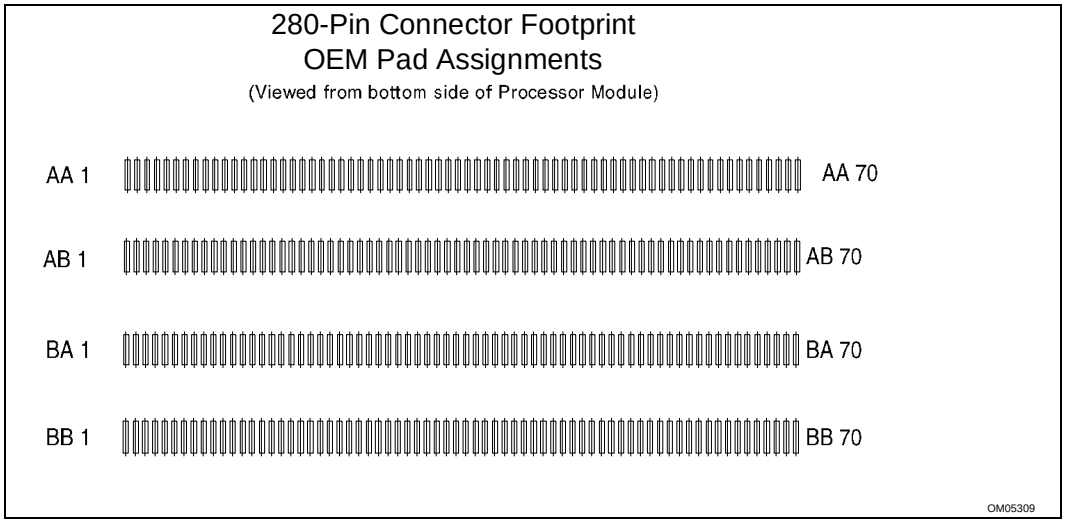

Figure 2. 280-Pin Connector Footprint Pad Numbers, I/O Module Primary Side

2.4. Connector Specifications

The Intel Mobile Module connector is a surface mount, 0.6 mm pitch, 280-pin connector. There are currently four unique connectors that will be offered by vendors for the Intel Mobile Module.

Table 11 summarizes some of the more critical specifications for the connector.

Table 11. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Copper Alloy
	Housing	Thermo Plastic Molded Compound: LCP
Electrical	Current	0.4 A
	Voltage	50 VAC
	Insulation Resistance	100MΩ min. @ 500 VDC
	Termination Resistance	20mΩ max. @ 20mV open circuit with 10mA
	Capacitance	5pF max. Per contact
Mechanical	Mating Cycles	50 cycles
	Connector Mating Force	0.9N (90gf) max. Per contact
	Contact Un-mating Force	0.1N (10gf) min. Per contact

3.0. FUNCTIONAL DESCPRIPTION

3.1. Intel Mobile Module

The Intel Mobile Module will support the mobile Pentium processor with MMX technology processors running at 133/66, 150/60 MHz and 166/66 MHz with 16 KB on-chip code and data cache sizes.

3.2. L2 Cache

The mobile Pentium processor's internal cache is complimented with a second-level cache using a high-performance pipeline burst SRAM. The L2 cache can support up to 64 MB of system memory, the maximum amount of cacheable system memory supported by the 430TX PCIset system controller. The Intel Mobile Module has two 100-pin TSOP (Thin Small Outline Package) footprints for 256K direct-mapped write-back L2 cache.

The Intel Mobile Module supports the ZZ, or snooze mode power management features in current pipeline burst SRAM (PBSRAM). The PIIX4 ISA bridge Southbridge component on the I/O Module is the source for the generation of ZZ mode. This ZZ signal is named L2_ZZ on the Intel Mobile Module interface, clarifying its sole purpose of ZZ support for second-level cache.

3.3. 430TX PCIset System Controller

Intel's 430TX PCIset system controller is a highly integrated device that combines the mobile Pentium processor bus controller, the DRAM controller, second-level cache controller and PCI bus controller into one component. The 430TX PCIset has multiple power management features specifically for notebook systems:

- CLKRUN# is a feature that enables controlling of the PCI clock on or off
- 430TX PCIset suspend modes include Suspend to RAM (STR), Suspend to Disk (STD) and Powered On Suspend (POSA)
- System Management RAM (SMRAM) power management modes include Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). C_SMRAM is the traditional SMRAM feature implemented in all Intel PCI chipsets. E_SMRAM is a new feature that supports write-back cacheable SMRAM space up to 1Mbyte. To minimize power consumption while the system is idle, the internal 430TX PCIset clock is turned off (gated off) when there is no processor and PCI activity.

The Intel Mobile Module supports only the 430TX PCIset features available in the Mobile Mode of operation. Refer to Intel's latest revision of the 430TX PCIset specification for complete details.

3.3.1. MEMORY ORGANIZATION

The complete memory interface of the 430TX PCIset is available at the Intel Mobile Module's connector; all of the 430TX PCIset Mobile Mode memory configurations and modes of operation are supported. Two memory features not supported by the 430TX PCIset Mobile Mode are Parity and Error Detection and Correction (EDC).

NOTE

The Intel Mobile Module does not support the use of fast page mode (FPM) memory on the I/O Module.

DRAM technologies supported by 430TX PCIset include Extended Data Out (EDO) and SDRAM. These memory types may be mixed in the system, but only on a row-by-row basis. In other words, all DRAM in a particular row (RAS[5:0]#) must be of the same technology. The 430TX PCIset targets 60ns DRAMs, but also supports 50 ns and 70 ns components.

The Intel Mobile Module's clocking architecture supports the use of SDRAM. Due to the tight timing requirements of 66-MHz SDRAM clocks, the clocking mode for SDRAM or system manufacturer custom memory configurations allows all host and SDRAM clocks to be generated from the same physical device on the system manufacturer I/O Module. Driving all of these clocks out of a single device ensures minimal skew and jitter between clock outputs. For complete details about using SDRAM memory, and for trace length guidelines, refer to the *Intel Mobile Module Design Guide* (order number 243339).

For details on memory device support, organization, size and addressing, refer to 430TX PCIset documentation and PCD application notes.

3.3.2. 64-MBIT SDRAM SUPPORT

Support for 64-Mbit SDRAM memory technology is provided by the 430TX PCIset Northbridge component. See the 430TX PCIset documentation for operational details on how this support is implemented by the component. To provide the equivalent support at the Intel Mobile Module connector and maintain compatibility with future Northbridge architectures, the memory signals on the Intel Mobile Module are routed to the connector as shown in Figure 3.

Memory control signals that allow the 430TX PCIset to support 64-Mbit SDRAM memory devices are RAS4/MA12 and RAS5/MA13. These signals are multiplexed within the 430TX PCIset to signals RAS4# and RAS5# respectively (these signals are configurable through the 430TX PCIset configuration registers). Figure 3 shows a wiring diagram on the Intel Mobile Module of the RAS4/MA12 and RAS5/MA13 signals for clarification. In order to support 64-Mbit SDRAM technologies, MA12 and MA13 should be routed to the upper address lines of the SO-DIMM sockets (note that supporting 64-Mbit technologies limits the I/O Module design to four banks of memory).

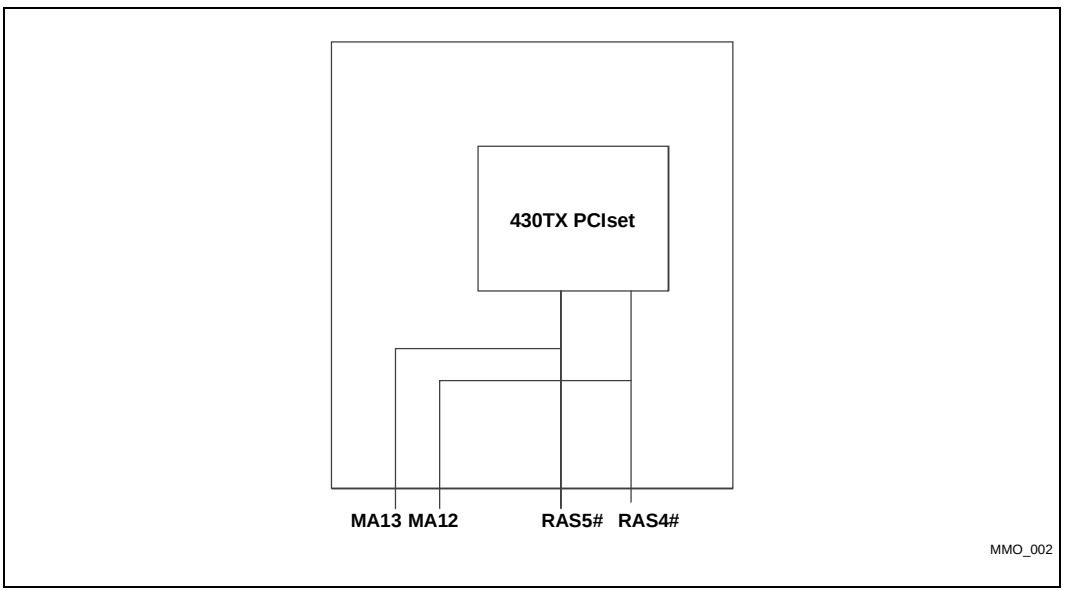

Figure 3. Pentium® Processor Address Routing

If the I/O planar is designed to support four banks of memory and 64-Mbit SDRAM memory devices, the system manufacturer should route the upper two address signals from the Intel Mobile Module's address pins MA[12:13], and not the RAS[4:5]# pins. Subsequently if the I/O design supports six banks of memory and does not intend to support 64-Mbit memory devices, then RAS[4:5]# for Banks 4 and 5 should be routed from the Intel Mobile Module's RAS[4:5]# pins.

Even though these two sets of Intel Mobile Module pins are electrically equivalent on the module, connecting the memory address and control signals as suggested will help maintain compatibility with future modules.

The 430TX PCIset does not support six banks of memory and 64-Mbit SDRAM devices simultaneously, however, future PCIsets may provide this flexibility. To design today for this type of upgrade, it is recommended that Q-switches be used on either the RAS[4:5]# or MA[12:13] signals, or both. This would ensure that the trace lengths of the RAS signals are kept to a minimum, and signal quality is not compromised.

3.3.3. PCI INTERFACE

The 430TX PCIset is compliant with the PCI 2.1 specification, which improves the worst-case PCI bus access latency from earlier PCI specifications. The complete PCI interface of the 430TX PCIset is available at the Intel Mobile Module's connector. The 430TX PCIset supports the PCI Clockrun protocol for power management of PCI. In this protocol, PCI devices assert the CLKRUN# open-drain signal when they require the use of the PCI interface. (Refer to the PCI Mobile addendum for complete details on the PCI Clockrun protocol.)

The 430TX PCIset is responsible for arbitrating the PCI bus. When configured in Mobile Mode, the 430TX PCIset can support up to four PCI bus masters. There are four PCI Request/Grant pairs, REQ[3:0]# and GNT[3:0]# available on the connector to the system manufacturer I/O Module.

The 430TX PCIset supports only Mechanism #1 for accessing PCI configuration space, as detailed in the PCI specification. This implies that signals AD[31:11] are available for PCI IDSEL signals. However, since the 430TX PCIset is always device #0; AD11 will never be asserted during PCI configuration cycles as an IDSEL. Thus, AD12 is the first available address line usable as an IDSEL.

3.4. Processor Core Voltage Regulation

The Intel Mobile Module's DC voltage regulator (DC/DC converter) is designed to support the core voltage and I/O ring voltage for current and future processors. Current processors have a 3.3V I/O ring voltage, so currently the only voltage regulation is for the processor's core voltage. The same regulator will also support future processors whose I/O ring voltage is not 3.3V. In all cases, the processor's core voltage will be supplied, and if the I/O ring voltage is not 3.3V, the regulator will supply the correct voltage.

The Intel Mobile Module supports an input DC voltage range of 5V - 20V (+5 percent) from the system battery/power supply. Maximum peak input voltage is 21.1V including ripple.

3.4.1. VOLTAGE REGULATOR EFFICIENCY

The voltage regulator is optimized for Pentium processors and is most efficient in the 1A to 3A range. When placed in suspend mode, the module will consume approximately 20mW. See Table 12 for details over the entire current range.

Table 12. Typical Voltage Regulator Efficiency

Vin	Iin	Vout	Iout	Efficiency %	V_5	I_5
5	0.269	2.476	0.5	90.70	5	0.004
5	0.527	2.4642	1	92.81	5	0.004
5	1.072	2.460	2	91.45	5	0.004
5	1.649	2.4563	3	89.16	5	0.004
5	2.257	2.4526	4	86.78	5	0.004
5	3.101	2.4647	5	79.38	5	0.004
8	0.176	2.4774	0.5	86.74	5	0.004
8	0.34	2.4758	1	90.36	5	0.004
8	0.684	2.474	2	90.09	5	0.004
8	1.049	2.4723	3	88.17	5	0.004
8	1.436	2.4706	4	85.87	5	0.004
8	1.846	2.4689	5	83.48	5	0.004
12	0.126	2.4792	0.5	80.91	5	0.004
12	0.231	2.4708	1	88.50	5	0.004
12	0.457	2.4674	2	89.66	5	0.004
12	0.698	2.4648	3	86.71	5	0.004
12	0.952	2.4627	4	86.08	5	0.004
12	1.239	2.4735	5	83.07	5	0.004
18	0.093	2.484	0.5	73.32	5	0.004
18	0.159	2.474	1	85.84	5	0.004
18	0.311	2.4731	2	88.04	5	0.004
18	0.474	2.4717	3	86.71	5	0.004
18	0.646	2.4716	4	84.88	5	0.004
18	0.854	2.482	5	80.63	5	0.004

NOTE:
These efficiencies will change with future voltage regulators that accommodate higher input voltages.

3.4.2. VOLTAGE REGULATOR CONTROL

The VR_ON pin on the connector allows a digital signal (3.3V, 5V safe) to control the voltage regulator. The system manufacturer can use this signal to turn the Intel Mobile Module's voltage regulator on or off. VR_ON should be controlled with the same digital control signal used to control the system's switched 5V/3.3V regulator. The PIIX4 ISA bridge defines Suspend B as the power management state in which power is physically removed from the processor, L2 cache and 430TX PCIset. In this state, the SUSB# pin on the PIIX4 ISA bridge controls these power planes.

From the assertion of VR_ON, the voltage regulator has a turn-on time latency of approximately 6ms. In order to bring both the processor's core and I/O ring voltages up together, the system manufacturer must ensure that the system's switched 3.3V supply (voltage plane V_3S) turns on and off with the Intel Mobile Module's core voltage. This requires proper sequencing of the system's voltage regulator and the VR_ON signal.

The Intel Mobile Module also provides the VR_PWRGD signal, which indicates that the voltage regulator power is operating at a stable voltage level. The system manufacturer should use this signal on the I/O Module to control power inputs, and gate PWROK to the PIIX4 ISA bridge.

See the *Intel Mobile Module Design Guide* (Order Number 243339) for more details about the voltage regulator and voltage signal sequencing.

3.5. Active Thermal Feedback

Table 13 identifies three addresses allocated for the System Management Bus (SMBus) on the Intel Mobile Module. Two of these addresses are reserved for future use.

Table 13. LM75 SMBUS Address Table

Function	Fixed Address AD Bits (6:3)	Selectable Address AD Bits (2:0)
LM75 Thermal Sensor	1001	000
Reserved	1001	001
Reserved	1001	010

NOTES:

The LM75 is not compliant with SMBus addressing. The 4-bit fixed address used by the LM75 is invalid under Revision 1.0 of the System Management Bus Specification from Intel.

After consulting your local Intel sales representative, refer to the datasheet for the LM75 digital thermometer for complete device programming details.

3.6. Thermal Transfer Plate

The Intel Mobile Module provides a thermal transfer plate connected to the processor in a standard position called the thermal attach point. The thermal attach point is a fixed location relative to the mounting holes and other physical datum on the Intel Mobile Module. The system manufacturer can use both a heat pipe and a heat spreader plate in contact with the thermal attach point to transfer heat through the notebook system.

The thermal transfer plate is physically mounted to the Intel Mobile Module, and may be different from one generation of Intel Mobile Module to the next. However, the thermal attach point will remain fixed across future generations of Intel Mobile Modules. Figure 4 shows the conceptual relationship between the circuit board, thermal transfer plate and thermal attach point. Refer to the *Intel Mobile Module Design Guide* (Order Number 243339) for complete mechanical details of the thermal transfer plate and thermal attach point.

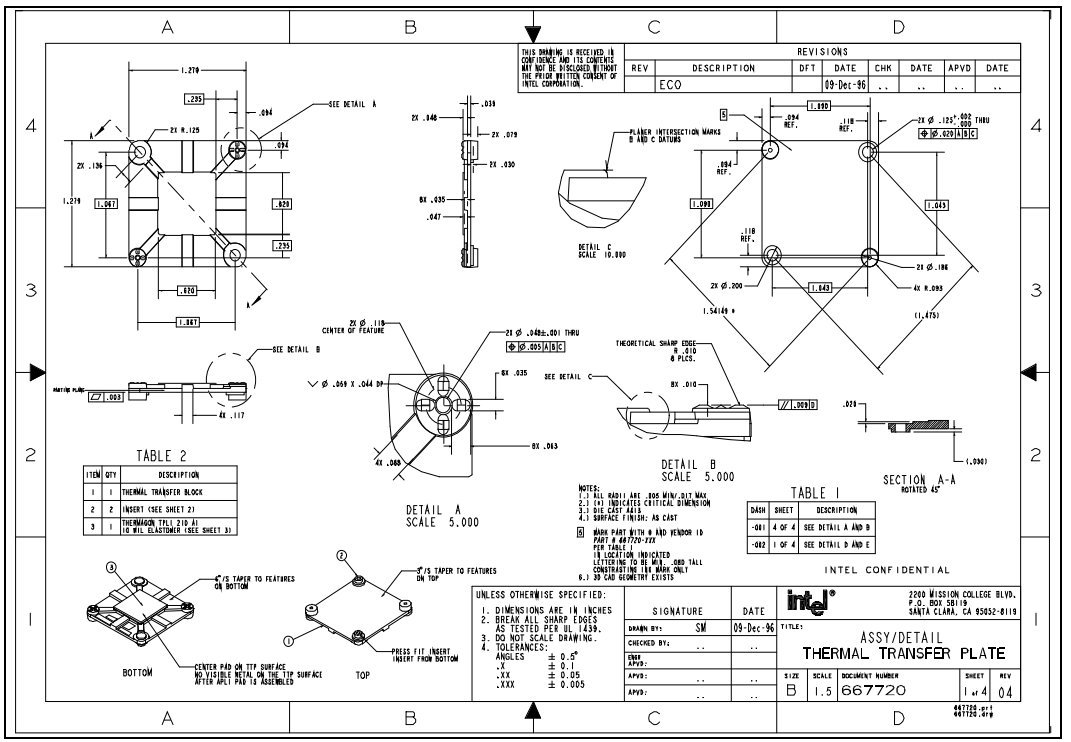

Figure 4. Intel Mobile Module Thermal Transfer Plate

4.0. MECHANICAL REQUIREMENTS

4.1. Module Dimensions

This section provides the physical dimensions for the Intel Mobile Module

4.1.1. BOARD AREA

Figure 5 shows the board dimensions and the connector orientation for the Intel Mobile Module . These dimensions are necessary to accommodate the next generation of Intel mobile processor and PCI Northbridge chipset controller.

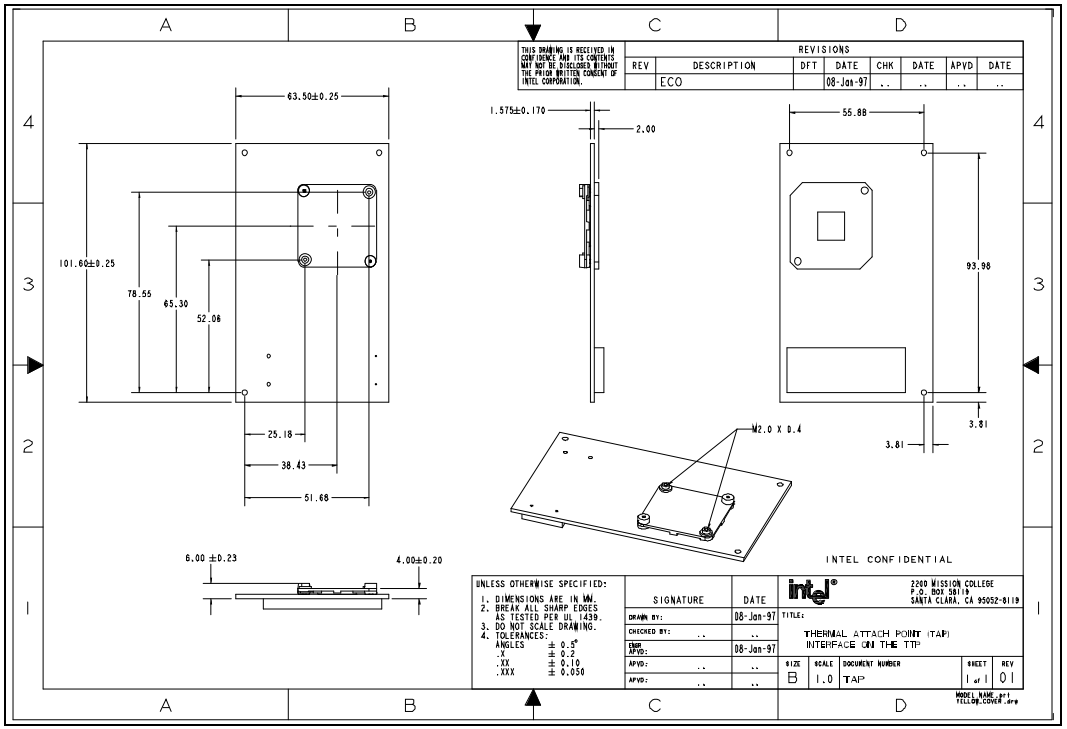

Figure 5. Board Dimensions with 280-Pin Connector Orientation

4.1.2. PRINTED CIRCUIT BOARD THICKNESS

Figure 6 shows the Intel Mobile Module profile and the associated minimum and maximum thickness of the printed circuit board (PCB). The range of PCB thickness allows for different PCB technologies to be used with current and future modules.

NOTE

The system manufacturer must ensure that the mechanical restraining method and/or system-level EMI contacts are able to support this range of PCB thickness, to ensure compatibility with future modules.

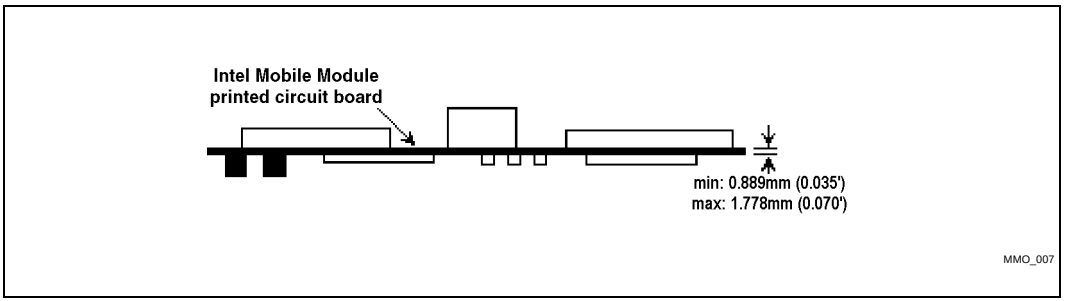

Figure 6. PCB Board Thickness

4.1.3. HEIGHT RESTRICTIONS

Figure 7 shows the Intel Mobile Module mechanical stackup and associated component clearance requirements.

The system manufacturer establishes the board-to-board clearance between the Intel Mobile Module and the I/O Module by selecting one of three possible mating connectors. The mating connectors provide board-to-board clearance distances of 4 mm, 6 mm or 8 mm. With these three options, the system manufacturer has reasonable flexibility in choosing components on the I/O Module that are between the two boards.

NOTE

The Intel Mobile Module top side component clearance is referenced from the bottom of the PCB, so it is independent of the PCB thickness.

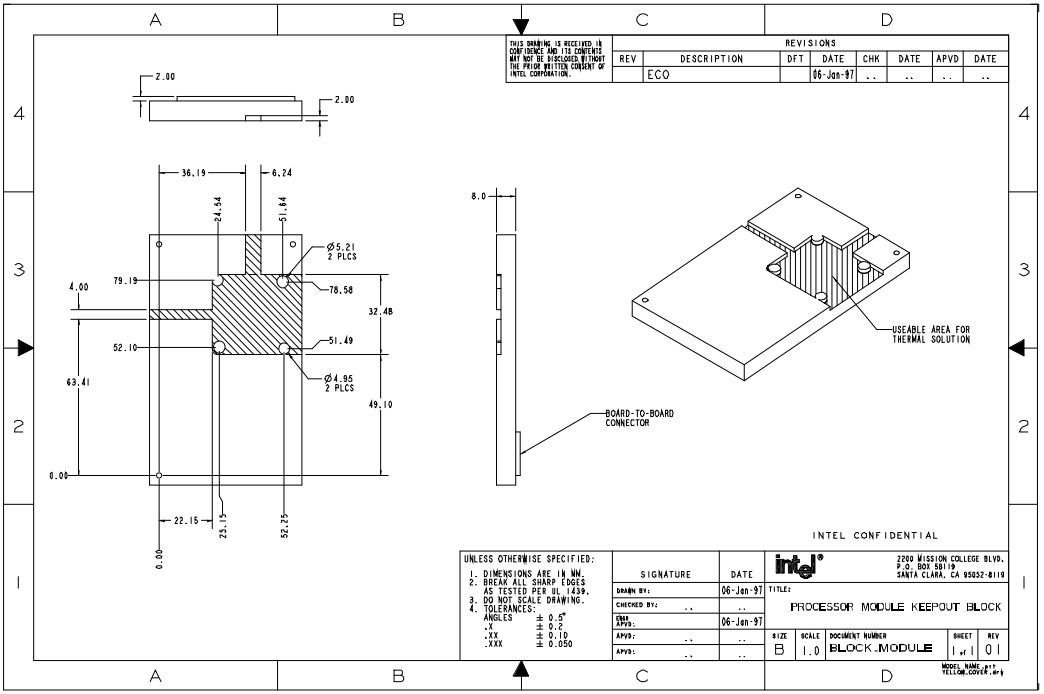

Figure 7. 3-D Mechanical Drawing

4.2. Module Physical Support

Figure 8 shows the Intel Mobile Module standoff support hole patterns and the board edge clearance around the perimeter of the module. These hole locations and board edge clearances will remain fixed for all Intel Mobile Modules. The hole patterns and board edge clearance lets the system manufacturer develop several methods for mechanically supporting the Intel Mobile Module within a particular notebook system.

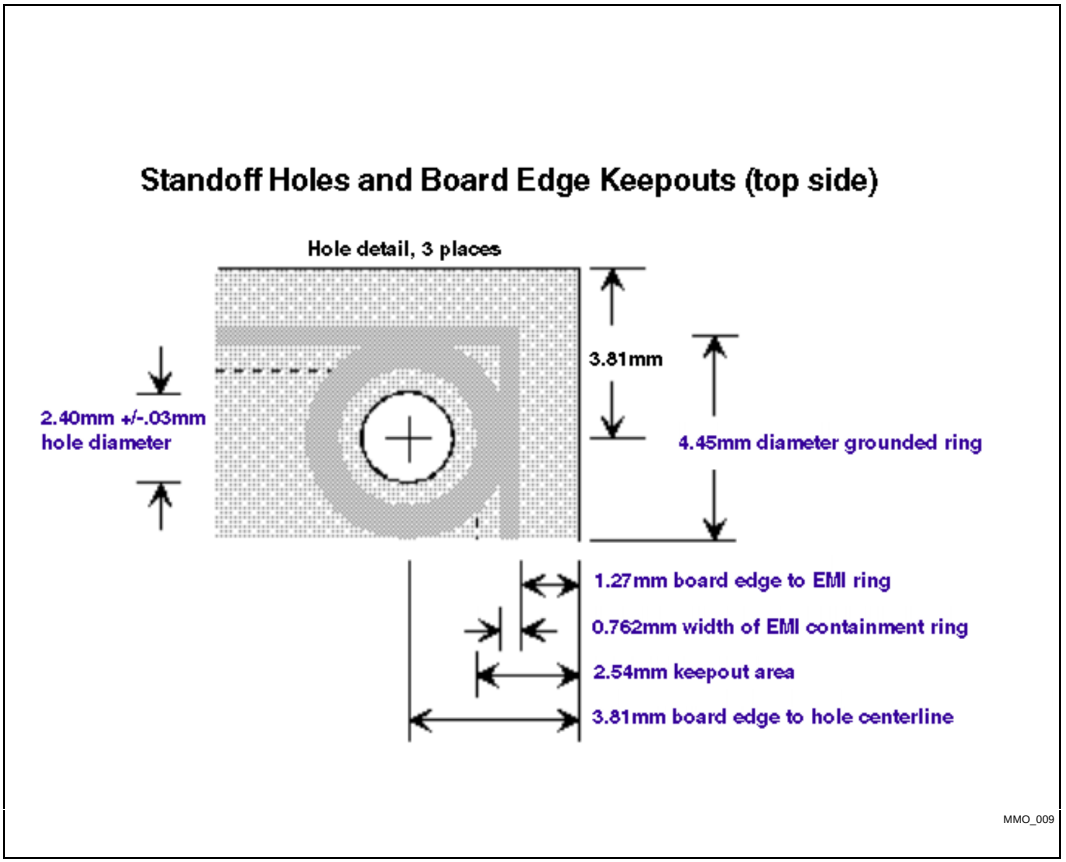

Figure 8. Standoff Holes, Board Edge Clearance and EMI Containment Ring

The board edge clearance includes a 0.762 mm (0.030 in) width EMI containment ring around the perimeter of the module. This ring is on each layer of the module PCB and is grounded. On the surface of the module, the metal is exposed for EMI shielding purposes. The hole patterns placed on the module also have a plated surrounding ring and one can use a metal standoff to contact the ring for EMI shielding purposes. Figure 8 shows the dimensions of the EMI containment ring and the keepout area. No components are placed on the board in the keepout area.

5.0. ENVIRONMENTAL STANDARDS

The environmental standards for this product are being developed. Table 14 provides the parameter list to which specifications will be defined.

Table 14. Environmental Standards

Parameter	Condition	Specification
Temperature	Non-Operating	-40°C to 70°C
	Operating	0°C to 55°C
Humidity		95% relative humidity at 30 °C
Voltage	V_DC	+/- 5%
	V_3S	+/- 5%
	V_3	+/- 5%
Shock	Operating	Half Sine, 2G, 11msec
	Unpackaged	Trapezoidal, 30G, 11msec
	Packaged	Inclined Impact at 5.7ft/s
	Packaged	Half Sine, 2msec at 42” Simulated Free Fall
Vibration	Unpackaged	5Hz to 500Hz 2.2gRMS random
	Packaged	10Hz to 500Hz 1.0gRMS
	Packaged	11,800 impacts 2Hz to 5Hz (low frequency)
ESD	Air Discharge	0 to 2kV (no detectable err)
		0 to 8kV (no intermittent err)
		0 to 20kV (no hard failures)