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APPLICATION NOTE

Voltage Guidelines For Pentium® Processors With MMX™ Technology

October 1996

Order Number: 243186-001

CONTENTS

FIGURES

TABLES

1.0. INTRODUCTION

This document explains the voltage specifications, recommends solutions for supplying consistent power, and suggests validation techniques to ensure robust Pentium® processor with MMX™ technology-based systems.

The Pentium processor with MMX technology uses a split power plane with separate voltage islands for the core and I/O. The split power plane has separate V_{CC2} pins connected to the core voltage island, while the V_{CC3} pins are connected to the I/O voltage island.

This document contains guidelines for measuring V_{CC} Noise levels on the V_{CC2} (2.8V) plane of the Pentium processor with MMX technology. The document outlines measurement procedures for a Pentium processor with MMX technology system running at 200 MHz. The V_{CC2} specification for the core is the 2.7V-2.9V range. The V_{CC3} specification for the I/O voltage island uses the standard 3.3V range from 3.135-3.6V. For voltage transient measurement information on Pentium processors, refer to the application note *Implementation Guidelines for Pentium® Processors with VRE Specifications*, Order Number 242687.

This document contains six key sections:

- Section 2.0 discusses the core and I/O specifications. This chapter also gives an overview of some important system design and voltage measurement considerations associated with V_{CC}. The consequences of specification violations are also discussed.
- Section 3.0 deals with the power supply and regulation. It contains voltage regulator and power supply recommendations to ensure a robust system design. In addition, this chapter contains detailed bulk and high-speed decoupling recommendations for Pentium® processor designs.
- Section 4.0 explains the proper measurement techniques to verify that systems meet their respective voltage specifications. These measurement techniques apply to all Pentium processors. Sample measurement results are shown in this chapter.
- Appendix A provides information on how to obtain and use the recommended “stress” code for voltage noise measurements.
- Appendix B provides a list of third party vendors. These vendors include suppliers of regulators, resistors, capacitors, and sockets
- Appendix C provides worksheets for recording measurements.

2.0. SPECIFICATIONS

2.1. The CORE and I/O Specification

The Pentium processor with MMX technology has a split power plane with the core operating at 2.8V and the I/O operating at 3.3V. The VCC2DET# pin defined on the Pentium processor with MMX technology is used to indicate to the voltage regulator the correct CPU core voltage of 2.8V (V_{CC2} plane). The I/O should meet the standard 3.3V specifications for the voltage supply requirements. Both the core and I/O have strict V_{CC} requirements and are very sensitive to voltage supply noise and transients.

NOTE

Any overshoot or undershoot beyond the voltage range (at a measurement bandwidth of 20 MHz) is outside specifications. Transient excursions beyond the specified voltage range may result in unstable system behavior. The measuring techniques are also specified in Section 4.0 and should be followed to ensure consistent and accurate measurements. The complete specifications shown above must be met to ensure a robust Pentium processor with MMX technology-based platform.

All measurements must be made and guaranteed at the back of the motherboard at the CPU socket pins. The voltage specifications assume an oscilloscope measurement bandwidth of 20 MHz. For complete measurement specifications, see Section 4.4.

Table 1. Core and I/O Specifications for Pentium® Processors with MMX™ Technology

Specifications	Core	I/O
V_{CC}	**2.7 to 2.9V** No overshoot or undershoot allowed	**3.135V to 3.6V** No overshoot or undershoot allowed
Measurement	Measurements must be taken in accordance with the procedures outlined in Section 4.4. Transients must be measured and guaranteed at the back of the motherboard at the CPU socket pins.	

2.1.1. THE SUPPLY VOLTAGE RANGE

To compensate for the small transient tolerance, platforms must use accurate voltage regulators and adequate local decoupling capacitors. During worst-case transient conditions (transition into and out of Stop Grant Mode or Halt Power Down Mode), current supplied to the processor can change by several amperes in tens of nanoseconds. Since power supply units and voltage regulators can, at best, respond in a time frame on the order of milliseconds, bulk decoupling capacitors are required to act as current reservoirs until the power supply unit or voltage regulators compensate for the new load. Due to the high-speed operation of the Pentium processor, high-frequency capacitors are also required to filter the excessive noise components. Failure to provide adequate power regulation during any transient conditions may result in undershoot and overshoot beyond the voltage specifications of the processor.

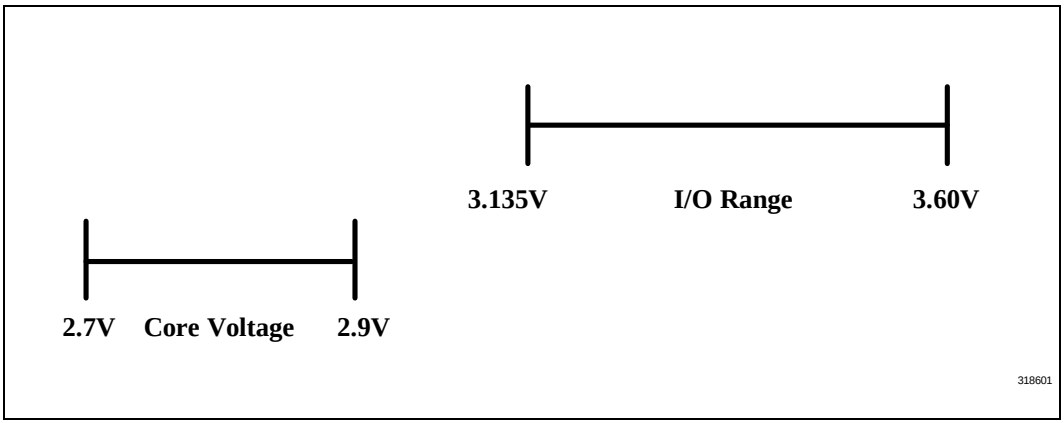

Figure 1. The Core and I/O Voltage Specifications for Pentium® Processors with MMX™ Technology

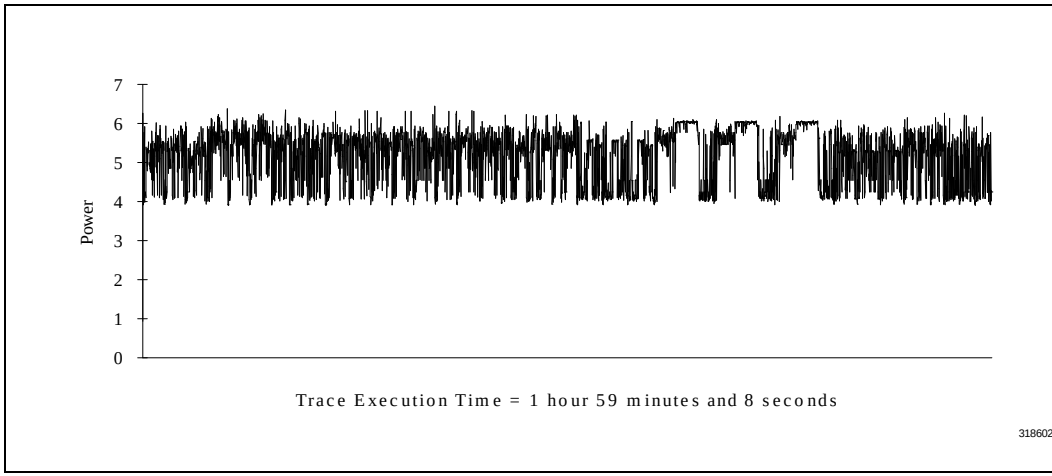

Figure 2. Rapid Fluctuations of System Power While During Active Operation (BAPCo93*)

2.2. Typical Application Behavior

Poorly designed desktop and server systems will violate voltage specifications during normal operation. An unusual application instruction mix can cause large current spikes from clock cycle to clock cycle. Figure 2 shows the rapid fluctuations of system power during execution of a BAPCo93* benchmark trace on the Pentium processor (BAPCo93 is a system benchmark used for measuring system performance). These quick transitions in current occur in a shorter time frame than that in which the power supply unit or voltage regulator may be able to respond.Worst-case transients occur during the transition into or out of a low power state. Figure 3 shows an oscilloscope trace of a system using STPCLK# assertion/deassertion to enter/exit the Stop Grant State. When STPCLK# is deasserted, the supply voltage “droops” due to ESL and ESR effects (see Section 3.6), and because the voltage regulator cannot respond quickly enough to the large, instantaneous change in current. Similarly, when STPCLK# is asserted, the system enters Stop Grant state, and the supply voltage “surges” because of ESL/ESR effects and the large instantaneous changes in current. Droops and surges also occur in systems with proper decoupling, but to a lesser extent. The system also has high-frequency noise due to high operation speed of the internal core.

NOTE

Violating the voltage specifications by undershooting or overshooting the voltage range will result in unreliable and unstable behavior.

The consequences of voltage specification violations are explained in the next section. In Section 3.0, recommended techniques for providing accurate regulation and proper decoupling to ensure a robust platform are reviewed.

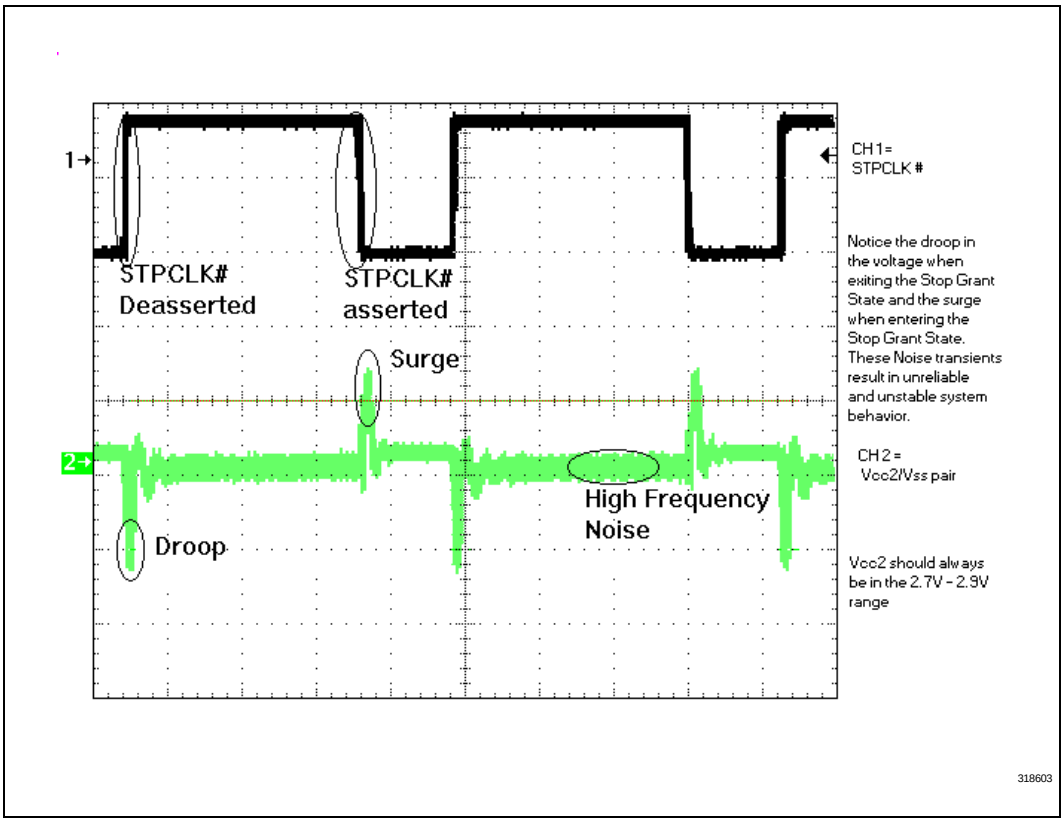

Figure 3. Voltage "Droop" and "Surge" When Toggling STPCLK#

2.3. Voltage Specification Violations

Transient excursions outside of the specified voltage range may result in unstable system behaviour. Excessive and sustained surges can cause hot electron related effects and compromise the reliability of the device. Transients may also cause timing violations, which in turn may lead to a failure in the system.

We have seen instances of a system failure because of excessive V_{CC} transient noise.

Extensive die probing experiments show the frequency components of noise that can be damped on a motherboard by adding decoupling capacitors. Data collected through these experiments showed that only noise components less than 20 MHz were reduced on the die by decoupling capacitors added externally. As a result, the recommended oscilloscope measurement bandwidth has been adjusted to 20 MHz (see Section 4.2 for details).

3.0. THE POWER SUPPLY

Unless using a 2.8V power supply, supplying power to the 2.8V core of the Pentium processor with MMX technology requires a 5V-to-2.8V voltage regulator or a 3.3V-to-2.8V voltage regulator. The power supply pins on the Pentium processor with MMX technology are seperated into V_{CC2} and V_{CC3} pins. These pins must be connected appropriately to the CPU core voltage island and the CPU I/O voltage island on the motherboard. The Pentium processor with MMX technology requires 5.7A at 2.8V (200 MHz) for its core from the supply voltage solution. The 3.3V I/O voltage has to be supplied by the system (either through the 3.3V power supply or through a 3.3V voltage regulator on the motherboard).

Robust local decoupling must be provided to accommodate the transition to and from low-power modes. It is important to select the components for the voltage regulation circuitry to be as accurate as possible. A platform based on an inaccurate power supply unit must be compensated with a more accurate regulator and extra local decoupling. Similarly, a platform based on an inaccurate regulator requires accurate supporting components and additional decoupling capacitors. As shown below, selecting accurate components will allow larger voltage transients.

V_{CC} Specifications =	$\sum$ Voltage Regulator Accuracy
	+ Support Component Accuracy
	+ Thermal Drift and Aging Effects
	+ Measured Voltage Transient

The V_{CC2} specification allows a total voltage budget of 200mV. It is important to understand the voltage budget must include any deviation in the voltage regulator, the inaccuracy of its supporting components, and other non-ideal behavior of real components. When designing a platform, these DC factors must be subtracted from the total V_{CC} budget. The remaining allowance should be targeted when measuring the voltage transient (an example is shown in Section 4.5). It is important to select accurate voltage regulators and precise support components to allow maximum voltage transients.

3.1. Selecting an Accurate Power Supply Unit

The power supply unit must provide a minimum setpoint equal to, or higher than, the minimum input voltage required by the regulator. Off-the-shelf 5V power supply units with a 5% accuracy specification can meet the typical 4.75V requirement of most regulators. Figure 4 shows that a 5V power supply unit with an accuracy of 10% may provide a setpoint as low as 4.5V and fail the minimum input requirement of a voltage regulator. If using a less accurate power supply unit, the minimum setpoint must be raised to meet or exceed the minimum input voltage required by the voltage regulator. If a voltage regulator requires an input voltage higher than 4.75V, consider choosing a more accurate power supply unit to raise the minimum setpoint.

Sufficient decoupling must be provided between the power supply unit and the voltage regulator to minimize any noise. The disturbance on the 5V power supply unit may exceed the specification of TTL logic devices if the decoupling capacitance is insufficient.

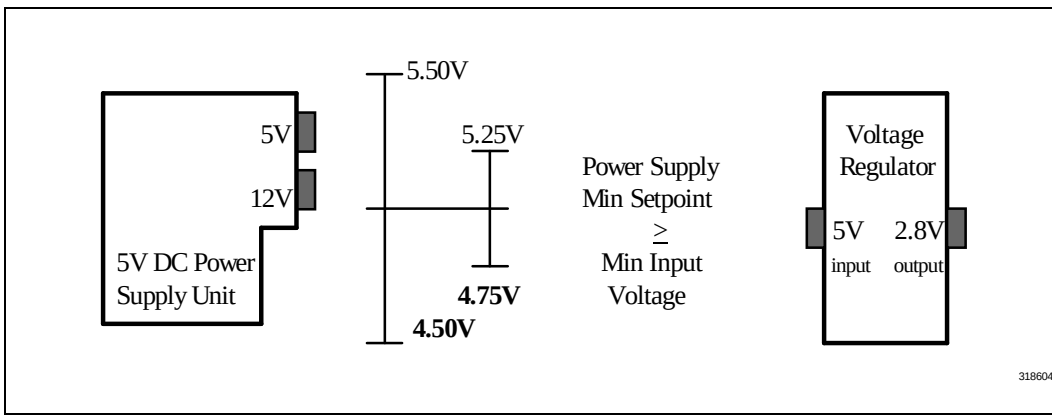

Figure 4. Setpoint Requirement of Power Supply for a 5V-to-2.8V Voltage Regulator

3.2. Selecting an Accurate Voltage Regulator

There are two types of voltage regulators: switching and linear. Switching regulators provide power by pulsing the voltages and currents to the load, thus resulting in lower heat dissipation and higher efficiency. Switching regulators are however generally more expensive and require more supporting components than linear regulators. Linear regulators essentially are voltage dividers and provide power by "dividing down" the 5V/3.3V inputs to 2.8V outputs. Linear regulators dissipate more power, but are less expensive and typically require only two additional (feedback) resistors. Unless the system has strict thermal requirements, linear regulators generally are suited for high-volume designs. Both types of regulators can meet the V_{CC2} voltage range if they have accurate outputs and precise supporting components. Table 2 compares the two types of voltage regulators and shows that linear regulators are cheaper than switching regulators and also require less additional components, but dissipate more power.

An inaccurate regulator leaves little room for transient tolerance. For example, V_{CC2} specifications allow a voltage regulator solution to deviate only ±3.5 percent (2.7V to 2.9V) from the nominal regulator setpoint of 2.8V. Static specifications such as line regulation, temperature drift, and the initial setpoint must be held to 1% if any transient is to be permitted at all. Table 3 shows sample voltage regulator module accuracy for a Pentium processor with MMX technology-based platform.

Table 2. Comparison of Voltage Regulators

Characteristics (Typical)	Linear Regulator		Switching Regulator	
	5V-to-3.3V	5V-to-2.8V	5V-to-3.3V	5V-to-2.8V
Maximum Efficiency	67%	56%	95%	90%
Maximum Power Dissipation	33%	44%	5%	10%
Supporting Components	2 to 6 (feedback resistors)	2 to 6 (feedback resistors)	5 to 12 (feedback resistors, MOSFET switches, inductor, diode, caps)	5 to 12 (feedback resistors, MOSFET switches, inductor, diode, caps)
Approximate Total Cost	Moderate	Moderate	Moderately High	Moderately High

Table 3. Recommendations for Linear Voltage Regulator

Parameters	Total Accuracy	Maximum Deviation
Voltage Regulator Setpoint +	±1 %	±28mV
Feedback Resistors +	±0.2%	±5.6mV
Thermal Drift, Aging Effects =	±0.1% =	±2.8mV =
Total Variation	±1.3 %	±36.4mV

Based on calculations in Section 4.5 for Table 3, the noise transient of the processor should not exceed ±63.6mV (assuming the setpoint is 2.8V). There are direct tradeoffs between the accuracy of the regulator and the amount of local decoupling. Using a less accurate regulator requires more accurate dividing resistors and more decoupling. Conversely, using high-ESR, quick-aging capacitors necessitates accurate regulators. The next section recommends the bulk and high-speed decoupling required to ensure a robust Pentium processor with MMX technology-based platform. The recommendations were based on extensive simulations and empirical measurements.

3.3. Decoupling

The small size of the CPU core voltage island, its isolation from the motherboard power plane, and support of varied voltage requirements make proper decoupling of the island power plane voltage and ground plane essential. Appropriate decoupling capacitors are required on the voltage island near the processor to ensure that the CPU voltage stays within specified limits during normal and transient conditions. There are two types of decoupling that need to be considered: bulk decoupling and high-frequency decoupling.

3.4. Bulk Decoupling

For the processors supported on the flexible motherboard, the power consumption can transition from a low level to a much higher level (or vice versa) very rapidly. This can happen during normal program execution; however, a higher surge of current typically occurs when entering or exiting the Stop Grant State. Another example is when executing a HALT instruction which causes the processor to enter the Auto-HALT Power-down State, or transition from HALT back to the Normal State. (Note that the Auto-HALT Power-down feature is always enabled even when other power management features are not implemented.) All of these examples may cause abrupt changes in the power consumed by the CPU. As the voltage supply (regulator) cannot respond to a sudden load change instantaneously, bulk storage capacitors with low ESR (Effective Series Resistance) are required to maintain the regulated supply voltage during the interval that falls between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

3.5. High-Frequency Decoupling

High-frequency decoupling is required to provide a short, low impedance path to high-frequency components such as high current spikes in order to minimize noise. The processor driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

For high-frequency decoupling, low inductance capacitors and interconnects are recommended for best high-speed electrical performance. Inductance can be reduced by shortening circuit board traces between the CPU and decoupling capacitors as much as possible. Surface mount capacitors are preferable, as capacitors with long leads add inductance to the circuit. The capacitors should be of RF grade, with low ESR and low inductance to reduce spikes.

3.6. Decoupling Recommendations

Table 4 shows the processor decoupling recommendations for the flexible motherboard for both the CPU core and I/O voltage islands. This is based on simulation and testing of the voltage transients from the CPU and the effects of motherboard decoupling.

Spice modeling (modeling worst case current transients including the CPU package inductance, capacitance, routing, decoupling, voltage regulator output inductance, etc.) should be used to estimate the amount of decoupling capacitance required for the CPU voltage island.

It is advised that before committing to any change from the decoupling capacitor recommendation, the new solution be simulated for the variety of variables in components, temperature and lifetime degradation.

Table 4. Decoupling Recommendations for CPU Core and I/O Voltage Islands

	Quantity	Value	ESR	ESL	Type
CPU Core Voltage Island	4	100µF	25 mOhms [1]	0.45 nH [3]	Tantalum
	25	1µF	0.6 mOhms [2]	0.084 nH [4]	X7R dielectric, ceramic
CPU I/O Voltage Island [5]	12	0.1µF			603 Type

NOTES:

1. ESR per capacitor should be less than 100 mOhms.
2. ESR per capacitor should be less than 15 mOhms.
3. ESL per capacitor (including 0.7nH Via inductance per capacitor) should be less than 2.7 nH.
4. ESL per capacitor (including 0.7nH Via inductance per capacitor) should be less than 2.1 nH.
5. This does not include decoupling for components other than the CPU in the 3.3V I/O voltage island.

For bulk decoupling, tantalum capacitors are recommended over electrolytic capacitors. In general, electrolytic capacitors degrade at a much faster rate, are not as accurate, and are not as stable over temperature as tantalum capacitors.

For high-speed decoupling in the CPU core voltage island, low inductance, 1µF capacitors of X7R dielectric are recommended. These capacitors not only decouple the CPU core for high-frequency noise but also control the voltage during very fast transients (less than 100ns.)

3.7. Placement of Decoupling Capacitors

Figure 5 shows an example of how the recommended CPU decoupling capacitors shown in Table 4 would be placed on the respective voltage islands on the flexible motherboard. The bulk capacitors should be placed near the CPU inside the voltage island to ensure that the supply voltage stays within specified limits during changes in the supply current during operation. The 1µF, X7R capacitors should be evenly distributed inside the CPU core voltage island inside and around the CPU footprint.

Figure 5 also shows the 12 0.1µF capacitors evenly placed around the CPU, close to the CPU V_{CC3} pins inside the CPU I/O voltage island.

In this example, all the capacitors were placed on one side of the board. If components are assembled on both sides of the board, then these capacitors can be distributed between the top and bottom sides. If done this way, vias connecting the capacitor pads to the power and ground layer can be shared between the capacitors on the top and bottom sides. This can help reduce the total overall capacitor inductance. The traces connecting the vias to the capacitor pads should be kept as short as possible. In cases where it is difficult to reduce the length of the circuit board trace, the trace should be made wider so as to reduce the trace inductance.

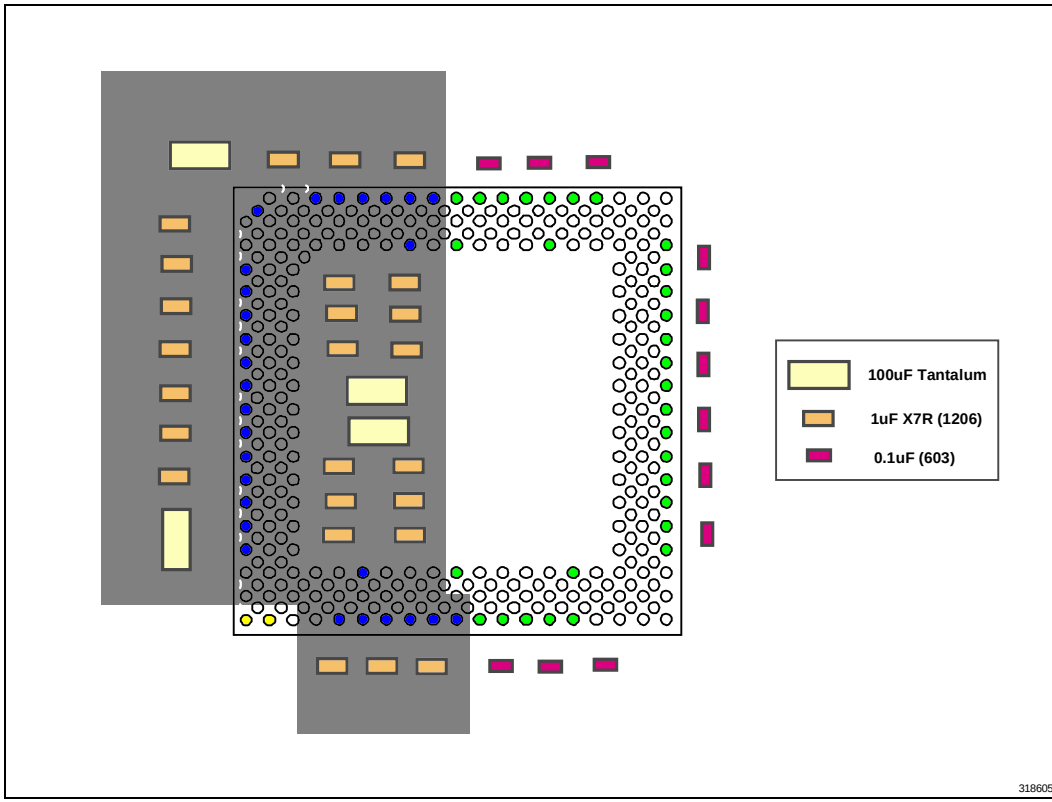

Figure 5. Example of CPU Decoupling Capacitor Placement

3.8. ESR and ESL: Why Less is Better?

Effective Series Resistance (ESR) and Effective Series Inductance (ESL) are elements of non-ideal behavior of real components. The ESR and ESL determine how quickly a capacitor can source current to regulate a new load. More importantly, the ESR must be low enough at high frequencies to not offset the desired filtering effects of bulk decoupling capacitors. For a given current transient, the voltage transient is proportional to the ESL and ESR. The use of capacitors with high ESR and ESL hence contributes to higher voltage transients and may cause overshooting or undershooting. Aluminum electrolytic capacitors degrade at a relatively low frequency. Low ESR tantalum caps can retain ESR specifications up to about 1-10 MHz. Low ESR ceramic capacitors can retain ESR specifications up to 100 MHz.

Do not reduce the quantity of capacitors shown in Table 4 if substituting with capacitors with a larger value. When placed in parallel, two 220µF tantalum capacitors may have higher ESR than four 100 µF capacitors. Placing capacitors in parallel reduces the maximum overall ESR. Therefore, many caps in parallel may be required to ensure a low enough overall ESR.

Table 5. Summary for Creating Worst-Case Transient

Step One	A	Install 200 MHz Pentium® processor with MMX™ technology
Step Two	B	Set up the measurement system as described in Figure 9.
Step Three	C	Set oscilloscope as shown in Table 6 to obtain the voltage transient
Step Four	D	Assert and deassert STPCLK#
Step Five	E	Measure V_{CC} as shown in Table 7 to obtain the voltage transient. The voltage transient must not overshoot 2.9V, or dip lower than 2.7V for V_{CC2} planes.
Step Six	F	Assert and deassert STPCLK# while the "hi_pwr2.exe" program is executing. Measure V_{CC} transients as in Step Five.

4.0. TAKING VOLTAGE MEASUREMENTS

4.1. Creating Worst-Case Transient Excursion

The recommendations for regulators and local decoupling can be validated by creating worst-case supply transient conditions and measuring accurately. Worst-case transients may be generated by toggling the STPCLK# and executing the "hi_pwr2.exe" program on a Pentium processor with MMX technology (refer to Appendix A for an explanation of the "hi_pwr2.exe" program). Table 5 contains a summary of the procedure explaining the steps for creating the worst-case transient conditions:

4.2. Measurement Technique

All transient measurements must be taken at the back of the motherboard at the CPU pins. Measuring transients at a different location will result in inaccurate readings. For accurate readings, all probe connections must be clean. Shorten the ground lead of the probe to minimize any extra inductance. Figure 6A proposes a solution by providing a short loop of wire around the ground shield of the probe.

NOTE

Figure 6B is an example of how not to perform measurements; the ground cable of the probe will add significant noise to the transient measurements.

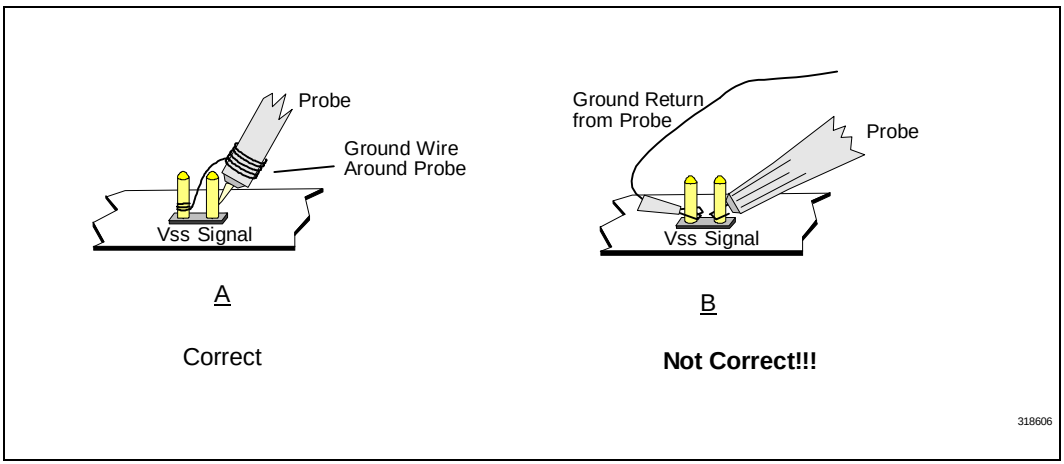

Figure 6. Correct and Incorrect Probe Connections for Measuring V_{CC} Transients

Table 6. Recommended Oscilloscope Settings to Capture Voltage Transients

Bandwidth	20 MHz
Sampling Rate	≥ 100 Million Samples / Second
Vertical Reading	≤ 20 mV/division
Horizontal Reading	≥ 500 nS/division
Display	Infinite Persistence / Envelope Mode

The Pentium processor specifications outline a set of 12 pins for voltage measurements. The V_{CC2}/V_{SS} pairs to be measured are A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2, AN13/AM10. The V_{CC3}/V_{SS} pins that should be measured according to the specifications are AN21/AM18, AN29/AM26, AC37/Z36, U37/R36, L37/H36, A25/B28. These pins are a subset of all V_{CC}/V_{SS} pairs, and hence should not be singled out when placing decoupling capacitors.

The scope settings shown in Table 6 are recommended for accurate measurements. Extensive die probing experiments were performed on Pentium processors with MMX technology. These experiments concluded that any noise components less than 20 MHz could be reduced on die by decoupling capacitors added externally. Therefore, the measurement bandwidth of the scope should be set at 20 MHz, although a probe with a bandwidth of at least 250 MHz should be used. This high bandwidth probe ensures a total effective bandwidth of 20 MHz. The trigger point should be set in the middle of the range and slowly moved to both the high and low ends of the voltage specification range. A Vertical reading of 20mV/division ensures an accurate reading and display of the transient waveform. The display should be set either on infinite persistence or envelope mode. The advantage of using infinite persistense as compared to envelope mode for this measurement is that random noise points can be ignored in infinite persistence readings. Envelope mode makes the display crispier and the cursor can be positioned more accurately.

4.3. STPCLK# Toggling

It is necessary to assert and deassert the STPCLK# signal while executing the “hi_pwr2.exe” program to create the worst-case transient conditions. Asserting the STPCLK# signal will place the processor into the Stop Grant state (consuming about 15% of active current). Deasserting the STPCLK# signal will return the processor to the Normal state. To simulate actual system behavior, V_{CC} should be stabilized before asserting or deasserting STPCLK# as shown in Figure 7. Asserting and deasserting STPCLK# too rapidly may generate unrealistic voltage transients. There are no minimum time specifications required to stabilize V_{CC} since the estimated time is highly dependent on the system (length of current instruction, outstanding write cycles, response time of voltage regulator, and accuracy and quantity of decoupling). In general, STPCLK# should be asserted and deasserted at a rate of 200 Hz to 100 KHz.

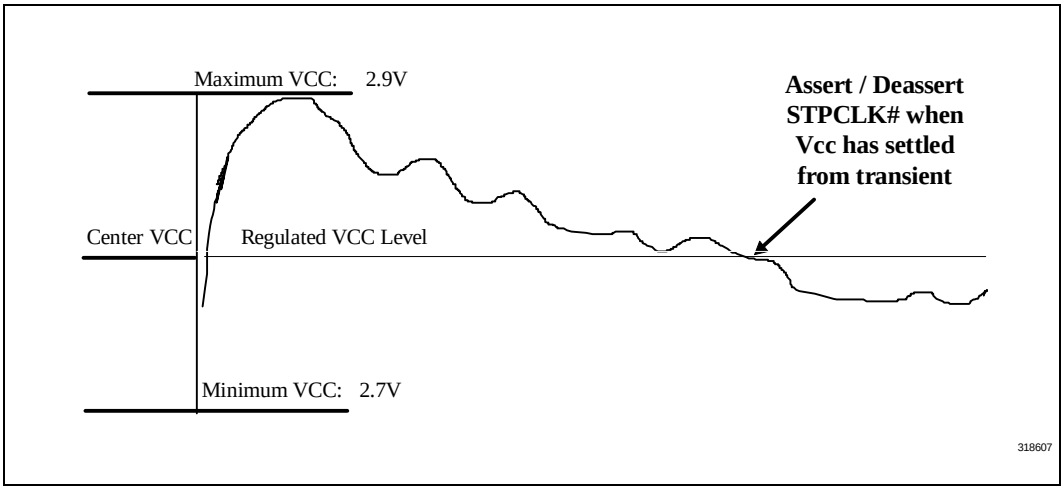

Figure 7. Toggle STPCLK# When V_{CC} Transient Has Settled

STPCLK# toggling is most easily accomplished using a standard function generator. Emperical measurements show that frequency variations from 200 Hz to 100 KHz do not impact V_{CC} measurements. For ease of measurement, toggling the STPCLK# between those frequencies is recommended. For toggling the STPCLK# with a standard frequency generator, a square wave should be generated with 3.3V peak, and a duty cycle in the 25%-75% range.

If a function generator is not available, alternative means may be used for toggling the STPCLK#. Figure 8 illustrates a simple 555 Timer circuit which can be used to produce a square wave with its duty cycle determined by R2 and R1 and the frequency controlled by the capacitor C.

- **Duty Cycle = (R1 + R2) / (R1 + 2R2) * 100**
- **Frequency = 1.44 / (R1 + 2*R2) /(R2*C)**

Emperical results have shown that the 555 timer is adequate at toggling the STPCLK#. Experiments done using the 555 timer circuitry have been successful in making accurate Voltage Transient Measurements.

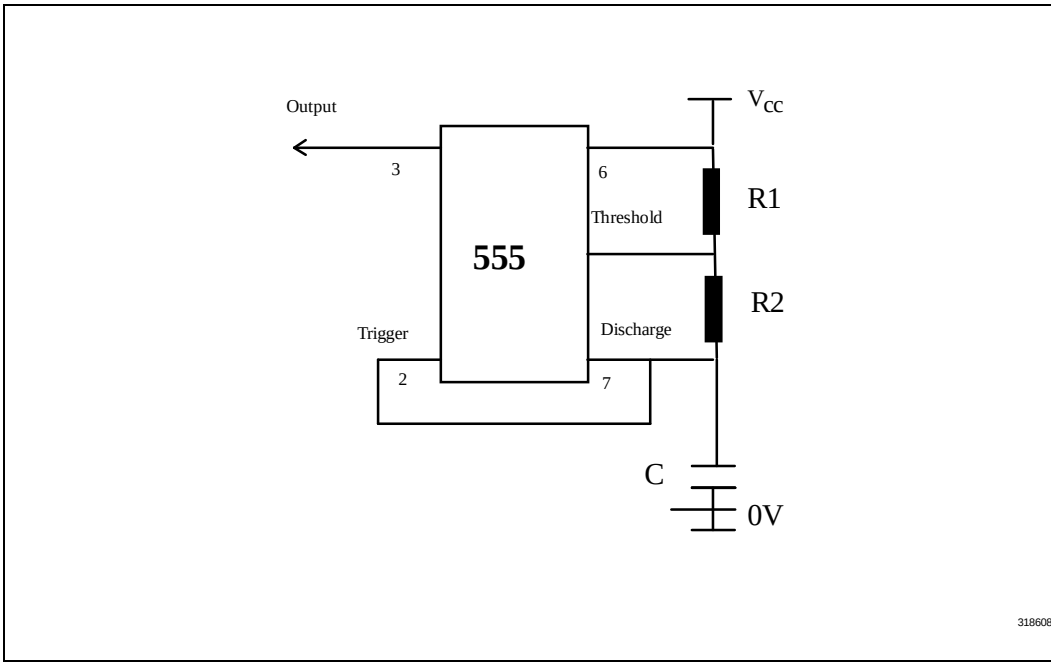

Figure 8. 555 Timer Implementation for Toggling the STPCLK#

4.4. Step by Step Measurement Procedure

The basic setup for measurements is shown in Figure 9. Connect a probe to Channel 1 of the oscilloscope for measuring at the CPU pins located at the back of the board. V_{CC} measurements for all transient analysis must be done at the back of the board and at the 12 pins noted in Section 4.2. The STPCLK# pin at the back of the board is soldered to a wire for ease of toggling the STPCLK#.

Connect the Signal generator output to the soldered STPCLK# pin on the board using a 50 Ohm coaxial cable. The frequency generator should output a 3.3 V peak signal with a 25-75% duty cycle. Connect another oscilloscope probe to the soldered STPCLK# pin wire (for trigger). Make sure not to ground this oscilloscope probe to the board ground, because this may cause excess noise. Instead, the probe ground can be wrapped around the probe ground shield such as shown in Figure 6.

Table 7. Measurement Technique Summary

Measurement Bandwidth[1]	20 MHz
Probe Bandwidth	$\geq$ 250 MHz
Board Location	At the back of the board, at Socket pins
Pin Locations	6 Pins for V_{CC2} measurements (listed below) A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2, AN13/AM10

NOTES:

1. Signals should be attenuated by no more than 3dB at 20 MHz, and 6dB at 40 MHz.

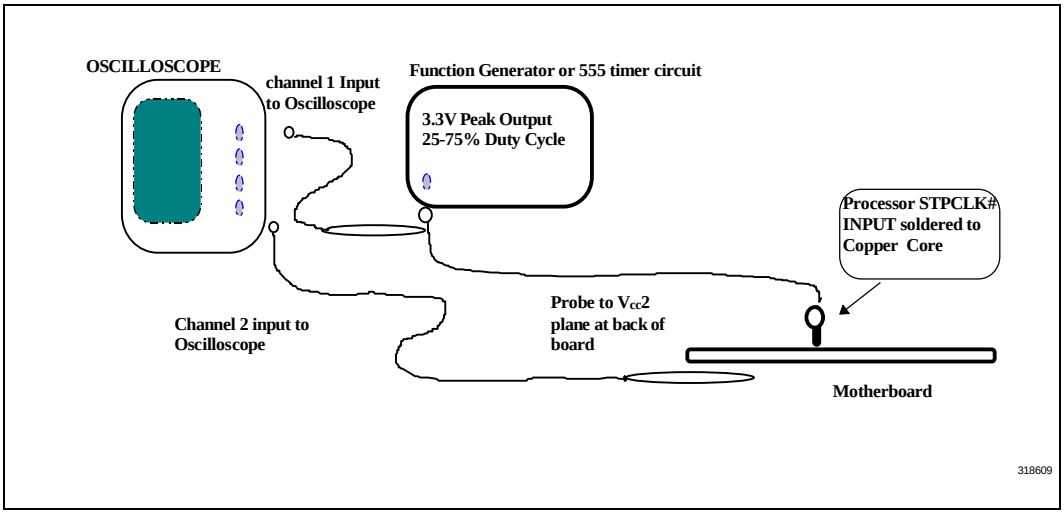

Figure 9. Setup for Measuring V_{CC} Transients at the Back of the Board

Then follow these basic instructions:

1. Calibrate the scope to set it to the desired settings as shown in Table 6.
2. Make sure the board powers up correctly. Measure the setpoint for V_{CC} to ensure it is near 2.8V (2.7V to 2.9V). Use the oscillloscope or digital multi-meter for measurement.
3. If the board powers up and the setpoint is unsatisfactory then recheck the setup for accuracy. If the setpoint is still not within the voltage specifications, check with the Flexible motherboard guidelines for design guidelines. If the setpoint is satisfactory, test the 200 MHz PP/MT in the following three settings:
   A. At the MS-DOS prompt: measure the min/max voltage (for set point).
   B. At the MS-DOS prompt and with STPCLK# toggling: measure the min/max voltage (for 2.8V V_{CC} plane margining).
   C. With the stress code (Hi_pwr2.exe) running and the STPCLK# toggling: measure the min/max voltage (for corner cases of V_{CC} spikes and drops).

Measure V_{CC} transients at the six V_{CC2}/V_{SS} measurement pairs as discussed in Section 4.2. Tables for documenting these measurements are provided in Appendix C. The next section evaluates each of the measurement settings in significantly more detail. For each of the measurements, document the following for the Data Table in Appendix C.

- Total Δ
- Average V_{CC}
- Absolute Minimum V_{CCc}
- Absolute Maximum V_{CC}

4.4.1. PROCEDURE A

At the MS-DOS prompt without the pulse generator connected to the STPCLK# pin, make sure the scope is set to the settings in Table 7 and is triggered at the STPCLK# edge. Measure the difference from the top of the V_{CC}/V_{SS} signal to the bottom as shown in the sample oscilloscope plot in Figure 10. The pupose of this measurement is to get the Min/Max voltage for setpoint. Fill in the table in Appendix C.

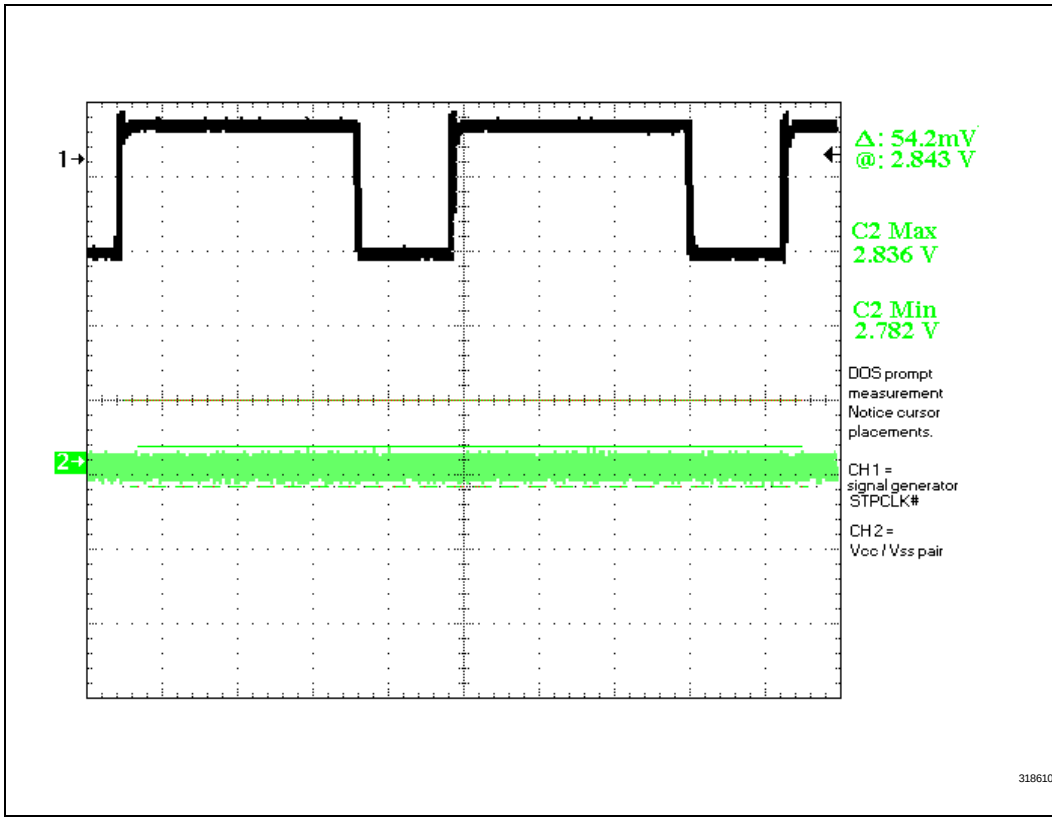

Figure 10. Measuring Min/Max Voltage for Setpoint at MS-DOS* Prompt

4.4.2. PROCEDURE B

At the MS-DOS prompt with the pulse generator "on" and connected to STPCLK# for V_{CC2} plane margining, make sure the scope is set to the setting in Table 7 and is triggered at each edge from the frequency generator. Measure the difference from the top of the surge to the bottom of the droop as shown in the sample oscilloscope plot in Figure 11. Document the following in the data table in Appendix C.

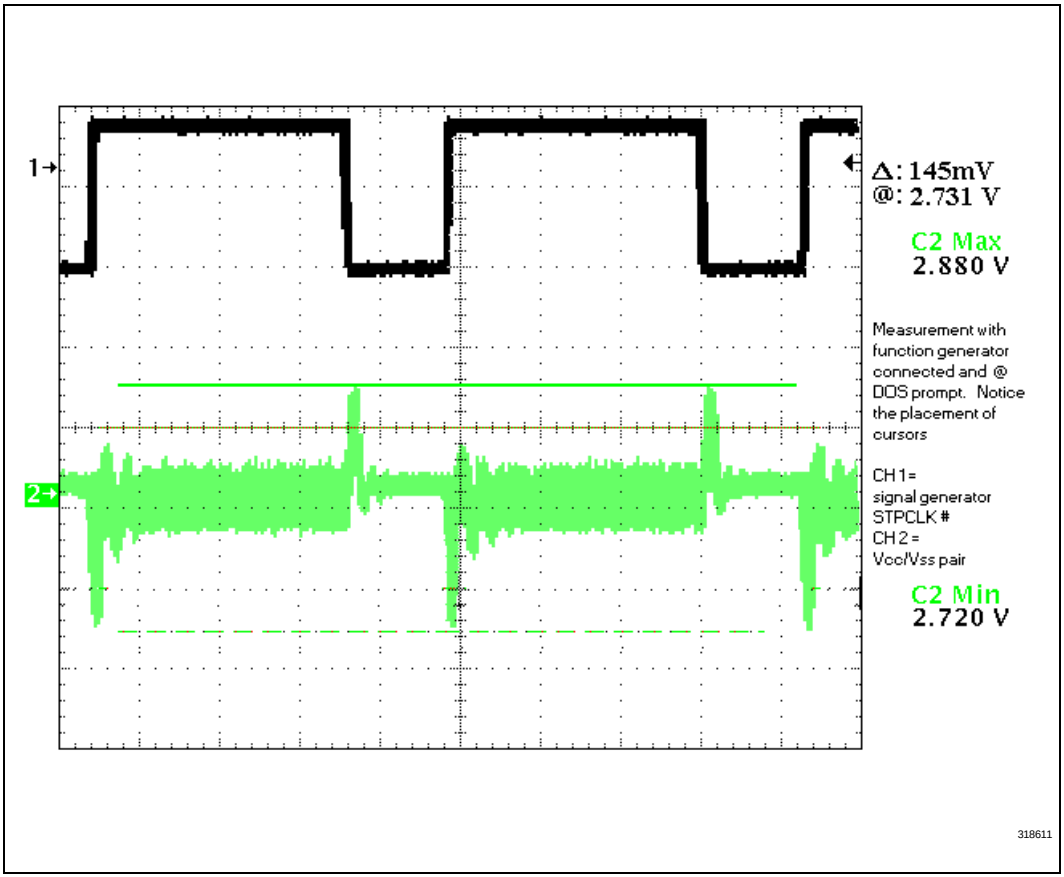

Figure 11. Measuring Min/Max Voltage for Setpoint at MS-DOS* Prompt with STPCLK# Toggling

4.4.3. PROCEDURE C

With the pulse generator connected to STPCLK# and the stress test running (hi_pwr2), make sure the scope is set to the settings in Table 7 and is triggered at STPCLK# edge from the frequency generator. Measure the difference from the top of the surge to the bottom of the droop as shown in the sample oscilloscope plot in Figure 12. This setting should give the worst case measurement. Complete the data table in Appendix C.

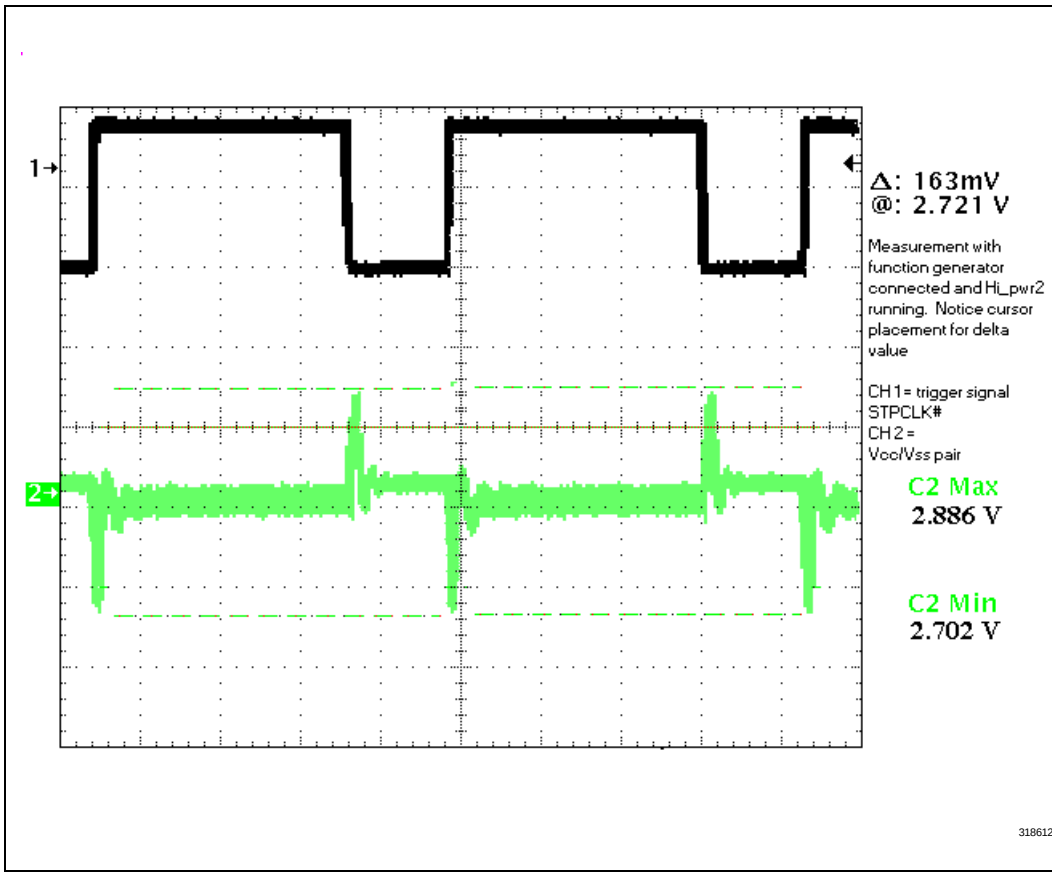

Figure 12. Measuring Worst V_{CC} Transients with STPCLK# Toggling and Stress Code Running

4.5. Evaluation of Measurement Results

The Pentium Processor with MMX technology V_{CC2} specification allows a total budget of 200mV, ranging from 2.7V to 2.9V. However, it is important to realize that this voltage specification includes any deviation in the voltage regulator and its circuitry, as well as aging effects of these components as described in Section 3.0. There is a probability that these components may display less than accurate behavior. Therefore, a measurement delta of 200mV is not considered passing (The setpoint may change, as well as the supporting components may display less than accurate behavior). For example, consider the numbers for a linear voltage regulator shown in Table 3. The voltage regulator setpoint, feedback resistor accuracy, and the thermal drift and aging effects combine together to use up ±36.4mV (±28mV ±5.6mV±2.8mV) of the ±100mV range. This leaves a margin of only ±63.6V ([200mV — (±36.4 * 2)] / 2) for Vcc transients. Therefore, a measured delta of 137.2mV for V_{CC} transients would surely constitute a stable system for the scenario in Table 3.

APPENDIX A

A1.0. "Hi_pwr2" CODE

The hi_pwr2.exe code is used for V_{CC} transient analysis and to validate the processors thermal design for the Pentium processor with MMX technology. To get maximum current draw in the system, after the initial setup, the code runs a loop of instructions.

An average Pentium processor with MMX technology in a typical system may dissipate slightly less power than the specification while executing this code. This is because Intel has allowed for process variations between wafers of CPUs, system variations, and test instrumentation guardbands. Since we can not be sure what power this code will draw in a particular customer system, the actual power drawn by the processor in the particular system should be measured.

The file hi_pwr2.exe contains a short loop of Intel Architecture intensive code. This code uses the most power of any stable, MS-DOS executable program that Intel has tested on Pentium processors with MMX technology.

This code has been optimized for use only with Pentium processors with MMX technology. Any power testing on a Pentium processor without MMX technology should be done with hi_pwr.exe (STR4Y) code.

To use this code for V_{CC} transient analysis:

1. Execute the code
2. While the code is executing, toggle the STPCLK# signal (i.e. externally since the code itself will not toggle STPCLK#)
3. Measure the noise transients according to the methodology found in this Application Note

To use the code to validate a Pentium processor with MMX technology thermal design:

1. Execute the code and measure the power dissipation.
2. If the processor power dissipation falls short of the maximum Thermal Design Power specification, the V_{CC} level may be increased (within its specified range) to attempt to reach the maximum value.
3. If the power dissipation still does not reach the specified maximum value, a thermal linear projection to the guaranteed worst case of the Thermal Design Power should be performed.

Since this program runs in an infinite loop and disables all interrupts, a hard reboot of the system is necessary to exit out of the code.

APPENDIX B

B1.0. THIRD PARTY COMPONENTS

The following vendors offer various solutions to ensure a robust Pentium processor with MMX technology-based platform. Please contact the following vendors for specifications, samples, and design support.

2.8V/3.3V/VRE Linear Regulator Solutions

Vendor	Part Number	Electrical				Remote Sense	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Power (Max) (W)			Sample	Product
Cherry	CS5206	5	2.8	6	17	No	TO-220/ D^2Pak	Now	Now
		5	3.3/ VRE	6	20				
	CS5207A	5	2.8	7	20	Yes	TO-220	Q4'96	Q4'96
		5	3.3/ VRE	7	23				
Linear Tech	LT1575 (+ ext FET)	3.3	2.8	10	5	Yes	8-pin SOIC	Now	Now
		5	2.8	10	22				
		5	3.3/VRE	10	27				
	LT1577 (Dual)	5	2.8	10	22	Yes	16-pin SOIC	Now	Now
		5	3.3/VRE	10	27				
	LT1580	5	2.8	7	15.4	Yes	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	LT1584	5	2.8	7	15.4	No	TO-220/TO-263	Now	Now
		5	3.3/VRE	7	11.9				
	LT1585A	5	3.3	5	8.5	No	TO-220/TO-263	Now	Now
Linfinity	LX8384	5	3.3/VRE	5	8.5	No	TO-220/TO-263	Now	Now
	LX8585	5	3.3/VRE	4.6	7.82	No	TO-220/TO-263	Now	Now
	LX8586	5	2.8	6	13.2	No	TO-220/TO-247	Now	Now
		5	3.3/VRE	6	10.2				

2.8V/3.3V/VRE Linear Regulator Solutions (Contd.)

Vendor	Part Number	Electrical				Remote Sense	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Power (Max) (W)			Sample	Product
National	LM2951	5	2.8	7	15.4	No	SO-8	Now	Now
		5	3.3/VRE	7	11.9				
	LM3411	5	3.3/VRE	7	11.9	No	SO-8/ 5-pin SOT 23	Now	Now
Raytheon	RC5102 (Dual)	5	2.8	7	15.4	Yes	8-pin SOIC	Now	Now
		5	3.3/VRE	7	11.9				
Semtech	EZ1083/A	5	2.8	7.5	16.5	No	TO-220 or	Now	Now
		5	3.3/VRE	7.5	12.75		TO-247		
	EZ1082	5	2.8	10	22.0	No	TO-220 or	Now	Now
		5	3.3/VRE	10	17		TO-247		
	EZ1584A	5	2.8	7	15.4	No	TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1900	5	2.8	7	15.4	No	8-pin SOIC	Now	Now
	(Dual)	5	3.3/VRE	7	11.9				
	EZ1580	5	2.8	7	15.4	Yes	5-pin TO-220	Now	Now
		5	3.3/VRE	7	11.9				
	EZ1585D	5	2.8	6	13.2	No	TO-220	Now	Now
		5	3.3/VRE	6	10.2				
Unisem	US1080	5	2.8	8	17.6	No	TO-220/TO-263	Q1'97	Q1'97
		5	3.3/VRE	8	13.6				

2.8V/3.3V/VRE Switching Regulator Solutions

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
Cherry	CS5120	5	2.8	5.7	85%	1	14-pin PDIP	Now	Now
		5	3.3/VRE	5.7	85%	1	14-pin SOIC		
Harris	HIP5010	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5011	5	2.8	11	91%	2	16-pin SOIC or	Now	Now
		5	3.3/VRE	11	95%		7-pin TO-220 or 7-pin D^2Pak		
	HIP5010	5	2.8	6	89%	2	7-pin TO-220	Now	Now
		5	3.3/VRE	6	92%		or 7-pin D^2Pak		
	HIP5016	5	2.8	6	89%	2	7-pin TO-220 or	Now	Now
		5	3.3/VRE	6	92%		7-pin D^2Pak		
Linear Tech	LTC1266	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				
	LTC1430	5	2.8	15	93%	2	16-pin SOIC or	Now	Now
		5	3.3	15	95%		8-pin SOIC		
	LTC1435	5	2.8	10	93%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	95%				

2.8V/3.3V/VRE Switching Regulator Solutions (Contd.)

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
Linfinity	LX1660/1	5	2.8	12	85%	2	SO-16	Q4'96	Q4'96
		5	3.3/VRE	12	85%				
Maxim	MAX797	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				
	MAX798	5	2.8	10	88%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	10	88%				
National	LM3578 & LM3411	5	3.3/VRE	10	88%	1	SO-8 or 5-pin SOT23	Now	Now
Raytheon	RC5036 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5031	5	2.8	10	87%	1	14-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
	RC5035 (Dual)	5	2.8	10	87%	2	16-pin SOIC	Now	Now
		5	3.3/VRE	5	89%				
Siliconix	Si9140	5	2.8	6	90%	2	16-pin SOIC	Now	Now
		5	3.3	6	90.5%				
	Si9145	5	2.8	6	82%	1	16-pin SOIC or	Now	Now
		5	3.3/VRE	6	83%		16-pin TSSOP		

2.8V/3.3V/VRE Switching Regulator Solutions (Contd.)

Vendor	Part Number	Electrical				Number of MOSFETs	Package	Availability	
		V_{IN} (V)	V_{OUT} (V)	I_{OUT} (Max) (A)	Solution Efficency (typical)			Sample	Product
Unitrode	UC3886	5	2.8	10	85%	1	16-pin SOIC	Now	Now
		5	3.3/VRE	10	85%		or 16-pin DIP		
	UCC3881	5	2.8	10	85%	1	16-pin SOIC	Now	Q1‘97
		5	3.3/VRE	10	85%		or 16-pin DIP		
	UCC3880	5	2.8	10	85%	1	20-pin SOIC	Now	Now
		5	3.3/VRE	10	85%		or 20-pin DIP		
	UC3874	5	2.8	10	90%	2	18-pin SOIC	Now	Now
		5	3.3/VRE	10	90%		or 18-pin DIP		
Unisem	US2050	5	2.8	10	85%	1	7-pin TO-220	Q1’97	Q1’97
		5	3.3/VRE	10	85%		or TO-263		

Regulator Vendor Solutions Contact List

On-board Regulators

Vendor	North America	Europe	Asia	Japan
Cherry	Dennis Gatano Tel: (401) 886-3305 Fax: (401) 885-5786			
Harris	Dean Henderson Tel: (919) 405-3603 Fax: (919) 405-3651	Robert Lahaye Tel: (33) 1 346 54046 Fax: (33) 1 394-64054	Jason Lin Tel: (886) 2 716 9310 Fax: (886) 2 715 3029	Masaru Agano Tel: (81) 3 3265 7571 Fax: (81) 3 3265 7575
Linear Tech	Bob Scott Tel: (408) 432-1900 Fax: (408) 434-0507	Fred Killinger Tel: (49) 89-9642550 Fax: (49) 89-963147	Dave Quarrels Tel: (65) 753 2692 Fax: (65) 754 4112	
Linfinity	Andrew Stewart Tel: (714) 898-8121 Fax: (714) 893-2570			
Maxim	David Timm Tel: (408) 737-7600 Fax: (408) 737-7194	David Watson Tel: (44) 17 3430 3388 Fax: (44) 17 3430 5511	Steve Huang Tel: (886) 2558 6801 Fax: (886) 2555 6348	Tadi Kodairo Tel: (81) 3 3232 6141 Fax: (81) 3 3232 6149
National	Venkatesh Shan Tel: (408) 721-3753 Fax: (408) 721-8763	Werner Obermaier Tel: (49) 81 4135 1331 Fax: (49) 81 4135 1220	Vincent Lin Tel: (852) 2737 1616 Fax: (852) 2736 9931	Mark Kachmerak Tel: (81) 43 299 2373
Raytheon	David McIntyre Tel: (415) 966-7734 Fax: (415) 966-7742	David Frye Tel: (44) 17 0566 5555 Fax: (44) 17 0566 3355	Mike Wisnia Tel: (81) 3 3406 5998 Fax: (81) 3 3406 5998	
Semtech	Gene Krzwinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Siliconix	Erik Ogren Tel: 408-970-5543 Fax: 408-567-8910	Sean Montgomery Tel: (44) 344 485757 Fax: (44) 344 427371	Serge Jaunay Tel: (852) 2378 9715 Fax: (852) 2375 5733	Tony Grizelj Tel: (81) 3 5562 3321 Fax: (81) 3 5562 3316
Unitrode	John O'Connor Tel: (603) 429-8504 Fax: (603) 429-8963	David Wells Tel: (44) 181 318 1431 Fax: (44) 181 318 2549	Wilkie Wong Tel: 8522-722-1101 Fax: 8522-369-7596	
Unisem	Reza Amirani Tel: (714) 453-1008 Fax: (714) 453-8748			

Voltage Regulator Modules

Vendor	North America	Europe	Asia	Japan
Ambit	Leonard Kao Tel: (886) 35-7849575 Fax: (886) 35-782924			
Amp	Larry Freeland Tel: (717) 780-6045 Fax: (717) 780-7027	Rob Rix Tel: (44) 1753-67-6800 Fax: (44) 1753-67-6801	Hirotada Ito Tel: (81) 44-844-8077 Fax: (81) 44-812-3203	
C-MAC	Dave Holmes Tel: (407) 881-2321 Fax: (407) 881-2342			
Corsair	John Beckley Tel: (408) 559-1777 Fax: (408) 559-4294			
Semtech	Gene Krzywinski Tel: (805) 498-2111 Fax: (805) 498-3804	Julian Foster Tel: (44) 592-773520 Fax: (44) 592-774781	Kenny Pai Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Raytheon	David McIntyre Tel: (415) 966-7734 Fax: (415) 966-7742	David Frye Tel: 44 17 0566 5555 Fax: 44 17 0566 3355	Mike Wisnia Tel: 81 3 3406 5998 Fax: 81 3 3406 5998	
VXI	Joseph Chang Tel: (503) 652-7300 Fax: (503) 786-5011			

Decoupling Capacitors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1µF, X7S	Dennis Lienemann Tel: (803) 946-0616	Steve Chan (Singapore) Tel: (65) 258-2833 Fax: (65) 258-8221
	TPSD107K010R0100	100µF, Tantalum	Fax: (803) 946-6678	K.J. Kim (Korea) Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
Johanson Dielectrics	160R18W105K4	1µF, X7R	Dave Lopez Tel: (818) 364-9800 Fax: (818) 364-6100 NCTR (California only) Tel: (510) 624-8900 Fax: (510) 624-8905	Bill Yu (Taiwan) Nanco Electronics Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Sales Dept (Hong Kong) Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100µF, Tantalum	Richey-Cypress Elect. Tel: (408) 654-9100 Fax: (408) 566-0160	Warren Marshall Tel: (800) 421-7258 Fax: (714) 713-0129
Murata Electronics	GRM40X7R105J016	1µF, X7R	Sales Department Tel: (770) 436-1300 Fax: (770) 436-3030	Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721 Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (847) 803-6100 Fax: (847) 803-6296	Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090 Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108

APPENDIX C

C1.0. TEST RESULTS

These tables are provided for you to record your test results.

At MS-DOS* Prompt

CPU Points V_{CC}/V_{SS} pairs	Average V_{CC} (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B20				
A7/B10				
G1/K2				
S1/V2				
AC1/Z2				
AN13/AM10				

In MS-DOS* Mode with STPCLK# Toggling

CPU Points V_{CC}/V_{SS} pairs	Average V_{CC} (Volts)	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B20				
A7/B10				
G1/K2				
S1/V2				
AC1/Z2				
AN13/AM10				

Running Stress Code(hi_pwr2) with STPCLK# Toggling

CPU Points V_{CC}/V_{SS} pairs	Average CC	Minimum Droop (V)	Maximum Surge (V)	Δ Total (mV)
A17/B20				
A7/B10				
G1/K2				
S1/V2				
AC1/Z2				
AN13/AM10