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AP-577

APPLICATION NOTE

An Introduction to Plastic Pin Grid Array (PPGA) Packaging

March 1997

Order Number: 243103-003

CONTENTS

1.0. INTRODUCTION

As Intel microprocessors become faster, more complex and more powerful, the demand on high-performance packaging technology increases. For instance, higher clock rates imply faster internal signals, which may cause more switching noise. Thus packaging technology needs to tackle power supply decoupling issues. For each new generation of microprocessors, a greater number of transistors are packed onto each chip, generating more heat. The package thermal resistance becomes critical. Furthermore the shrinking die size causes higher power density, which tests the effectiveness of the package to dissipate the heat. The improvements in microprocessor speed and functionality drive the package design improvements in electrical, thermal and mechanical performance.

Over the years, Intel has introduced a variety of innovative package designs, such as surface mount, small out-line, very thin package, and multilayer molded plastic quad flatpacks (PQFP). Keeping form, fit and function in mind, Intel continues to research and develop advanced packaging technology. The Pentium® microprocessor family has been available in either ceramic pin grid array (CPGA) package or tape carrier package (TCP) format to date. However as the core frequency of microprocessors steps up. Power dissipation will be increasing accordingly.

In 1993, Intel engineers began the development of plastic pin grid array (PPGA) packages to alleviate potential performance-limiting package problems. Compared to the existing CPGA package technology, the PPGA package has a better power distribution and improved thermal and electrical performance. Intel also ensures that the processors in PPGA and CPGA packages meet the same product specifications in Input/Output (I/O) timings, mechanical fit and quality and reliability.

Table 1 summarizes the key differences between the PPGA package and the CPGA package. The following sections will detail the physical structure, electrical modeling and performance of PPGA.

Table 1. Differences Between CPGA and PPGA Packages

Attribute	CPGA	PPGA
Physical		
Appearance	Tile, flat ceramic top	Circuit board, exposed pins
Package Body Material	Ceramic body, Al bond wires	BT laminate, Ni/Cu slug, encap, Au bondwires
Body Thickness	2.8 mm	3.0 mm (with heat slug)
Weight	29 gms	18 gms
Package Trace Metal	Tungsten	Copper
External Heat Slug	No	Yes
External Capacitors	No	Yes
Performance		
Thermal (θ_{jc}) with Heat Sink	1.25° C/W	0.50° C/W
Power Distribution	Good	Better
Package Trace Propagation Delay	Good	Better
Others		
Thermal Grease Used for Heat Sink Attachment	Electrically conductive or non-conductive	Electrically non-conductive
Thermal grease tranfer foil if used	flat, curved or cupped	flat only
Foil size if used	determined by the system manufacturers	equal or smaller than the heatslug
Board Mount	Socket or thru-hole insertion	Socket only
Shipping Tray	Blue color ,see Figure 6	Brown color, pocket size reduced
***Caution*:** For PPGA packages, electrically conductive surfaces should not touch any part of the processor except the heatslug. For instance, an electrically conductive heat sink should not contact the exposed pins, the external capacitors or the exposed metal on the sides of the package.		

2.0. PPGA OVERVIEW

2.1. PPGA Package Physical Dimensions

Figure 1 is the top view of a PPGA package. Note the nickel plated copper heatslug and the eight discrete capacitors. The weight of the package is around 18 grams, as compared to an average of 29 grams for a CPGA package.

Figure 2 and Table 2 show the dimensions of a 296-pin staggered PPGA package with a heatslug. Compared to the existing CPGA package, the PPGA height is increased by 0.2 mm (0.009 inches).

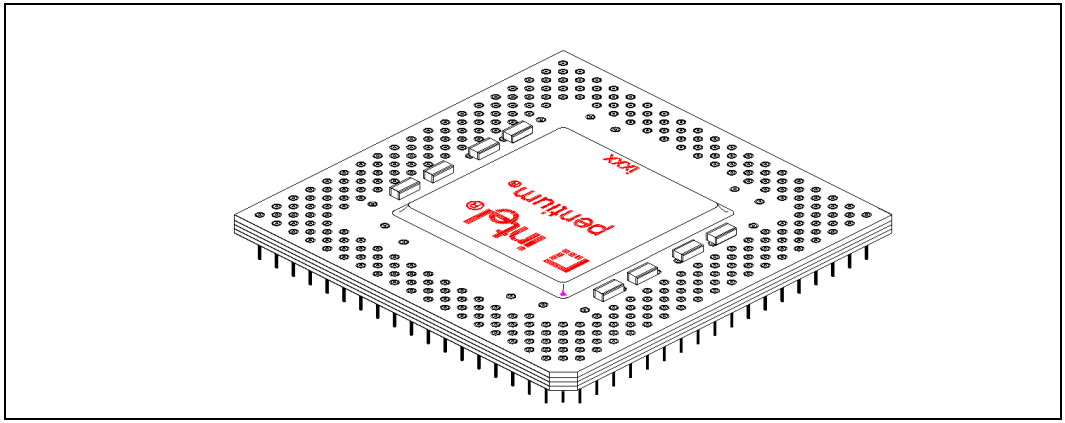


Figure 1. Top View of a PPGA Package

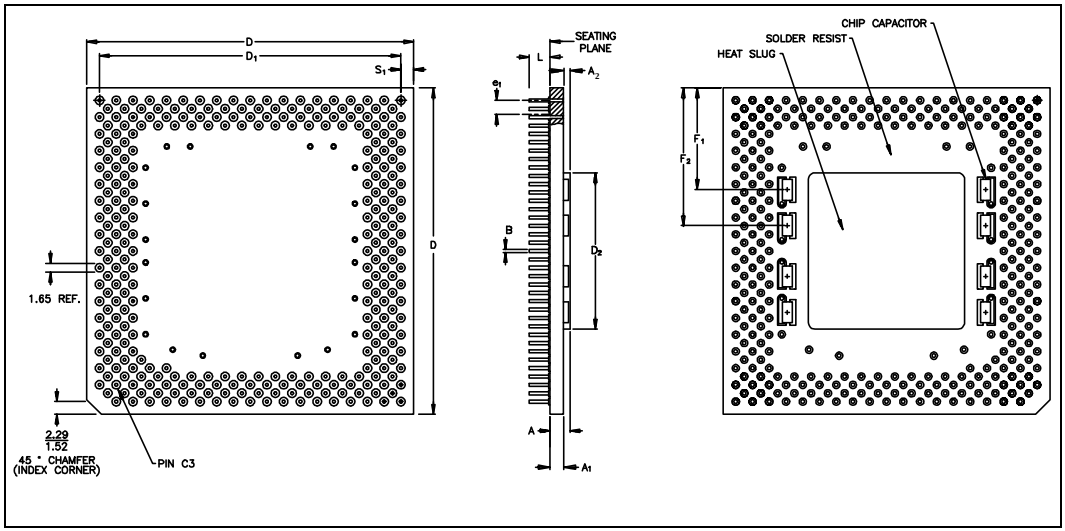


Figure 2. Plastic Pin Grid Array (PPGA) Package Dimensions

Table 2. Physical Dimensions of a 296 -Pin Staggered PPGA Package

Family: Plastic Pin Grid Array Package				
Symbol	**Millimeters**		**Inches**	
	Minimum	Maximum	Minimum	Maximum
A	2.72	3.33	0.107	0.131
A1	1.83	2.23	0.072	0.088
A2	1.00		0.039	
B	0.40	0.51	0.016	0.020
D	49.43	49.63	1.946	1.954
D1	45.59	45.85	1.795	1.805
D2	23.44	23.95	0.923	0.943
e1	2.29	2.79	0.090	0.110
F1	17.56		0.692	
F2	23.04		0.907	
L	3.05	3.30	0.120	0.130
N	296		296	
S1	1.52	2.54	0.060	0.100

2.2. Physical Structure of a PPGA Package

The PPGA package body is a pinned laminated printed circuit board (PCB) structure. Figure 3 illustrates the cross section schematic[1]. The dielectric material, which is chosen for its high temperature stability and industry history, is a glass-reinforced high glass transition temperature (Tg) Bismaleimide Triazine (BT) with a Tg ranging from 170° C to 190° C. Conductors are copper traces. For bondability, the copper (Cu) bond fingers are plated with gold (Au) over nickel (Ni). The heat slug is Ni plated copper, which gives high thermal dissipation. The Kovar pins are plated with Au over Ni.

[1] The cross section is a schematic only. It does not depict the exact stackup model of the PPGA production units.

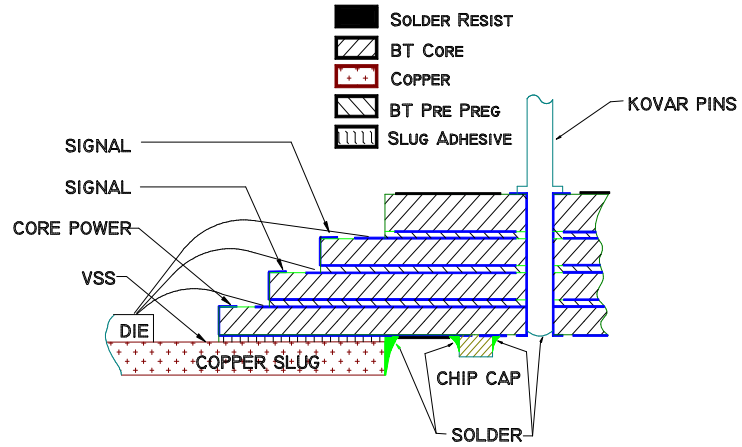
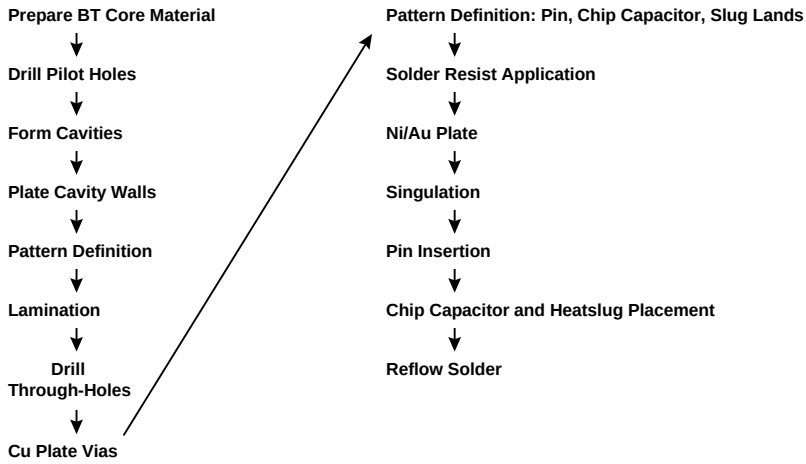


Figure 3. A PPGA Schematic Cross Section

In manufacturing the PPGA piece part, standard Printed Circuit Board (PCB) processing and equipment are used. Figure 4 lists the basic manufacturing and lamination process.



Note:
This process is performed at the piece part supplier.

Figure 4. Piece Part Substrate Manufacturing and Lamination Process

Intel's PPGA component assembly process is very similar to CPGA in both equipment and process steps. This is summarized in Figure 5.

2.3. PPGA Package Shipping Media

PPGA shipping trays meet the JEDEC standards. All external dimensions of the PPGA tray are the same as the CPGA tray. For easy identification, the PPGA tray has a brown color while the CPGA tray is blue. In addition, to reduce package free-play, the PPGA tray has slightly smaller pocket dimensions. Refer to Figure 6 for the dimensions of the PPGA shipping tray.

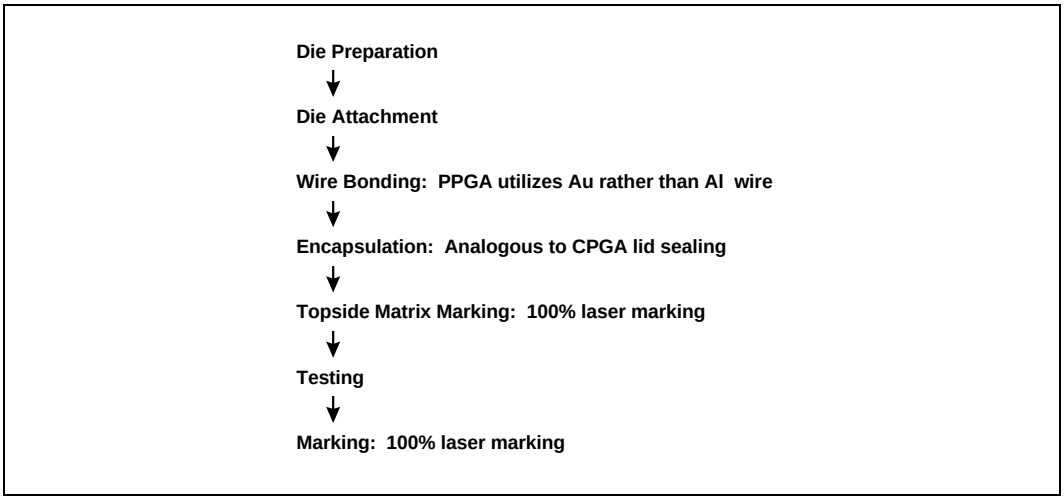


Figure 5. Intel PPGA Assembly Process

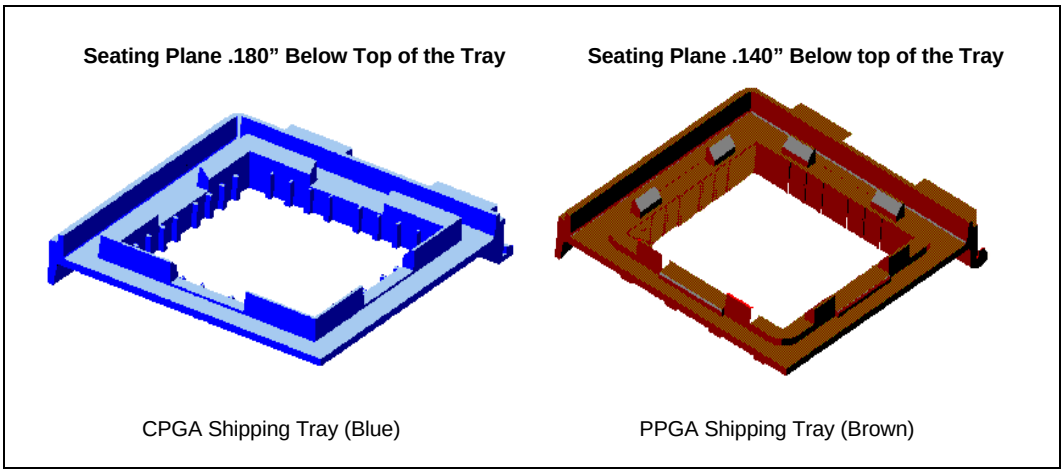


Figure 6. CPGA and PPGA Shipping Trays

3.0. PPGA PERFORMANCE CHARACTERISTICS

3.1. Thermal Characteristics

To improve the thermal performance, the PPGA package utilizes a heat slug with a high thermal conductivity. The die is attached directly to the nickel plated copper heat slug, resulting in a lower thermal resistance than the commensurate ceramic version. Based on measurements on the Pentium processor, θ_{JA}[2] of PPGA is about 1.1 ° C/W lower than that of CPGA. Appendix A details the thermal resistance values for the Pentium processor in ceramic pin grid array and plastic pin grid array packages. The benefit in thermal improvement for the PPGA package is more pronounced when the absolute power is higher and when the die size is smaller. In other words, the PPGA technology will be a preferable choice for the future generations of high power processors and systems. Figure 7 illustrates the thermal conduction and heat flux spreading of both CPGA and PPGA.

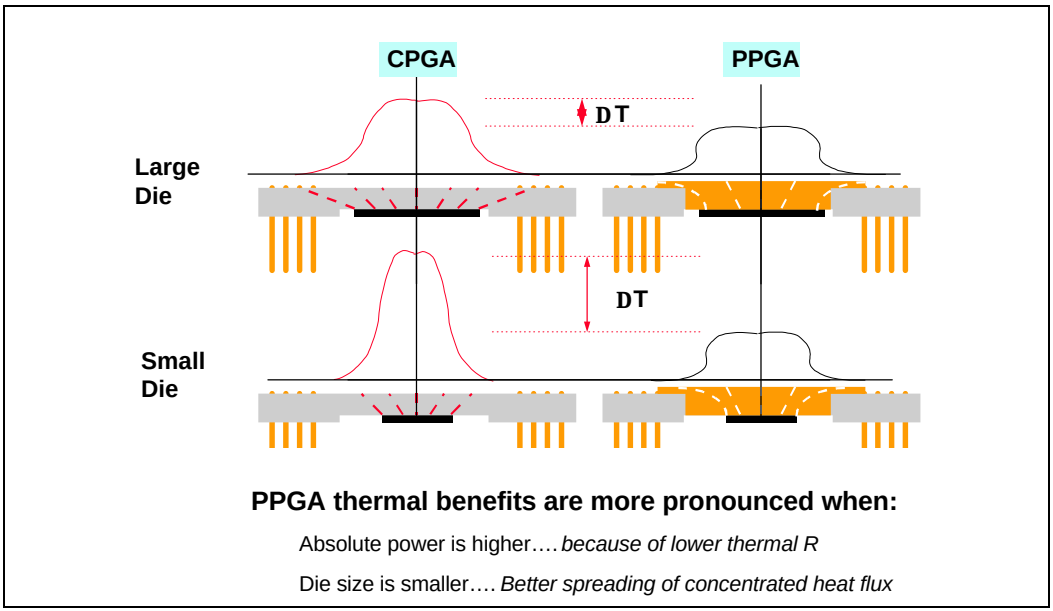


Figure 7. PPGA Has Better Thermal Conduction/Spreading

[2] θ_{JA} = junction to ambient thermal resistance (°C/W)

θ_{JC}= junction to case thermal resistance (°C/W)

θ_{CA} = case to ambient thermal resistance (°C/W)

3.2. Electrical Characteristics

3.2.1. I/O BUFFER

The package I/O model for Pentium processors in PPGA packages is shown in Figure 8 as a first order buffer model. R_O and C_O values are independent of the package and remain unchanged. Lp is the package inductance that includes bond wire inductance, trace inductance, pin inductance and socket inductance. Cp is the package capacitance consisting primarily of trace capacitance and socket capacitance. The parameter values are compiled in Table 3 and the buffer types for signals can be found in Table 4. The PPGA package input buffer model is the same as CPGA.

In this model, an effective inductance is used for the bond wire. Both self and mutual inductance are taken into account. The pin and its socket are considered as a single entity and a typical inductance value of 4.5 nH is used. A typical value of 1.0 pF is used for the socket capacitance.

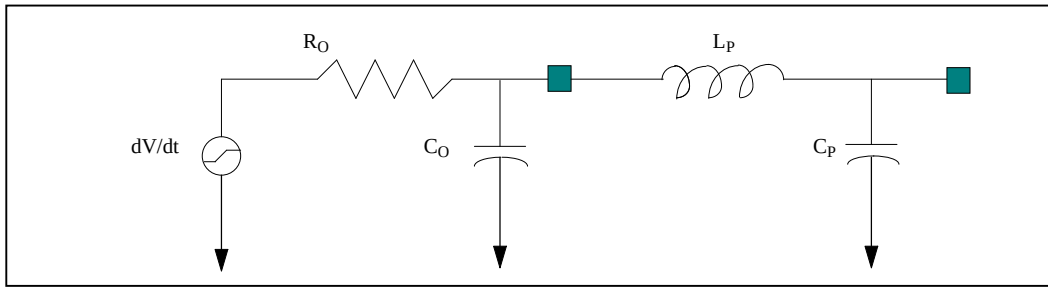


Figure 8. First Order I/O Buffer Model for PPGA

Table 3. Parameter Values for PPGA I/O Model (Pentium® Processor)

Buffer Type	Cp (pF)[1]		Lp (nH)[1]	
	min	max	min	max
ER0	3.41	3.41	9.64	9.64
ER1	3.25	5.98	9.3	11.94
ED1	3.37	5.0	9.09	14.99
EB1	3.2	5.48	9.18	15.98
EB2	3.36	5.06	9.54	14.7
EB2A	3.36	5.06	9.54	14.7
EB2B	3.36	5.06	9.54	14.7
EB3	4.72	4.72	13.24	13.24
EB4	3.7	4.03	10.57	10.7

Note:

[1] The values provided included typical socket capacitance and socket inductance.

Table 4. Signal To Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	Input		ER0
A20M, AHOLD, BF, BOFF#, BRDY#, BRDYC#, BUSCHK#, EADS#, EWBE#, FLUSH#, FRCMC#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, PICCLK, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	Input		ER1
ADSC#, APCHK, BE[7:5]#, BP[3:2], BREQ, FERR#, IERR#, PCK, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TD0, U/O#	Output	ED1	
A[31:21], AP, BE[4:0]#, CACHE#, D/C#, D[63:0], DP[8:0], HLDA, LOCK#, M/IO#, PBGNT#, PBREQ#, PHIT#, PHITM#, SCYC	Input/Output	EB1	EB1
A[20:3], ADS#, HITM#, W/R#	Input/Output	EB2/A/B	EB2
HIT#	Input/Output	EB3	EB3
PICD0, PICD1	Input/Output	EB4	EB4

3.2.2. SIGNAL QUALITY

Intel has performed noise measurements on the Pentium processors in both CPGA and PPGA packages. The results show that at the component level, the PPGA packages are comparable with the CPGA packages. In addition, the results indicate that all PPGA parts have a higher mean-core-power supply level than CPGA parts.

3.2.3. EMI

The Federal Communications Commission (FCC) has set limits on the maximum radiation from electrical systems. In turn, each component in a system should not exceed the typical level that is allocated to it. Electromagnetic Interference (EMI) levels from Intel's Pentium processors in ceramic pin grid array (CPGA) and PPGA packages have been measured with and without heat sinks attached. Measurements were performed up to a core clock frequency of 280 MHz. EMI levels are well below critical levels at all clock speeds tested. There is no significant EMI performance difference between CPGA and PPGA.

3.3. Mechanical Characteristics

3.3.1. MECHANICAL FIT

Note

Intel suggests that, when performing insertion and extraction, the maximum force should not exceed 100 lbs. For better manufacturing control, Intel also suggests that the force be placed on the pin matrix area uniformly, rather than on the heat slug. The insertion and extraction tooling should take into account the clearance for the external capacitors and the heat slug.

In order to ensure that PPGA packages are mechanically interchangeable with CPGA packages, Intel did extensive studies on mechanical fit, including insertion/extraction force, peak compressive force, clip force and heat sink attachment.

For the maximum insertion force measurement, the 296L PPGA packages were inserted at a rate of 1.27 mm/min (0.050 in/min). To understand the worst case scenario, the insertion force was applied uniformly on the entire heat slug surface of the package. A steel plate was glued to the package using a room

temperature cure adhesive. A stud was then attached to the plate to perform the extraction tests.

PPGA package insertion/extraction forces were measured with low insertion force (LIF) and zero insertion force (ZIF) sockets from different vendors. The socket insertion process involves applying an increasing amount of pressure on a package as it is inserted into the position in the socket. The applied load overcomes the frictional resistance applied to the package pins by the contact receptacles in the socket. If the socket receptacle structure is simple, the applied force increases smoothly as the package is inserted and the load-displacement curve is usually linear. When the package is completely inserted and any additional force will cause the package/socket assembly to bend together, the load-displacement curve will show a change in slope. The insertion force in this case is defined as the point where the load-displacement curve shows a final distinct change in slope.

To reduce the insertion force, some socket vendors stagger the placement of the pins in the socket body in the "Z" direction. The load-displacement curve in this case is no longer a simple linear curve. From the package integrity perspective, the maximum force seen by the package before complete insertion is critical. The maximum force, indicated by the point of final change in slope of the load-displacement curve is defined as insertion force. Table 5 summarizes the average measured insertion and extraction force with different sockets.

Components can be inserted into all socket types tested and still meet the suggested maximum loading of 100 lbs. Separate studies of package integrity have demonstrated that the PPGA package can sustain this level of applied normal compressive force plus margin.

The peak compressive force was uniformly distributed over the package heat slug while the PPGA unit rested on a PCB which contained a matrix of through-hole vias allowing for pin insertion. The rate at which the force was applied was 0.76 mm/minute (30 mils/minute). After the force was applied, each package was examined and no apparent physical changes were observed. Then each package was tested electrically and each package passed all electrical test parameters. Finally each package was inspected using Through Scan Acoustic Microscopy (TSAM) imaging. The result exhibited no significant changes and the cross section results confirmed that there was no delamination or internal package cracking .

3.3.2. HEAT SINK ATTACHMENT

3.3.2.1. Thermal Interface Material

CAUTION

Components on top (and exposed metal on the sides) of the PPGA packages can be shorted by any electrically conductive materials including heat sinks, thermal grease(if electrically conductive) and thermal grease foil carriers (if electrically conductive)

To ensure that PPGA packages are mechanically compatible with CPGA, Intel has performed a comprehensive evaluation of the effective method of heat sink attachment. Intel suggests that the interface material used for heat sink attachment should have the thermal conductivity greater than 0.8 W/mK, and should be electrically insulating. The volume resistivity of the material should be greater than $1x10^6$ Ohm-cm. Intel has demonstrated that Thermalcote I* Conductacoat* with a flat aluminum foil carrier is an effective interface material for the Pentium® processor heat sink. Shaped or curved conductive foil carriers are not recommended with the PPGA package.

Table 5. PPGA Insertion/Extraction Force Measurement

Socket[1]	Average Insertion Force (lb.)	Average Extraction Force (lb.)
Preci-Con LIF	44.69	57.43
Mill-Max LIF	38.09	49.65
Robinson Nugent LIF	78.35	73.51
AMP LIF	65.06	69.91
Andon LIF	54.26	58.58
Yamaichi ZIFs	n/a	80.94[2]

Notes:

1 These data do not constitute a recommendation for any specific supplier or part number.

2 This is measured when the socket is in the "closed" position.

3.3.2.2. Clip Design and Attach

A minimum clip force of 5 lbs is recommended. Clips retain the heat sink assembly in the socket by exerting a force on the heat sink and the socket. The clip force, in turn, aids in forcing the grease to fill the many microscopic peaks and valleys on the heat sink and package surface, thereby reducing the interface thermal resistance. Since the quantity of grease squeezed out is different depending on the clip, the corresponding bond line thickness of the grease will affect thermal performance.

3.3.2.3. Thermal Test Results

296-pin PPGA packages were used as test vehicles. The assemblies of packages with a Thermalloy heat sink (0.87" tall) and a steel spring clip were tested inside a wind tunnel at a power setup of 10 W and an air flow rate of 300 LFM .

Test samples were subjected to the following stress test conditions: (1) 50 cycles of Temperature Cycle (T/C) from - 40 to 70° C; (2) 60 hours of aging at 150° C; (3) 120 hours of 92 percent humidity at 55° C. Junction to ambient thermal resistance (θ_{JA}) was measured before and after each stress. The failure criteria was defined as an increase of more than 1° C at 10 W in the junction temperature when measured after stressing. The results showed that there is no significant degradation of thermal performance for Thermalcote I Conductac oat after reliability stressing.

The effect of foil sizes, clip force and voiding on Thermalcote I* Conductacoat* thermal performance was also explored. If there is an insufficient amout of grease on the Al foil, voiding will exist in the bond line. This results in higher θ_{ja} values. While up to 30% grease voiding can be tolerated without any impact on PPGA thermal performance, zero voiding is strongly recommended for any heat sink attachment methods.

A larger foil size will cover a larger area with grease, but a smaller foil size is preferred for handling. For instance, thermal resistance θ_{ja} measured with a 1.0" x 1.0" foil is 0.1 C/W to 0.2 C/W lower than θ_{ja} measured with a smaller foil (0.7" x 0.7"). In addition, if the foil dimensions exceed that of the heatslug, the risk of shorting the external capacitors will greatly increase. Note that the aluminum foil is a carrier specific for Thermalcote I* Conductacoat* grease to aid volume manufacturing. OEMs should decide whether to use flat aluminum foils based on their particular heat sink attachment methods and assembly lines.

Clip force determines the thermal grease bond line thickness and directly impacts thermal performance. To determine the effect of clip force on thermal performance, θ_{JA} and θ_{CS}[3] values for the heat sink assemblies were measured at different clip forces. The actual clip forces of these modified clips were individually measured by using a Material Testing System (MTS) before the thermal resistance measurement. All clip forces were also verified by using MTS after the thermal resistance measurement. Figures 9 shows θ_{JA} and θ_{CS} values versus clip force, respectively. The result indicates that as long as clip force is higher than 5 lbs (corresponding to ~ 5 psi),

3 θ_{CS}= case to heatsink thermal resistance (°C/W)

there is no significant effect of clip force on PPGA thermal performance.

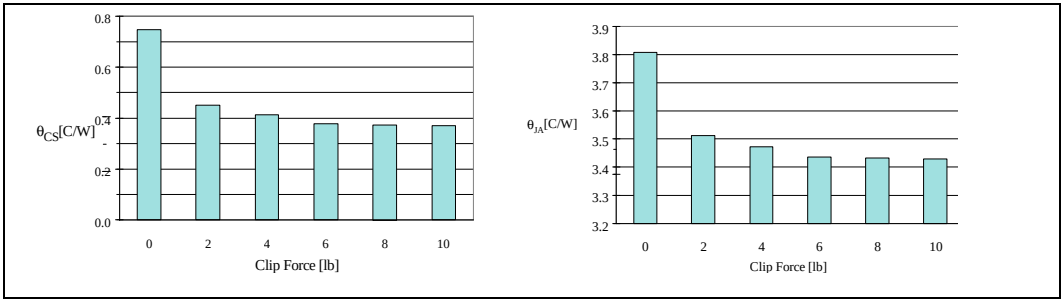


Figure 9. Comparison of q_{CS} and q_{JA} for Different Clip Forces

The new PPGA package may affect some existing heat sink designs. In one design, shown in Figure 10, the heat sink has a lip designed for CPGA Pentium processors to prevent movement of the heat sink relative to the package, socket and clip during mechanical shock tests. However, the new PPGA package has a heat slug, external capacitors, and exposed pins on the top side of the package. On the PPGA package, if the heat sink slips out of its secured position, the lip may touch the exposed pins. Therefore, the lip needs to be extended to a proper length to lock the heat sink in a secured position. Intel's evaluations indicate that a 50 mil lip is not adequate and that a 70 mil lip is needed to ensure reliable performance. Our tests also show that the 70 mil lip works well with CPGA packages. In addition, the side of the package has exposed metal that is electrically conductive. If the heat sink is electrically conductive, and the lip touches the side of the package, electrical shorting may occur, causing damage to the processor.

There may be other instances where heat sink designs need minor modifications to fit both the new PPGA package and the existing CPGA package. Customers need to work with their heat sink suppliers to ensure that their heat sink designs can accommodate both the PPGA and CPGA packages.

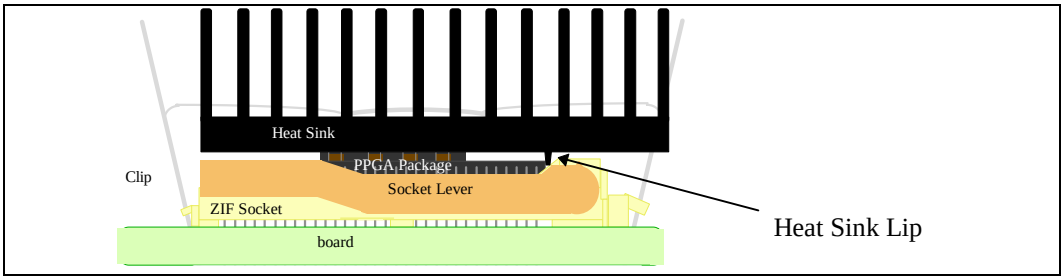


Figure 10. A Heat Sink Design With a Lip

3.4. Quality and Reliability

To ensure that the PPGA package continues to meet performance requirements over time, Intel performed extensive reliability stress tests, including temperature cycle, temperature/humidity/bias, high temperature life test, and steam. Thermal, mechanical shock and vibration stress tests were also performed as part of the system level evaluation. Table 6 lists some of the reliability tests performed on PPGA packages. The quality and reliability test results meet Intel's requirements.

4.0. SYSTEM LEVEL CHARACTERIZATION

The Plastic Pin Grid Array (PPGA) package was evaluated as a drop-in replacement for the Ceramic PGA package for present and future Intel board designs.

First, the impact of the PPGA package on board assembly was studied by assembling PPGA packages into sockets soldered on boards. These packages were split equally between LIF and ZIF sockets and the process steps included the application of thermal grease, and attachment of heat sinks and clips. No major issues were discovered during this evaluation. This indicates that introduction of the PPGA will cause no adverse impact on the manufacturing process flow for assembling boards.

Second, the PPGA package integrity and reliability under board and system level environmental stress tests were ascertained . The PPGA packages with the Pentium processors, assembled on a server CPU module, were subjected to thermal shock, vibration, mechanical shock, humidity, and temperature and voltage limits tests. After each test, the CPU modules were checked for functionality. Every module passed after each test.

4.1. System Level Assembly and Manufacturing

The goal for this phase was to identify incompatible process, tooling, materials and handling issues for the PPGA package in comparison to the CPGA on Intel's manufacturing line.

The sequence for assembling the PPGA packages in sockets soldered onto boards was:

- Visual inspection under 10X magnification
- Sockets were wave soldered on each dummy test board. Half of the sockets were ZIF sockets and the other half were 296-pin LIF sockets.
- Multiple boards were assembled with the sockets
- After wave soldering, the boards were delivered to the heat sink assembly area.
- PPGA components were inserted into the ZIF and LIF sockets per standard procedure. A lubricant is typically also sprayed on the socket to aid in this insertion process. ZIF socket insertions are done manually.
- Next, a grease foil was placed on top of the package.

Table 6. Some PPGA Reliability Tests

	Stress Test	Duration	Stress Condition
Package Level	Temperature Cycle "B"	1000 cycles	-55° C to 125° C
	Temperature Humidity Bias (85/85)	1000 hours	T = 85° C, Humidity = 85%
	Biased Life Test	1000 hours	
	Steam Stress	168 hours	T = 121° C, Pressure = 2 Atm
System Level	Thermal Shock		T = -40° C to +70° C
	Mechanical Shock		50 grams and averages 3 shakes per axis
	Vibration		Random frequencies between 20 Hz to 2000 Hz

- The heat sink was placed on the package, the heat sink clip was hooked on to the socket.
- After the assembly process was completed, the heat sink assemblies were disassembled, the PPGA packages were removed from the sockets and inspected under 10X magnification for damage.

The test results did not show any damage to any of the PPGA packages. The use of PPGA packages required no manufacturing process change.

Note:

Insertion tooling may need to be modified for the clearance due to the external capacitors on top of the package. No problem has been observed in the evaluation process related to foil misalignment on the heat slug causing shorts between the adjacent capacitors. Use manufacturing controls when stacking up the processor, thermal interface and the heat sink to avoid foil misplacement on the PPGA package heat slug.

4.2. Quality and Reliability

PPGA Packages with Pentium processor devices were the test vehicles for this evaluation. These PPGA packages were inserted into LIF sockets on typical server product type boards. These boards have one Pentium processor with an expandable cache. Table 7 details the environmental tests to which the boards were subjected.

After each of the stress tests described above, a functional test was performed to verify that the boards under test were functional. All the boards tested passed after every environmental stress test exposure and they were functional at the end of the entire test sequence. The PPGA packages passed the typical Intel board and system level environmental stress exposure tests.

Table 7. Environment Stress Exposure Evaluation

Thermal Shock Test (Non-operating)	-40° C to 70° C for 50 hours, at a rate of 15 °C to 30° C /minute
Vibration Test	10 minutes per axis for all 3 axes. 5 Hz to 20 Hz at a rate of 0.01 g^2/Hz to 0.02 g^2/Hz 20 Hz to 200 Hz at a rate of 0.02 g^2/Hz
Mechanical Shock	Trapezoidal 50G, 11 msec at a velocity change of 170 inches/sec
Temperature/Voltage Corner Tests	0° C, +4.75 V, +11.4 V 0° C, +5.25 V, +12.6 V 55° C, +4.74 V, +11.4 V 55° C, +5.25 V, +12.6 V
Humidity Test	95% humidity at a temperature range from 25 °C to 65° C for 240 hours

5.0. PERFORMANCE COMPARISON BETWEEN PPGA AND CPGA

5.1. Package Level Comparison

The PPGA package provides increased availability of high frequency microprocessors, and provides better system thermal margin. Moreover, as the die size continues to shrink, the concentrated heat flux becomes critical. Hence effective heat spreading will significantly improve the processor performance.

Figure 11 details the package trace for CPGA and PPGA. Because of the different metallization, the trace metal of the CPGA package being tungsten and that of the PPGA being copper, the resistance is lower in PPGA package, yielding lower IR drop. Therefore a higher core voltage is achieved when PPGA is used. Intel guarantees that the product I/O timing specifications will not change from one package type to another.

5.2. System Level Comparison

A 120 MHz Pentium processor in a CPGA package was compared to a 120 MHz Pentium processor in a PPGA package for its thermal effectiveness in a typical server chassis. The conditions under which these two packages were tested were identical. The heat sink and thermal interface compound used was also the same. The case temperatures of the packages were measured and recorded for comparison. The results show a 5° C to 6° C difference between the margin of the two packages, with the device in the PPGA package running cooler than that in the CPGA package. It can be concluded that the device in a PPGA package can be installed in any system that currently has the same device in a CPGA package.

6.0. CONCLUSION

The new PPGA package outperforms the CPGA package electrically and thermally. In addition to providing increased availability of high-performance microprocessors, it is compatible with CPGA board manufacturing processes and is board-level reliability compliant. The interchangeability ensures that the thermal design solutions for PPGA package are compatible with the existing CPGA thermal designs.

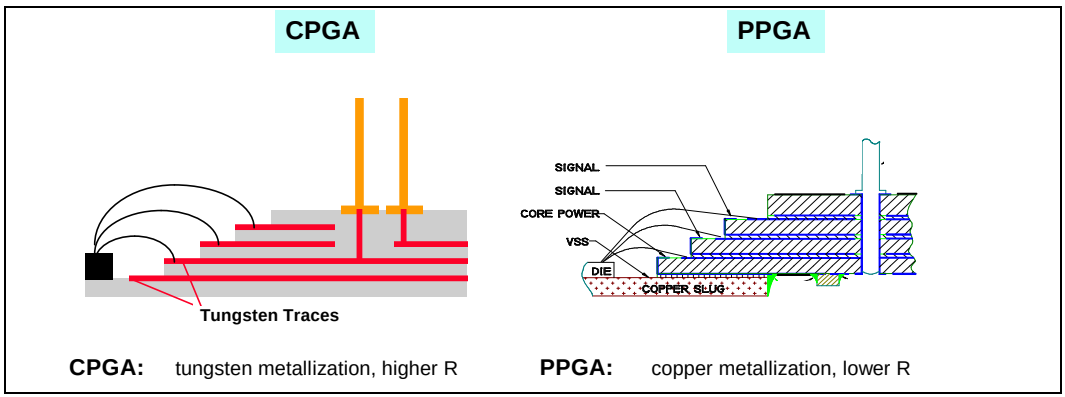


Figure 11. PPGA Has Lower Trace Resistance

APPENDIX A. THERMAL RESISTANCE VALUES FOR PENTIUM® PROCESSOR CB1 IN CPGA (WITHOUT HEAT SPREADER) AND IN PPGA

Table A-1: q_{CA}[°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)

	q_{CA}[°C/W] vs Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25”	9.4	8.3	6.9	4.7	3.9	3.3
0.35”	9.1	7.8	6.3	4.3	3.6	3.1
0.45”	8.7	7.3	5.6	3.9	3.2	2.8
0.55”	8.4	6.8	5.0	3.5	2.9	2.6
0.65”	8.0	6.3	4.6	3.3	2.7	2.4
0.80”	7.3	5.6	4.2	2.9	2.5	2.3
1.00”	6.6	4.9	3.9	2.9	2.4	2.1
1.20”	6.2	4.6	3.6	2.7	2.3	2.1
1.40”	5.7	4.2	3.3	2.5	2.2	2.0
1.50”	5.5	4.1	3.1	2.4	2.2	2.0
None	14.5	13.8	12.6	10.5	8.6	7.5

Note:

θ_{CA} is case to ambient thermal resistance. θ_{CA} values shown in this table are typical values. The actual q θ_{CA} values depends on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

Table A-2: q_{JC}[°C/W] for a CPGA Package With and Without a Heat Sink

	No Heat Sink	**With Heat Sink**
Average q_{JC}	1.7	1.25

Table A-3: q_{JA}[℃/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)

	q_{JA} ℃/W] verses Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25”	10.6	9.5	8.1	5.9	5.1	4.5
0.35”	10.3	9.0	7.5	5.5	4.8	4.3
0.45”	9.9	8.5	6.8	5.1	4.4	4.0
0.55”	9.6	8.0	6.2	4.7	4.1	3.8
0.65”	9.2	7.5	5.8	4.5	3.9	3.6
0.80”	8.5	6.8	5.4	4.1	3.7	3.5
1.00”	7.8	6.1	5.1	4.1	3.6	3.3
1.20”	7.4	5.8	4.8	3.9	3.5	3.3
1.40”	6.9	5.4	4.5	3.7	3.4	3.2
1.50”	6.7	5.3	4.3	3.6	3.4	3.2
None	16.2	15.5	14.3	12.2	10.3	9.2

Table A-4: q_{CA}[℃/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)

	q_{CA}[℃/W] verses Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25”	9.0	7.9	6.5	4.3	3.5	2.9
0.35”	8.7	7.4	5.9	3.9	3.2	2.7
0.45”	8.3	6.9	5.2	3.5	2.8	2.4
0.55”	8.0	6.4	4.6	3.1	2.5	2.2
0.65”	7.6	5.9	4.2	2.9	2.3	2.0
0.80”	6.9	5.2	3.8	2.5	2.1	1.9
1.00”	6.2	4.5	3.5	2.5	2.0	1.7
1.20”	5.8	4.2	3.2	2.3	1.9	1.7
1.40”	5.3	3.8	2.9	2.1	1.8	1.6
1.50”	5.1	3.7	2.7	2.0	1.8	1.6
None	13.0	12.3	11.4	8.0	6.6	5.7

Note:

θ_{CA} is case to ambient thermal resistance. θ_{CA} values shown in this table are typical values. The actual θ_{CA} values depends on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

Table A-5: q_{JC}[℃/W] for a PPGA Package With and Without a Heat Sink

	No Heat Sink	With Heat Sink
Average q_{JC}	1.3	0.50

Table A-6: q_{JA}[℃/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)

	q_{JA}[℃/W] verses Air Flow Rate [LFM]					
Heat Sink Height	0	100	200	400	600	800
0.25”	9.5	8.4	7.0	4.8	4.0	3.4
0.35”	9.2	7.9	6.4	4.4	3.7	3.2
0.45”	8.8	7.4	5.7	4.0	3.3	2.9
0.55”	8.5	6.9	5.1	3.6	3.0	2.7
0.65”	8.1	6.4	4.7	3.4	2.8	2.5
0.80”	7.4	5.7	4.3	3.0	2.6	2.4
1.00”	6.7	5.0	4.0	3.0	2.5	2.2
1.20”	6.3	4.7	3.7	2.8	2.4	2.2
1.40”	5.8	4.3	3.4	2.6	2.3	2.1
1.50”	5.6	4.2	3.2	2.5	2.3	2.1
None	14.3	13.6	12.7	9.3	7.9	7.0

APPENDIX B. FREQUENTLY ASKED QUESTIONS

1. Does Intel have any plans to cover the exposed circuitry on the slug side of the PPGA package?

Intel has no plans to pursue protective coatings on top of the current organic package. Exposed circuitry is not new to the component or PC board industries. World-class manufacturing techniques will ensure that shorting/damage does not occur.

2. What are the concerns in attaching a heat sink clip to the package rather than the socket?

Repeated installation/removal of the clip can cause damage to the package edge as it is PC board material rather than ceramic. Additionally, our tests indicate that if the combined mass of package and heat sink is greater than ~135 grams, the assembly can vibrate out of certain type 5 or 7 ZIF sockets during shock and vibration testing. If heat sink attach to the package is going to be used, the customer should evaluate the assembly fully for these types of issues. The majority of Intel data was taken attaching the heat sink clip to the socket.

3. Does Intel plan to add either product or S-spec marking to the heat slug?

Intel has no current plans to change the marking on the PPGA. The product speed code is marked on the heat slug.

4. Is Intel considering changing the color of the PPGA shipping tray to make it more distinguishable from the CPGA tray to distinguish product/speed?

The production version of the PPGA shipping tray is brown in color to distinguish it from the CPGA tray (blue). No other changes were made to the original PPGA tray. Production units will be shipped in the brown tray.

5. Is Intel considering an 85 °C T_{CASE} rating for this package?

PPGA thermal efficiency is a factor in enabling Intel to offer higher performance processors. We have no plans to increase T_{CASE} at the expense of performance.

6. In view of the PPGA package's superior thermal and electrical properties, will the same product in CPGA be interchangeable with PPGA?

Intel guarantees that all Pentium processors in the PPGA package meet the same AC/DC specifications as those in the CPGA package.

7. Will protective shipping bags be used to prevent foreign material accumulation during shipping or storage?

The PPGA package will be shipped in the same manner as the CPGA package. The shipping box itself offers protection from foreign material.

8. What is the maximum heat sink clip force that can be applied?

100 lbs is the maximum force. Experiments have shown that 5 lbs is sufficient to achieve optimum thermal transfer between the package slug and heats sink when thermal grease is used. Due to the slight package thickness increase when compared to the CPGA package, clip force will increase by approximately 5 percent when applying CPGA clips to the PPGA package. Before applying a CPGA heat sink, be sure to verify that it has proper clearance and will fit the PPGA package.

9. Is Intel planning to provide a video or other training on how to handle this package in a manufacturing environment?

We have no plans to offer any specialized training.

10. What is the total capacitance of the CPGA package and how does it compare to PPGA total capacitance?

The CPGA package capacitance is 14 nfds. The goal in design was to match effective series inductance between the packages rather than capacitance. Due to the capacitor layout, termination differences, and relative locations in relation to the die, the CPGA package requires considerably less total capacitance than the PPGA package's 120 nfds.

11. What are the flammability ratings for the encap and BT material used in the package?

The PPGA package passes the "Needle Flame Test" per IES 695-2-2. The samples do not support flaming time nor do they have any flaming particles. The Oxygen Index Test has been conducted. 24 percent oxygen is the minimum concentration that will support flaming. Copies of the UL reports are available.

12. Will Intel provide guidelines or recommendations for both passive and active heat sinks?

Intel has addressed the potential risk associated with an improperly designed heat sink and provide an example in the application note *An Introduction to Plastic Pin Grid Array (PPGA) Packaging*, along with a list of the heat sink suppliers to whom Intel has disclosed the new PPGA package. However we will not provide recommendations for passive or active heat sinks, since thermal solutions are customer unique.

13. Are there any concerns/issues with inserting the package after the heat slug is epoxied to the slug (insertion pressure will be applied to the slug rather than the pin matrix area)?

We expect no issues if force is applied uniformly and parallel to the plane of the package to ensure no heat sink tilt occurs and total force is kept below 100 lbs.

14. Can Intel supply its thermal modeling data or thermal test chips so customers can run their own simulations?

We can supply modeling data as to the effect of airflow LFM on heat sink size. This should be requested from your Field Applications Engineer (FAE).

15. Will Intel provide data on additional thermal interface materials?

Intel evaluated TC-208 and chose not to use it as it did not meet our manufacturing process dry out requirements. Our application note, *An Introduction to Plastic Pin Grid Array (PPGA) Packaging*, (Order Number 243103-001) references Thermalcote I. Other materials may have similar performance but we have no plans to provide data on any other materials.

16. Does Intel have any recommendations for epoxy or tape heat sink attach?

No. Manufacturers planning to use these materials should run their own evaluations. Intel will not model or run stress evaluations on specific customer applications.

17. Can Intel supply a representative drawing for component insertion and extraction tools for LIF sockets?

We have a drawing for a recess arbor press platen. Socket manufacturers should be contacted for extraction tools applicable to their specific socket.

18. Does Intel have any plans to cover the sides of the PPGA package, which has exposed metal and is electrically conductive?

Intel has no plans to pursue protective coatings on the side of the current organic package. World class manufacturing techniques will ensure that shorting/damage does not occur. Please refer to this application note for recommendation of implementation.

APPENDIX C. HEAT SINK/FANSINK AND SOCKET SUPPLIERS

Heat Sink/ Fansink Suppliers	Address of Suppliers	Contact	Phone	Fax
Aavid	One Kool Path P.O.Box 400 Laconia, NH 03247	Gary Kuzmin	(603) 528-3400	(603) 528-1478
Des Tech	No.463, Kang Ning St Hsi Chih Chen, Taipei 22121, Taiwan	Jason Hsu	886-6-695-0462	886-2-695-0462
Evox Rifa	300 Tri-State International Suite 375 Lincolnshire, IL 60069	Andrews Bellavia	(847) 948-9511	(847) 948-9320
Global Win Technology	IF, No. 366, Tanan Rd. Shih Lin, Taipei, Taiwan	Andy Lin	886-2-891-7388	886-2-881-7219
IERC	135 W. Magnolia Blvd. Burbank, CA 91502	Guy Addis	(818) 842-7277	(818) 848-8872
Johnson Matthey	15128 East Euclid Ave. Spokane, WA 99216	Brent Bollong	(509) 922-8702	N/A
Megaland Inc.	4962 El Camino Real Suite #109 Los Altos, CA 94022	Wayne Clement	(415) 967-2800	(415) 967-2878
Sanyo-Denki (Keymarc)	1-15 Kita Ohtsuka Toshima, Tokyo 170, Japan	James Sia	(310) 787-6825	813-3-917-4521
Thermalloy	2021 W. Valley View Lane Dallas, TX 75234	Larry Tucker	(214) 243-4321	(214) 241-4656
Chip Coolers*, Inc.	333 Strawberry Field Rd. Warwick, RI 02886	William B. Rife	(800) 227-0254	(401) 732-6119
EG&G Wakefield Engineering	60 Audubon Rd. Wakefield, MA 01880	David Saums	(617) 245-5900	(617) 246-0874

Socket Suppliers	Address of Suppliers	Contact	Phone	Fax
AMP	19200 Stevens Creek Blvd. Cupertino, CA 95014	Berny Kulwin	(408) 725-4984	(408) 725-4997
Andon	4 Court Drive Lincoln, RI 02865	John Tate	(410) 333-0388	(410) 333-0287
Bergquist	5300 Edina Industrial Blvd. Edina, MN 55435	Kevin Hanson	(612) 835-9096 x172	(612) 835-4156
Burndy	51 Richards Ave., P.O.Box5200, Norwalk, CT 06856	Ed Hrvatin	(203) 852-8553	(203) 852-8556
Loranger	3000 Scott Blvd. Santa Clara, CA 95050	Whitney Sharp	(408) 727-4234	(408) 727-5842
Mill Max	190 Pine Hollow Rd. Oyster Bay, NY 11771	Roger Sutcliffe	(516) 922-6000 x209	(516) 922-0023