Converting From the NMOS MCS 96 Family Members to the CHMOS 8XC196KB

The 80C196 is the replacement for the NMOS 8X9X. The part can be configured to be pin compatible with the 8096, but because of the process change and other enhancements, it may not be plug compatible in some designs. The are a few design considerations in making this conversion from the NMOS devices to the 8XC196KB and later devices.

This document will cover the changes in 2 sections. The first section takes you from the NMOS 8X9X-90 to the NMOS 8X9XBH. This is for those who wish to upgrade from the 8X9X-90, and will need to know the difference between the 8X9X-90 and the 8X9XBH in order to understand the second section. The second section then takes you from the NMOS 8X9XBH or 8X9XJF to the CHMOS 8XC196KB.

The purpose of this document is to aid designers who are moving from any NMOS MCS 96 family member to the 8XC196KB. It assumes a thorough understanding of the 8X9X-90, the 8X9XBH or the 8X9XJF. This document will only identify the differences between the 8X9X-90, the 8X9XBH, the 8X9XJF and the 8XC196KB. For more information on any differences consult the current 16-bit Embedded Controller handbook and corresponding data sheets.

For the remainder of this document, the 8X9X-90 will be referred to as the “-90”, the 8X9XBH will be referred to as the "BH", the 8X9XJF as the "JF", and the 8XC196KB as the "KB". Unless otherwise noted, all references to the BH also apply to the JF.

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I. UPGRADE PATH FROM 8X9X-90 TO THE 8X9XBH

Converting applications that use an 8X9X-90 to use an 8X9XBH requires consideration of a few of the BH enhancements. Descriptions of each of the differences between the -90 and the BH follow, along with a discussion of the implications of the change.

BHE# and INST are latched: The bus control signals BHE# and INST are valid throughout the bus cycle on 8X9XBH devices. On -90 devices, these signals need to be latched on the falling edge of ALE.

Byte Read following RESET# rising: The bus control and buswidth options of 8X9XBH devices are selected by configuration of the chip immediately following the rising edge of RESET#. During the usual 10 state reset sequence, BH parts will perform a byte read of location 2018H to acquire configuration information prior to fetching the first opcode at location 2080H. The 8X9X-90 does not perform this read.

ALE is high while in reset: The ALE/ADV# pin of the 8X9XBH is driven high while the RESET# pin is held low. On -90 devices, ALE is driven low while in RESET. Circuits which rely on the state of ALE while RESET is low must be modified. The reset state of ALE was changed to enable implementation of the Chip Configuration Byte tread from external memory following the rising edge of RESET.

EA# is latched on RESET# rising: The 8X9XBH latches the value of EA# on the rising edge of RESET#. On -90 devices, EA# was not latched and could be changed without placing the part in RESET#. This change was necessary to enhance ROM/EPROM security. Circuits that rely on EA# not being latched must be modified.

A/D speed increased: The 8X95BH and 8X97BH A/D converters complete conversion in 88 state times. On -90 devices with A/D converters, a conversion takes 168 state times. This translates in an increased conversion speed from 42 microseconds on -90 parts to 22 microseconds on BH parts running at 12 MHz. Software that relies upon the speed of conversion for timing must be changed. It is also recommended that MCS-96 software be written so as to not be impacted by further changes in A/D conversion speed.

Sample/Hold on A/D: The 8X95BH and 8X97BH have a sample/hold on the input of the A/D converter. 8X9X-90 devices with a/D converters do not have sample/hold circuitry. External analog circuitry which also includes a sample/hold must provide a settled analog input within the first four state times of 8X9XBH conversion.

Duplicate Fetches: The 8X9XBH bus controller was made more aggressive when it comes to instruction fetches in order to minimize the execution speed degradation of using an 8-bit bus. As a result, instruction fetches over a 16-bit bus sometimes occur when there is no space in the prefetch queue to store the fetched opcodes. This requires another instruction fetch from the same address when space in the prefetch queue opens up.

To the external system, these occurrences appear as duplicate instruction fetches. An estimated 10 percent of all instruction fetches will be “duplicates”, while overall bus loading will be approximately 65 to 70 percent, compared to an 8X9X-90 bus loading of approximately 55 to 60 percent. Execution speed is not impacted by a duplicate fetch.

Write Pulse Width: The 8X9XBH 16-bit bus write pulse width is one T_{OSC} longer than on the 8X9X-90, thus allowing slower memories and peripherals to be used. In order to widen the WR# pulse width, the time between the end of WR# pulse width, the time between the end of WR# and the next ALE was reduced by T_{OSC}. Note that the signals WRL#, WRH#, and WR# with an 8-bit bus are still the same width as on -90 parts.

V_{PP} Replaces V_{BB}: V_{PP} is the programming pin for EPROM devices. Systems that have this connected through a capacitor to ANGND (required on 8X9X-90 parts) do not need to change. ANGND must be held nominally at the same potential as V_{SS}, and V_{PP} must NOT be connected to V_{CC}. High voltage must NEVER be placed on the V_{PP} pin of a ROM device.

While there is almost no reason to do so, an application should not attempt to execute with the EA pin at logic zero and V_{CC} at 5.5 V_{DC} on an 879XBH EPROM device. Additionally, the design should always begin the “out of RESET” code execution from the internal EPROM, immediately after the power-on sequence.

Reserved location warning: Intel reserved addresses can not be used by applications which use 8X9XBH internal ROM/EPROM. The data read from a reserved location is not guaranteed, and a write to any reserved location could cause unpredictable results. When attempting to program Intel Reserved addresses, the data must be 0FFFFH to ensure a harmless result. When mapped to external memory, Intel Reserved locations must be filled with 0FFFFH to ensure compatibility with future parts.

A positive transition on NMI: The 8X9XBH does not clear the Watchdog Timer. The 8X9X-90 does clear the WDT on a positive transition of NMI, and both parts vector to external address 0000H.

II. CONVERTING FROM THE 8X9XBH OR 8X9XJF TO THE 8XC196KB

The 8XC196KB is upward compatible with the 8X9XBH and 8X9XJF. The 8XC196KB maintains the same architecture, instruction set, and peripheral set as the 8X9XBH and 8X9XJF. It also provides increased performance with lower power consumption and enhanced features.

1. 80C196 OVERVIEW

First, some background on the 80C196 is needed. The opcode set is a true super set of the 8096, but some enhancements have been made to the peripherals and timings. The crystal is divided by 2 on the 80C196, instead of 3, as on the 8096. This means that the 80C196 running at 8 MHz will have a 250 Ns state time, just like an 8096 running at 12 MHz.

An 80C196 running at 8 MHz will emulate an 8096 at 12 MHz except that some of the instructions and peripherals will operate faster. The instructions which will be speeded up include mul, div, interrupt, call ret, and jumps. The serial port will require a different baud value and the A to D may not run at exactly the same speed. This means that timing loops which measure instruction speed or A to D completion speed may have to be modified. The bus timings, while not nanosecond for nanosecond compatible, will work in most systems.

2. DESIGN CONSIDERATIONS

1) Do not use undefined register areas for storage or depend on them to return a specific value if it is not stated in the Embedded Controller. Undefined registers and locations on this, or any other, part should be considered off limits and reserved for development systems, testing or future use.

2) Do not base timings loops on instruction execution times, as some instructions may execute faster on the 80C196 than on the 8096, even when the 80C196 is slowed down to 8 MHz, it's 8096 compatible rate. Counter-type loops should be initialized with values that can easily be changed at compile time.

3) Do not base critical timings on interrupt responses, A to D completions, flag settings, etc. This is for the same reason as above; some of these responses may be slightly different from those on the 8096. Timer 1 is provided for critical timings. With an 8 MHz crystal, it will increment every 2 microseconds, just as an 8096 running at 12 MHz.

4) The serial port baud register values should be easily changeable at compile time. Since the serial port is now capable of running at higher frequency, a different baud rate value will be needed.

5) The circuitry interfacing to the chip should be capable of interfacing to the 80C196. The I/O lines on 80C196 will look a lot like those on the 80C51.

6) The BHE#/WRH# signal in eight bit and write strobe mode will go low for odd byte transfers and high for even byte transfers. The WR#/WRL# signal will go low for odd byte transfers and high for even byte transfers. Normally, the WR#/WRL# signal will go low for odd byte transfers and high for even byte transfers. Normally, the WR#/WRL# signal should go low for odd and even byte transfers since transfers are on the low byte of the data bus.

7) PUSH and POP operations addressed relative to the stack pointer work differently on the 80C196 than on the 8096. On the 8096, the address is calculated based on the un-updated stack pointer value, on the 80C196, the address is calculated based on the updated value. The only operations effected are: PUSH xx[sp], PUSH [sp], PUSH sp, POP xx[sp], POP [sp],
POP sp.

8) The KB is pin compatible with the BH with one exception. Pin 64 (on the PGA package, pin 14 on the PLCC package) is V_{PD} on the BH. On the KB this pin is V_{SS}.

3. MEMORY MAP

ON-CHIP ROM/EPROM - The BH ROM and EPROM devices have 8K bytes of on-chip memory. The JF has 16K bytes. The KB has 8K bytes.

ON-CHIP RAM - The BH has 232 bytes of register RAM. The JF has 232 bytes of register RAM plus 256 bytes of executable internal RAM (code RAM). The KB has 232 bytes of register RAM.

RESERVED LOCATIONS - The KB uses some of the reserved locations to support new features.

WINDOW SELECT REGISTER - The Window Select Register on the KB expands the SFR space to support new features and makes the SFR's readable and writeable.

4. CCB

CCB BIT 0 - The KB uses bit 0 in the CCB to enable/disable Power Down mode. This bit is reserved on the BH.

5. INSTRUCTIONS

NEW INSTRUCTIONS - There are 6 new instructions on the KB:

1. PUSHA
2. POPA
3. IDLPD
4. CMPL
5. BMOV
6. DJNZW

EXECUTION TIMES - There are 3 oscillator periods per state on the BH. There are 2 oscillator periods per state on the KB. This decreases the instruction execution time. Also, many instructions on the KB require fewer states than on the BH. Timing loops based on instruction execution times should be recalculated for the KB.

FLAGS - The DIV and DIVB instructions leave the overflow flag undefined on the BH. The flag is set or cleared as appropriate on the KB.

6. STACK POINTER

OPERATIONS - RELATIVE TO THE STACK POINTER (SP) - For indexed and indirect operations relative to the stack pointer (SP), the address is calculated using the un-updated version of the stack pointer on the BH. The KB uses the updated version. The offset for POP[SP] and POPnn[SP] instructions may need to be changed by a count of 2.

7. INTERRUPTS

SHARED INTERRUPTS - On the BH, interrupt vector locations were shared for the RI and TI interrupts, HSI Data Available and HSI FIFO Full interrupts, EXTINT and ACH.7 interrupts, and Timer1 and Timer2 overflow interrupts. The KB supports this interrupt structure and also provides separate interrupts for each event, available under software control.

NEW INTERRUPTS - The KB supports the following new interrupts:

NMI
TRAP
Unimplemented Opcode
EXTINT1
Timer 2 Capture
HSI4 (4 or more entries in FIFO)

NMI - On the BH, NMI vectors directly to location 0000H. On the KB it vectors to location 203EH. To be compatible with the BH location 203EH must be loaded with 0000H.

NEW STATUS REGISTERS - The KB has INT_PEND1 and INT_MASK1 registers to support the new interrupts.

PRIORITIES - The original interrupts have the same relative priorities on the KB as on the BH. However, the new interrupts all have higher priority than the original interrupts.

PUSHA AND POPA - The KB has two new instructions, PUSHA and POPA, to save the PSW, INT_MASK, INT_MASK1, and WSR on the stack.

INSTRUCTIONS WHICH INHIBIT INTERRUPTS - On the BH the EI, DI, POPF, PUSHF, and SIGND instructions inhibit interrupts from being acknowledged until after the next instruction has been executed. On the KB the PUSHA, POPA, and TRAP instructions also do this.

INTERRUPT LATENCY - Maximum interrupt latency on the BH is 70 states. This includes 42 states for execution of the longest instruction (NORML) and 24 states for the response time. On the KB the interrupt response time is 61 states. This includes 39 states for the NORML instruction and 18 states for response time.

8. PWM

PWM PERIOD - The period of the PWM output is 256 states on the BH. On the KB the pulse width can be 256 states or 512 states, as selected in software.

READING THE PWM - The PWM register can be read on the KB in WSR 15.

PWM TIMINGS - The state times of the KB are shorter than the BH. For PWM outputs which require exact timings you may need to recalculate the PWM register value.

9. TIMER 1

TIMINGS BASED ON TIMER 1 - The state times on the KB are different than the BH. Any timings based on Timer 1 should be recalculated for the KB.

WRITING TO TIMER 1 - On the BH Timer 1 can be changed by writing to location 0CH. Writing any value to location 0CH will set the Timer 1 and Timer 2 to 0FFFXH. On the KB Timer 1 can be programmed by writing to location 0AH in WSR 15. This will set Timer 1 to the value written to 0AH.

10. TIMER 2

MAXIMUM TRANSITION SPEED - On the BH the maximum transition speed of inputs to Timer2 is once per eight state times. The maximum transition speed on the KB is once per eight state times in normal mode and once per state time in Fast Increment Mode.

COUNTING UP AND DOWN - Timer 2 on the BH only counts up. Timer 2 on the KB can count up or down.

T2 OVERFLOW INTERRUPTS - On both devices an overflow on Timer 2 can cause an interrupt. The KB can also interrupt when Timer2 crosses the 7FFFH/8000H boundary. An overflow interrupt vectors to location 2000H on the BH. On the KB a Timer 2 overflow interrupt can vector to location 2000H or 2038H, as selected in software.

TIMER 2 CAPTURE - On the KB the value in Timer 2 can be captured into the T2Capture register. A Timer2 Capture can generate an interrupt.

WRITING TO TIMER 2 - On the BH Timer 2 can be changed by writing to location 0CH. Writing any value to 0CH will set Timer 1 and Timer 2 to 0FFFXH. On the KB Timer 2 can be programmed by writing to location 0CH in WSR 0. This will set Timer 2 to the value written to 0CH.

11. HSI

INTERRUPTS - The BH can generate an interrupt when either the HSI Holding Register contains data or the FIFO contains 6 entries. Both interrupts vector to the same location. The KB, under software control, can vector to the same location for each or to separate locations. The KB can also generate an interrupt when the FIFO contains four entries.

READING AND WRITING THE CONTROL REGISTERS - The HSI_STATUS and HSI_TIME registers can be written to and IOC0 and IOC1 can be read in WSR 15 on the KB.

12. HSO

LOCKED CAM ENTRIES - HSO entries on the KB can be locked into the CAM. They will occur continually without having to reload the CAM.

CLEARING THE CAM - The entire HSO CAM can be cleared without resetting the device on the KB.

STATUS REGISTERS - Status registers on the BH show the current state of the HSO pins and which software timer has interrupted. In addition to these, a new status register is provided on the KB to show which HSO pins have transitioned, if a Timer2 reset has occurred, or if an A/D conversion has started.

READING AND WRITING THE CONTROL REGISTERS - IOS0, IOS1 and IOS2 can be written to and HSO_COMMAND, HSO_TIME and IOC1 and IOC2 can be read in WSR 15 on the KB.

13. SERIAL PORT

FLAGS - The KB has three new serial port flags:

FE - Framing Error Flag
TXE - Transmitter Empty Flag
OE - Receive Overflow Flag

SP_STAT - SP_STAT supports the new flags on the KB:

KB SP_STAT

7	6	5	4	3	2	1	0
RB8/ RPE	RI	TI	FE	TXE	OE	X	X

CLEARING THE FLAGS - On both devices, RI and TI are cleared every time SP_STAT is read. FE and OE are also cleared on the KB. On both devices RB8 is cleared after a transmission. On the KB TXE is also cleared after a transmission.

INTERRUPTS - On the BH the RI and TI interrupts both vector to the same location. The KB, under software control, can vector to the same location for each or to separate locations.

BAUD RATES - The formulas to calculate the baud rate are different on the BH and KB.

READING AND WRITING THE CONTROL REGISTERS - SP_STAT can be written and SP_CON can be read in WSR 15 on the KB.

14. A/D

CONVERSION TIMES - The BH takes 88 states to complete a conversion. This corresponds to 22us at 12MHz. Because the KB can operate over a wider frequency range, a prescalar can be enabled to adjust the speed of the A/D. The KB takes 91 states to complete a conversion with the prescalar off (22.75us at 8MHz) and 158 states with the prescalar on (26.33us at 12MHz, 19.75us at 16MHz).

SAMPLE WINDOW - The BH has a 4 state sample window. The KB has an 8 state time window with the prescalar off and 15 state sample window with the prescalar on.

15. EPROM PROGRAMMING

PROGRAMMING MODES - The KB does not support gang programming using a KB as the master programmer. The programming control signals needed for this mode do not exist on the KB.

PROGRAMMING SIGNALS - The PACT (programming active) signal is multiplexed with HSO.0 on the BH. It is multiplexed with P2.7 on the KB. The KB multiplexes P2.4 with AINC (auto increment signal). Auto increment does not exist on the BH.

PROGRAMMING PULSE WIDTH REGISTER - The KB has a Programming Pulse Width Register (PPW) to determine the width of the programming pulse in the Auto, Auto PCCB, and Run-time Programming Modes.

AUTO PROGRAMMING MODE - On the KB in the Auto Programming Mode, the PPW value must be loaded into external location 4014H before the Programming Mode is entered.

SLAVE PROGRAMMING MODE - On the BH in the Slave Programming Mode, the data verify or word dump command must be issued for each address. On the KB the AINC signal can be used to automatically increment the addresses without issuing another command.

RUN-TIME PROGRAMMING - On the BH using run-time programming, the programming pulse width must be programmed in software using a software timer. A "Jump to Self" loop is recommended during programming. On the KB, the PPW controls the programming pulse width. Idle Mode is recommended instead of the "Jump to Self".

ROM DUMP MODE - The ROM Dump Mode is entered the same way on the BH ROM and EPROM and on the KB EPROM. The KB ROM enters the mode differently. On the BH, ROM Dump Mode places indeterminate data at addresses 9000H-91FFH. No data is placed at these addresses on the KB.

SIGNATURE WORDS - The KB contains two words following the Signature Words which can be used to determine the programming voltage.

READ AND WRITE LOCK BITS - On the BH in the Auto, Auto PCCB, and Slave Programming Modes, if either the READ or the WRITE lock bits are programmed in the CCB the device cannot be programmed or verified. On the KB, if either bit is programmed, the device will do a security key verification. If the keys match, the device can be programmed and verified.

AC AND DC SPECS - The AC and DC EPROM Programming Characteristics are different for the BH and the KB. Consult the current Data Sheets for the specifications.

16. PINOUT/PIN FUNCTIONS

PIN COMPATIBILITY - The KB is pin compatible with the BH with one exception. Pin 64 (on the PGA package, pin 14 on the PLCC package) is V_{PD} on the BH. On the KB this pin is V_{SS}.

NEW PIN FUNCTIONS - Several pins have new additional functions on the KB. These pins are listed below.

BH pin/function	KB pin/function
P2.4/T2RST	P2.4/T2RST/AINC
P2.7/PACT	P2.7/PACT/T2CAPTURE
P2.6	P2.6/T2UP-DN
P1.7	P1.7/HOLD
P1.6	P1.6/HLDA
P1/5	P1.5/BREQ

17. MINIMUM HARDWARE CONSIDERATIONS

UNUSED PINS - All unused pins on the KB must be tied high or low. No pins - especially EA#, READY, BUSWIDTH, NMI, EXTINT, which do not have pullups or pulldowns - can be left floating.

VPP - V_{PP} must be left floating on BH EPROM devices. It must be tied to V_{CC} on all KB devices.

18. RESET

INTERNAL RESET TIMING - An internal reset on the BH (software reset or watchdog timer reset) will hold the RESET pin low for at least one state. On the KB, it will hold the RESET pin low for four states.

EXTERNAL RESET TIMING - To externally reset the BH the RESET pin must be held low for at least 10 XTAL1 cycles. The RESET pin must be held low for at least 4 states on the KB.

CAPACITOR ON RESET PIN - If a capacitor between RESET and VSS is used to reset the device, the recommended size of the capacitor is different for the KB.

STATUS DURING RESET - The status of the control registers and the I/O pins during RESET are different on the BH and the KB.

19. EXTERNAL MEMORY INTERFACING

AC TIMINGS - The AC Timings for bus operations are different for the BH and the KB. Consult the current Data Sheets for specifications. Both devices will function with standard ROM/EPROM/Peripheral type memory systems.

HOLD/HOLDA - The KB supports a bus exchange protocol (HOLD/HOLDA) to allow other devices to gain control of the bus.

20. MODES

ENTERING AND EXITING POWERDOWN - Powerdown is entered and exited differently on the BH and the KB.

RAM IN POWERDOWN - The BH maintains the upper 16 bytes of RAM in powerdown mode. The KB maintains all the SFR's, all 232 bytes of RAM, and most of the peripherals.

DISABLING POWERDOWN - Powerdown mode can be disabled on the KB.

NEW MODES - The KB has two new modes - Idle and ONCE modes.

21. POWER CONSUMPTION

POWER CONSUMPTION - Power consumption on the KB is about 1/10 that of the BH. See the current Data Sheets for the I_{CC}, I_{IDLE}, and I_{PD} specifications.

22. DC CHARACTERISTICS

DC SPECS - The DC characteristics on the BH are different than those of the KB. Consult the current Data Sheets for specifications.

23. BH, KB ERRATA

STATUS OF BH AND JF ERRATA ON THE KB - Listed below are the current BH and KB errata and their status on the KB. Consult the Data Sheets for more detailed information on current BH and KB errata.

BH ERRATA	BH STATUS	KB STATUS
Indexed, 3 Operand Multiply.	Displacement is incorrect.	Displacement is correct.
High speed input FIFO operation.	The FIFO must be cleared after any 7 consecutive entries or the 8th or 9th entry will be corrupted.	The FIFO does not need to be cleared. The 8th and 9th entries are not corrupted.
RESET and the quasibidirectional ports.	At RESET, the low impedance pullups may or may not turn on.	At RESET, the low impedance pullups never turn on.
Software RESET	The RESET pin will pull down for at least one state.	The RESET pin timing. will pull down for four states.
Using T2CLK as the source for Timer2	Timer2 may increment	Timer2 increments correctly.

and writing to IOC0.	incorrectly.	
Indexed, 3 Operand Multiply.	Displacement is incorrect.	Displacement is correct.
Software RESET timing.	The RESET pin will pull down for at least one state.	The RESET pin will pull down for four states.
High Speed Inputs.	The HSI resolution is 9 state times. Time-tags may be skipped. The first and second events may get different time-tags even if they occur within 9 states of each other.	Same as BH.

24. PACKAGES

AVAILABLE PACKAGES - Consult the current data sheets for availability of specific products in specific packages.

-90 Packages> P, LP, TP (no longer available)
BH Packages > A, C, N, P, U, LA, LC, LN, LP, TN (EOL in 1996)
JF Packages > N, U, TN (EOL in 1996)
KB Packages > N, S, TN

A= 68L PGA
C= 48L CERAMIC DIP
N= 68L PLCC
P= 48L PLASTIC DIP
S= 80L QUAD FLATPACK
U= 64L SHRINK DIP

PREFIX L=EXTENDED TEMPERATURE (-40 TO +85 DEGREES CELCIUS)
WITH 160+8 HR BURN IN
PREFIX T=EXTENDED TEMPERATURE (-40 TO +85 DEGREES CELCIUS)

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