87C196LB
SPECIFICATION UPDATE

Release Date: February, 1997
Order Number: 273002-001

The 87C196LB may contain design defects or errors known as errata. Characterized errata that may cause the 87C196LB's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-879-4683, Europe 44-0-1793-431-155,
France 44-0-1793-421-777, Germany 44-0-1793-421-333, other countries 708-296-9333

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REVISION HISTORY

Rev. Date	Version	Description
02/03/97	001	This is the new Specification Update Document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
87C196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual	272973-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 87C196LB product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	#	#	#			
001				8	No fix	J1850 Transmitter Stall Upon Bus Short

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES

IDENTIFICATION INFORMATION

Markings

87C196LB processors may be identified electrically according to device type and stepping. Refer to the data sheet for instructions on how to obtain the identifier number.

Product	Part Number	Stepping	Marking

ERRATA

1. J1850 Transmitter Stall Upon Bus Short

PROBLEM: Under certain fault conditions during the transmission of a J1850 message byte, it is possible that the J1850 transmitter state machine may stall resulting in immediate termination of a transmission in progress. Under this condition, further message transmissions from the J1850 module are prohibited until the transmit state machine is reset, either by outside message activity or the execution of a software workaround.

This problem is typically encountered when the J1850 module is transmitting and a bus short to either VSS or VCC occurs on the J1850 bus. A bus short is a fault condition, which under typical operation should not occur. An abrupt stall of the J1850 module during transmission of a message frame is typically seen as an error condition by other nodes on the network. External stimulation, such as reception of a message transmitted by another node, or the execution of the software workaround will reset the J1850 transmit state machine.

In the event of a j1850 transmitter stall, a software workaround may be executed in the absence of external stimuli to reset the J1850 transmit state machine. Execution of the workaround unlocks the J1850 transmitter from a stalled condition. The following workarounds must be executed to guarantee self recovery from a transmit state machine stall.

Case 1: Upon a transmit error (Bit 0, J1850_STAT register = 1).

1. Set the ABORT bit in J1850_CMD register; write data 10h.
2. Clear the ABORT bit in the J1850_CMD register; write data 00h.
3. Overflow the J1850_TX buffer; write same data (ex. 00h) three times to force Overflow condition.
4. Set the ABORT bit in the J1850_CMD register; write data 10h.

Case 2: Prior to a message transmission.

1. Set the ABORT bit in J1850_CMD register; write data 10h.
2. Clear the ABORT bit in the J1850_CMD register; write data 00h.
3. Overflow the J1850_TX buffer; write same data (ex. 00h) three times to force Overflow condition.
4. Set the ABORT bit in the J1850_CMD register; write data 1xh (where x is a non-zero value less than 8h.)

The two implementations of the software workaround are similar except for the last value written to the command register. The write to the J1850_CMD register does two things, setting of the ABORT bit and writing a value to the J1850 MSG bits. The value written to the J1850 MSG bits changes, as noted above, depending on the condition under which the workaround is implemented. This change is necessary to prevent extra “invalid symbols” from being transmitted on the J1850 bus. The above sequences of commands reset the J1850 transmit state machine and enable immediate transmission of a new message.

NOTE:

The three successive writes to the J1850_TX buffer will create an overflow condition and result in a J1850_STAT interrupt. The overflow interrupt occurs immediately after writing the third byte to the J1850_TX register, the user software must be prepared to handle overflow conditions as a result of executing the software workaround.

STATUS: No fix

SPECIFICATION CHANGES

001.

ISSUE:

002.

SPECIFICATION CLARIFICATIONS

001.

ISSUE:

002.

DOCUMENTATION CHANGES

001.

ITEM:

002.