8XC196KB AUTOMOTIVE APPLICATION SPECIFICATION UPDATE

Release Date: November, 1996
Order Number: 272970-001

The 8XC196KB may contain design defects or errors known as errata. Characterized errata that may cause the 8XC196KB's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-879-4683, Europe 44-0-1793-431-155,
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REVISION HISTORY

Rev. Date	Version	Description
11/13/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
80C196KB User's Guide	270651
8XC196KB Advanced 16-bit CHMOS Microcontroller — Automotive	270679
8XC196KB/KC/KD Programming Support Fact Sheet	272225
Development Tools Handbook	272326

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC196KB product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata - Part I

Number	Steppings									Status
	A-0	B-3	A-2	A-0	B-0	C-0	C-1[1]	C-1	C-1	
Product	8EC196KA	8EC196KB	87C196KB	83C196KB	83C196KB	87C196KBS	83C196KBS	87C196KBS	83C196KBS	
9600001	X									Fixed
9600002	X									Fixed
9600003	X									Fixed
9600004	X									Fixed
9600005	X									Fixed
9600006	X	X	X	X						Fixed
9600007	X	X	X	X	X					Fixed
9600008	X	X	X	X	X	X	X	X	X	NoFix
9600009		X	X	X						Fixed
9600010		X	X	X	X					Fixed
9600011		X	X	X	X					Fixed
9600012		X								Fixed
9600013		X	X	X						Fixed
9600014		X	X	X	X					Fixed
9600015		X	X	X						Fixed
9600016	X	X	X	X	X	X	X	X	X	NoFix
9600017	X	X	X	X	X					Fixed
9600018	X	X	X	X	X	X	X	X	X	NoFix
9600019						X	X	X	X	NoFix
9600020	X	X	X	X	X	X	X	X	X	NoFix
9600021	X	X	X	X	X	X	X	X	X	NoFix

1. This 83C196KBS (C-1) is on the EPROM (P629.0) process

Errata - Part II

Number	Page	Errata
9600001	15	BYTE Shifts
9600002	15	DIVU and DIVUB
9600003	15	PUSHA with External Stack
9600004	16	RESET# Rise Time
9600005	16	HOLD#/HLDA# Not Available
9600006	16	IPD
9600007	16	Divide With HOLD# or READY
9600008	17	HSI Errata
9600009	17	SIO Baud Rate Tolerance
9600010	18	SIO Framing Error Flag
9600011	18	SIO RI Flag
9600012	18	HOLD#/HLDA#
9600013	19	RESET# Hysteresis
9600014	19	DJNZW
9600015	19	Interrupts After Jumps
9600016	20	CMPL with R0
9600017	21	ALE Glitch
9600018	22	SIO Mode 0 Maximum Baud Rate
9600019	23	Missing External Interrupt Request (EXTINT, EXTINT1, NMI)
9600020	25	HSI Events (9 or more)
9600021	27	Writing HSI_Mode Resets the Divide-by-Eight Counter

Specification Changes - Part I

Number	Steppings									Status
	A-0	B-3	A-2	A-0	B-0	C-0	C-1[1]	C-1	C-1	
Product	8EC196KA	8EC196KB	87C196KB	83C196KB	83C196KB	87C196KBS	83C196KBS	87C196KBS	83C196KBS	
001	X					X	X	X	X	Doc

1. This 83C196KBS (C-1) is on the EPROM (P629.0) process

Specification Changes - Part II

Number	Page	Specification Change
001	28	I_{TL} Specification Changed to -800 µA (from -650 µA)
002	29	T_{VDXH} Specification Changed to T_{OSC} + 60 (from T_{OSC} + 50)

Specification Clarifications - Part I

Number	Steppings									Status
	A-0	B-3	A-2	A-0	B-0	C-0	C-1[1]	C-1	C-1	
Product	8EC196KA	8EC196KB	87C196KB	83C196KB	83C196KB	87C196KBS	83C196KBS	87C196KBS	83C196KBS	
001						X	X	X	X	Doc
002						X	X	X	X	Doc

1. This 83C196KBS (C-1) is on the EPROM (P629.0) process

Specification Clarifications - Part II

Number	Page	Specification Change
001	30	Improved System Reset Circuit

Documentation Changes

Number	Document Revision	Page	Status	Documentation Change
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

See table.

Stepping Register

Product Name (1)	Step	Process	Top Side Mark (2)	MHz	Change Indicator (3)	Status
8EC196KA	A-0	P645	80C197 QDF or S-spec number		N/A	End of lifed
8EC196KB	B-3	P645	80C196KB QDF or S-spec number		N/A	End of lifed

NOTES:

1. All products currently offered are available in PLCC (indicated by “N” prefix), extended temperature PLCC (indicated by “TN” prefix), and QFP (indicated by “S” prefix) packages.
2. The “Rn” after a part number indicates a ROM code. The “n” is the ROM code number. The frequency of the ROM devices with the “Rn” can only be determined by the ROM or spec documentation.
3. The change indicator is the last character in the FPO number. The FPO number is on the second line on the top side of the device.

Stepping Register (Continued)

Product Name (1)	Step	Process	Top Side Mark (2)	MHz	Change Indicator (3)	Status
87C196KB	A-2	P624	87C196KB10 87C196KB12	10 12	B	End of lifed
83C196KB	A-0	P645	80C194 83C194, Rn 80C198 83C198,Rn 80C196KB10 80C196KB12 83C196KB10 83C196KB12	12 12 12 12 10 12 10 12	N/A	End of lifed
83C196KB	B-0	P645	80C194 83C194,Rn 80C198 83C198,Rn 80C196KB10,Rn 83C196KB12,Rn	12 12 12 12 10 12	B	Full Production
87C196KBS	C-0	P629.0	87C198-16 87C196KB 87C196KB16	16 12 16	E	Full Production

NOTES:

1. All products currently offered are available in PLCC (indicated by “N” prefix), extended temperature PLCC (indicated by “TN” prefix), and QFP (indicated by “S” prefix) packages.
2. The “Rn” after a part number indicates a ROM code. The “n” is the ROM code number. The frequency of the ROM devices with the “Rn” can only be determined by the ROM or spec documentation.
3. The change indicator is the last character in the FPO number. The FPO number is on the second line on the top side of the device.

Stepping Register (Continued)

Product Name (1)	Step	Process	Top Side Mark (2)	MHz	Change Indicator (3)	Status
83C196KBS	C-1	P629.0	80C198 83C198,Rn 80C196KB 80C196KB16 83C196KB,Rn	16 12,16 12 16 12,16	F	EPROM die. Used for CPU or factory programmed ROM. Only used in constrained situations.
87C196KBS	C-1	P629.0	87C198 87C196KB 87C196KB16	16 12 16	F	Full Production
83C196KBS	C-1	P629.1	80C198 83C198,Rn 80C196KB 80C196KB16 83C196KB,Rn 83C196KB16,Rn	16 12,16 12 16 12,16 16	G	Full Production

NOTES:

1. All products currently offered are available in PLCC (indicated by “N” prefix), extended temperature PLCC (indicated by “TN” prefix), and QFP (indicated by “S” prefix) packages.
2. The “Rn” after a part number indicates a ROM code. The “n” is the ROM code number. The frequency of the ROM devices with the “Rn” can only be determined by the ROM or spec documentation.
3. The change indicator is the last character in the FPO number. The FPO number is on the second line on the top side of the device.

ERRATA

9600001. BYTE Shifts

PROBLEM: Byte shifts do not work if performed on an odd-location register. Register retains same value after shift.

IMPLICATION: Any customer using byte shifts in their code will be affected. The effect is wasted register file space.

WORKAROUND: Locate byte-wide registers on even boundaries.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600002. DIVU and DIVUB

PROBLEM: The unsigned divide operations may result in a quotient that is one count larger than the correct value if the most significant bit of the divisor is a one. Any calculation involving an unsigned divide is slightly off.

IMPLICATION: Any customer using the unsigned divides will be affected. Extra code is required.

WORKAROUND: Decrement quotient by one if the most-significant bit of the divisor is a one.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600003. PUSHA with External Stack

PROBLEM: When the PUSHA instruction is used with an external stack, the data will be written into the location pointed to by the lower byte of the stack. This can corrupt the register file.

IMPLICATION: Any customer using PUSHA to external memory will affected. The effect is limited stack space.

WORKAROUND: Set the lower byte of the stack pointer to a much higher value than the highest register location.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600004. RESET# Rise Time

PROBLEM: The RESET# pin must have a rise time of less than 4 states. Slower rise times can prevent proper initialization.

IMPLICATION: Any customer who has a slow rise time on the RESET# pin will be affected. External hardware is required to generate a reset.

WORKAROUND: Use a Schmitt trigger on the RESET# pin.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600005. HOLD#/HLDA# Not Available

PROBLEM: The HOLD#/HLDA# function is not yet available.

IMPLICATION: This impacts the 8EC196KA.

WORKAROUND: Not applicable.

STATUS: Fixed. HOLD#/HLDA# has been made available in subsequent versions.

9600006. IPD

PROBLEM: IPD is not specified.

IMPLICATION: Applies to 8EC196KA, 8EC196KB, 87C196KB, 83C196KB, and 87C196KBS devices.

WORKAROUND: Not applicable.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600007. Divide With HOLD# or READY

PROBLEM: If an unsigned divide instruction (word or byte) is in the queue when HOLD# or READY is asserted, the mathematical result may be incorrect.

IMPLICATION: Any customer using an unsigned divide instruction along with HOLD# or READY on a B-step 87C196KB will be affected. The workaround requires extra code that results in slower response from peripherals.

WORKAROUND: Disable HOLD# before every divide and enable it after the divide is complete. For applications using READY, limit wait states by programming bits 4 and 5 of the CCR.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600008. HSI Errata

PROBLEM:

This problem takes two forms:

1. The maximum event rate is once per nine states instead of eight states. Every nine states an event can be captured. The mismatch between the nine-state resolution and the eight-state hardware timer causes one time tag to be skipped every nine timer counts. Events may receive a time tag one timer count later than expected.
2. The first two events into the FIFO may also receive time tags that are one timer count apart even if the two events occur within a nine-state window of each other.

Events occurring on the same pin more frequently than once every nine states may be lost.

IMPLICATION: Any customer using the HSI will be affected. Since these errata can only be found when the HSI is pushed to the limit, they should not cause problems for most customers.

WORKAROUND: Allow at least nine state times between consecutive events on each pin.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600009. SIO Baud Rate Tolerance

PROBLEM: The serial port baud error tolerated between the transmitter and receiver is +1.25% through -7.5% (instead of ± 5.0%). If the baud rate error exceeds this tolerance, the serial port receiver will not function.

IMPLICATION: Any customer using the receiver will be affected. Requires code modification to get the correct baud rate.

WORKAROUND: If the serial port fails on the receiver, increase the baud rate by 2% to 3%.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600010. SIO Framing Error Flag

PROBLEM: The stop bit in a normal receive frame is a ‘1’. If a ‘0’ is received instead of an expected stop bit, the serial port should recognize the ‘0’ as a framing error and set the framing error flag.

An error occurs when the last data bit preceding a stop bit is a ‘1’ and the RXD line glitches low, causing an erroneous ‘0’ stop bit. When this occurs, the receiver interprets the erroneous ‘0’ stop bit as the first data bit for the next frame, corrupting the next frame.

IMPLICATION: Any customer using the serial port will be affected.

WORKAROUND:

1. Use 8-bit mode with parity disabled, and use the 7-bit ASCII character set.
2. Use 9-bit mode, and set the 9th data bit to '0'.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600011. SIO RI Flag

PROBLEM: The RI flag is not generated after the first byte is received. The serial port cannot receive another byte.

IMPLICATION: Any customer using the serial port will be affected.

WORKAROUND: Reload baud rate register after each reception.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600012. HOLD#/HLDA#

PROBLEM: If a branch instruction is prefetched into the queue while HOLD# is asserted, the microcontroller fetches from the same address twice when it comes out of hold.

IMPLICATION: Any customer using the HOLD#/HLDA# protocol for external memory systems will be affected. External peripherals cannot take control of the bus.

WORKAROUND: Disable HOLD#/HLDA# before a branch instruction and enable it after.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600013. RESET# Hysteresis

PROBLEM: RESET# hysteresis is not specified. The RESET# pin must have a rise time of less than 4 states. Slower rise times can cause lockup and failure to execute the power-on startup sequence properly.

IMPLICATION: Any customer with a slow time on the RESET# signal will be affected. Additional hardware may be required to generate a reset.

WORKAROUND: Use a Schmitt trigger on the RESET# pin.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600014. DJNZW

PROBLEM: The DJNZW (decrement and jump if not zero word) instruction does not work. Loops that use DJNZW will not work.

IMPLICATION: Any customer using the DJNZW instruction will be affected.

WORKAROUND: Use DJNZ (byte) and use nested loops to attain word resolution.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600015. Interrupts After Jumps

PROBLEM: Interrupts do not occur between a conditional jump not taken and the next instruction. This results in increased interrupt latency.

IMPLICATION: Increased interrupt latency.

WORKAROUND: None.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600016. CMPL with R0

PROBLEM: Using the CMPL (compare long) instruction with the zero register (R0) is not guaranteed to provide accurate results. R0 is a word register, and the AD_COMMAND

and HSI_MODE registers occupy the word above R0. When CMPL addresses R0 as a double-word, the microcontroller reads R0 as the low word and AD_COMMAND and HSI_MODE as the high word. If AD_COMMAND and HSI_MODE contain values other than zero, incorrect flags will be set.

IMPLICATION: Any customer using CMPL with R0 will be affected. Customers must initialize a double-word register in memory.

WORKAROUND: Do not use R0 for CMPL instructions. Instead, use a double-word register that is initialized to zero.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600017. ALE Glitch

PROBLEM: Due to the internal grounding scheme of the P645 device, it is possible in certain application-specific conditions for a glitch to occur on the ALE signal. The glitch on ALE occurs after the correct address is latched externally with ALE. Therefore the glitch can be large enough to re-latch an incorrect address externally during a write cycle.

IMPLICATION: Any customer using ALE signal who has heavy bus loading in their system will be affected. The glitch becomes worse at cold temperatures.

A wrong address can be latched externally during a write cycle, so data can be lost.

WORKAROUND: Workarounds are dependent on the application. Some suggestions are as follows:

- Place a resistor, capacitor, or resistor-capacitor filter on the ALE line to reduce the glitch. In our bench experiments, several things were tried.

  A 100-pF capacitor was placed on the ALE line; however, in our bench set-up, the ALE waveform was significantly degraded. This capacitor fix may work in some applications, but the placement and size of the capacitor depends on the board capacitance and inductance. This workaround should be thoroughly analyzed in the specific application.

  Next, a series resistance of 47 ohms was placed on the ALE signal at the device. This fix lowered the glitch amplitude by approximately 45%. This appeared to be the preferred fix for our bench set-up.

  Finally, an RC filter was placed at the ALE pin (R=47 ohms, C=20 pF, time constant = ~1 ns). This reduced the glitch amplitude by approximately 50%. The RC filter fix, like the others, should be analyzed for the specific application, since the timing of the ALE glitch is critical.

These fixes worked for the bench set-up, but customers must analyze their systems to see if the capacitor, resistor, or resistor-capacitor fixes will work in their applications. Not only does this type of fix need to limit the amplitude of the glitch so that the address latch does not erroneously recognize a 0-to-1 transition, but also it must ensure that the ALE signal meets the timing requirements of the specific application.

- Place resistors on the address/data bus pins to limit the current at the time of discharge from the load. An analysis of the system should be made to see if this fix will degrade the response time of the address/data bus signals.
- Use a slower, CMOS input-level latch that cannot be clocked by the ALE glitch. Some suggestions are to use an AC or HC latch. TTL-level latches should be avoided in systems using the ALE glitch-prone device in a system with heavy address/data bus loading.
- Use separate ground and power planes in the board design to reduce the resistance/inductance on the ground connections of the microcontroller to the system ground.
- Use a CMOS inverter/buffer on ALE that will not switch on the ALE glitch and provide 'clean' ALE signal. Possibly a Schmitt trigger would provide the response needed for the ALE signal, while eliminating the spike.
- Avoid writes to high address locations (i.e., FF00-FFFF) where numerous address/data signals will be switching at one time. Software modifications and hardware address decoding will be necessary, but the probability of seeing the glitch is reduced.
- Consider converting to the process 629 8XC196KB product, which has the ALE pin and the address/data bus on different ground buses. Also the process 629 8XC196KB's internal grounding scheme has more localized ground points. Therefore, the ground bounce is not seen on the ALE signal.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600018. SIO Mode 0 Maximum Baud Rate

PROBLEM: In synchronous mode 0, the minimum baud value is 0001H for transmissions and 0002H for receptions.

In asynchronous modes 1, 2, and 3, the minimum baud value is 0000H when using the internal clock signal and 0001H when using an external clock signal on T2CLK. At 16 MHz, the maximum baud rate is 2.76 Mbaud for mode 0 and 1.0 Mbaud for modes 1, 2, and 3.

Bits 14:0 of the BAUD_RATE register specify the baud value. (Bit 15 selects either the internal clock signal or an external clock signal on T2CLK.) Using a value less than the minimums listed above results in incorrect data. For mode 0 receptions, whatever data is present on the RXD pin when TXD begins clocking is treated as the least-significant bit, each remaining bit is shifted left by one bit, and the most-significant bit from the transmitter is never shifted in.

IMPLICATION: Any customer who uses synchronous mode 0 will be affected. Use a baud value that is equal to or greater than the minimum value listed above. This will result in slower baud rates, but should result in correct data.

WORKAROUND: None. Use a baud value that is equal to or greater than the minimum value:

- for synchronous mode 0, 0002H for receptions or 0001H for transmissions
- for asynchronous modes 1, 2, and 3, 0001H when using an external clock source or 0000H when using the internal clock signal

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600019. Missing External Interrupt Request (EXTINT, EXTINT1, NMI)

PROBLEM: At low voltages and at high frequencies, it is possible to miss an interrupt occurrence on P0.7. The internal signal driver for P0.7 to the interrupt pending register was not strong enough to set the interrupt pending bit in certain conditions. The missed interrupt occurs at low Vcc and high frequency. The missed interrupt can occur in a window around the falling edge of CLKOUT.

On the B-stepping, the edge-triggered external interrupt EXTINT using P0.7 as the input source has been found to miss interrupts under certain conditions. The missed interrupts occur at high frequencies (greater than 16Mhz) and low voltages (less than 4.7V.) At voltages below spec, 3.1V and 16MHz, missed interrupts were discovered on EXTINT/P0.7, EXTINT1/P2.2, and NMI. Higher temperatures slightly increased the occurrence of the missed interrupts. Missed interrupts have not been seen on HSI.0 or T2CAPTURE. Investigation of the problem has shown that the edge-detect circuit that generates a single state pulse to the interrupt unit does not have enough drive to generate the proper signal at the interrupt unit to set the interrupt pending bit. The driver on P0.7 was found to be about 1/2 the size of the NMI driver, which explains the P0.7 failures occurring at voltages within the normal operating range. The driver on P2.2 is only slightly smaller than the NMI driver, which explains why failures were not seen on P2.2 in the normal operating range.

When an interrupt occurs on the EXTINT pin, an internal interrupt signal generates a request to the interrupt unit. The interrupt unit then sets the corresponding interrupt pending bit. The internal interrupt signal must meet a minimum pulse width to set the interrupt pending bit. If the external interrupt occurs in a window of time around the falling edge of CLKOUT, the internal interrupt signal is shortened. The shortened pulse cannot drive the interrupt unit to set the interrupt pending bit. At lower voltage and higher frequency, the driver of the internal interrupt signal can deactivate before the interrupt pending bit is set.

The missed interrupts occur most often at high frequencies, low voltages, and higher temperatures. Testing for the problem was done by skewing a positive pulse edge across the period of a CLKOUT signal and varying the voltage.

The missed interrupt occurred only during a window of time just after the falling edge of CLKOUT. On an 80C196KD at 3.0V, 25 MHz, and room temperature, the window was as large as 2 ns. The voltage was then increased in 0.1V increments. The size of the window decreased to about 1.8 ns, and the window position at which the interrupts are missed moved about 1 ns further from the falling edge of CLKOUT. This procedure was continued until missed interrupts were no longer observed. As the voltage got near 4.0V, the rate of missed interrupts was about 1 in 150,000 events on P0.7 when all the events were concentrated on a 0.1 ns window. Table 1 lists the voltages and frequencies at which problems were observed on the various products at room temperature.

Interrupt Pin	Voltage	Frequency	Device
P0.7 / EXTINT	2.9V - 4.6V	16 MHz	8XC196KB
	3.0V - 4.5V	20 MHz	8XC196KD
	2.9V - 4.4V †	20 MHz	8XC196KC
P2.2 / EXTINT1	2.9V - 4.1V †	20 MHz	8XC196KD
	2.9V - 3.7V †	20 MHz	8XC196KD
NMI	2.9V - 3.5V †	20 MHz	8XC196KD

† Outside specified operating range.

NOTE:

8XC196KB and 8XC196KD are the only devices that exhibit this failure in the normal operating range on the listed steppings.

IMPLICATION: Some missed interrupts were seen in the normal operating region of the device. Therefore, customers using P0.7 for EXTINT may be affected.

On the B-stepping, any application using the P0.7/EXTINT interrupt source at low voltages (less than 4.7V) and high frequencies (greater than 16MHz) should synchronize the interrupt signal to the rising edge of CLKOUT or, if possible, add software to ensure the servicing of the interrupt.

WORKAROUND: Add a latch that synchronizes the interrupt with the rising edge of CLKOUT. Software can be added to monitor P0.7 and check whether the interrupt pending bit is set when a transition occurs on P0.7.

Device Design Fixes: On the B step of the 8XC196KD products, different fixes were implemented in different devices. The following is a history of the fixes implemented.

83C196KD:	Buffer Driver Size Increased; errata still marginally exists just out of range of normal operating conditions.
87C196KD:	Buffer Driver Size Increased and Latch Added; errata fixed.

On the B-stepping, synchronizing the input signal to the rising edge of CLKOUT with a flip-flop will prevent an asynchronous signal from occurring in the window near the falling edge of CLKOUT. Software could also detect a missed interrupt by periodically checking whether the external interrupt signal is high at the port pin and the interrupt pending bit is low. If the level of the EXTINT pin has changed, the routine could then set the interrupt pending bit, thus causing an interrupt. This assumes the interrupt signal will remain high until the external interrupt routine acknowledges the interrupt.

P0.7/EXTINT has been found to miss interrupts when operating at voltages less than 4.7V and frequencies greater than 16 MHz. During a window near the falling edge of CLKOUT at the above operating conditions, the edge-detect circuitry fails to recognize and set the interrupt pending bit.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600023. HSI Events (9 or more)

PROBLEM: The HSI FIFO can hold seven events/times, and the holding register can hold an additional event/time, for a total of eight events/times. Reading the HSI_STATUS and HSI_TIME registers unloads the holding register, allowing the next event/time to move from the FIFO into the holding register.

An error occurs if a ninth event occurs while the FIFO and holding register are full. This ninth event sets an internal HSI event latch. When software unloads the first event from the holding register (by reading HSI_STATUS and HSI_TIME), the second event moves

into the holding register and the third through eighth events move down one position in the FIFO, leaving a vacancy in the FIFO. Because the internal HSI event latch is set, the ninth event moves into the FIFO. However, the ninth event has no time tag associated with it. A time tag is created at the time the event moves into the FIFO, and the FIFO_FULL and HSI_RDY bits of the IOS1 register reflect the event, so it **appears** that a valid ninth event occurred.

The FIFO_FULL bit, when set, indicates that the FIFO contains six or more events. The HSI_RDY bit, when set, indicates that the holding register contains one event. The following table summarizes the status of the FIFO_FULL and HSI_RDY bits after a series of eight events and after a series of nine events:

Event from FIFO	FIFO_FULL (9 events)	FIFO_FULL (8 events)	HSI_RDY (9 events)	HSI_RDY (8 events)
1	1	1	1	1
2	1	1	1	1
3	1	0	1	1
4	0	0	1	1
5	0	0	1	1
6	0	0	1	1
7	0	0	1	1
8	0	0	1	1
9	0	0	1	0

In summary, the HSI can correctly record only eight events. However, if a ninth event occurs while the FIFO and holding register are both full, the HSI module and the related status bits (FIFO_FULL and HSI_RDY) behave as though nine events were recorded.

IMPLICATION: Any customer using the HSI unit will be affected. Applications should be analyzed to ensure that nine events cannot occur before at least one event is unloaded from the holding register.

WORKAROUND: Analyze the application to ensure that nine events cannot occur before at least one event is unloaded from the holding register. The HSI unit can record an event every 9 state times. The maximum interrupt latency is 56 state times. Using this data, determine how frequently events can occur, and which interrupt should be used (HSI FIFO Full, HSI FIFO Fourth Entry, or HSI Data Available).

The following code can be used to ensure the FIFO is empty before setting up for an HSI event:

```
flush:ld 0, hsi_time            ; clear event
      skip 0                    ; delay 3 state times
      skip 0                    ; delay 3 state times
      skip 0                    ; delay 3 state times
      jbs ios1, 7, flush        ; repeat until HSI_RDY bit is clear
                                ; (the holding register is empty)
```

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600024. Writing HSI_Mode Resets the Divide-by-Eight Counter

PROBLEM: Writing to the HSI_MODE register always resets the HSI module's divide-by-eight counter.

If you write HSI_MODE to configure an HSI, and another HSI was previously configured for "eight positive transitions" mode, the counter reset causes the previously configured HSI to lose up to seven accumulated events.

IMPLICATION: Applications that write to HSI_MODE after an HSI is configured for "eight positive transitions" mode will be affected.

WORKAROUND: There are three possible workarounds:

If any HSI is to be used in "eight positive transitions" mode, use a single write to HSI_MODE to configure all HSI inputs at once.

Disable the HSI input by clearing the associated bit(s) the IOC0 register, poll the HSI_STATUS register until seven counts have occurred, then enable the HSI to load the FIFO on the eighth transition.

Configure the HSI for "every transition" mode, and use an external counter to pass through the eighth transition.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

001. I_{TL} Specification Changed to -800 µA (from -650 µA)

PROBLEM: The specification for I_{TL} on the 8XC198 and 8XC196KB/8XC196KB16 devices has changed from -650 µA to -800 µA to meet the device characteristics at low temperatures.

The I_{TL} specification is the maximum current that the 8XC196KB quasi-bidirectional pins can source during the transition from a logic 1 to a logic 0 input. Figure 1 shows the quasi-bidirectional port circuit. When the port is configured as an input, the output of the port latch is a '0'. Therefore, Q3 is weakly pulling the port pin high. When the external circuitry drives the pin high, Q4 also is turned on and holds the port pin signal high. As the external circuitry decreases the voltage below V_{CC} toward logic 0, Q4 begins to turn off. However, due to transistor characteristics, Q4 will source increasing amounts of current until the threshold voltage of the transistor is reached. Then, Q4 will turn off, leaving only Q3 driving the port pin signal high.

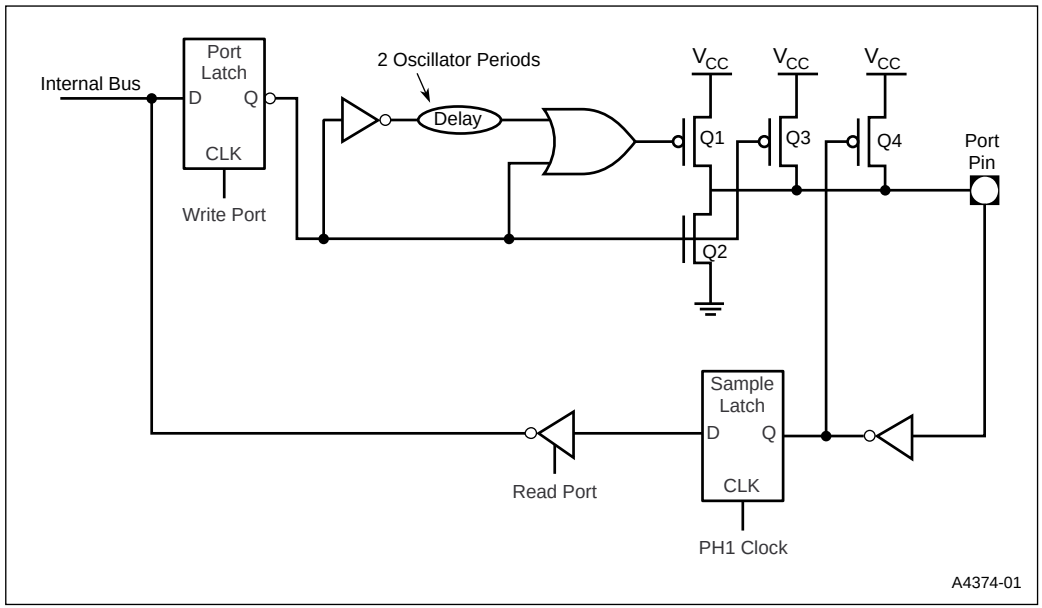

Figure 1. Quasi-bidirectional Port Circuit

Figure 2 shows the transfer characteristic of the port pin during the input's transition from logic 1 to logic 0. The I_{IL} specification shows the amount of current Q3 will source after Q4 turns off. The I_{TL} specification gives the maximum amount of current that Q4 will source during the input's transition from logic 1 to logic 0.

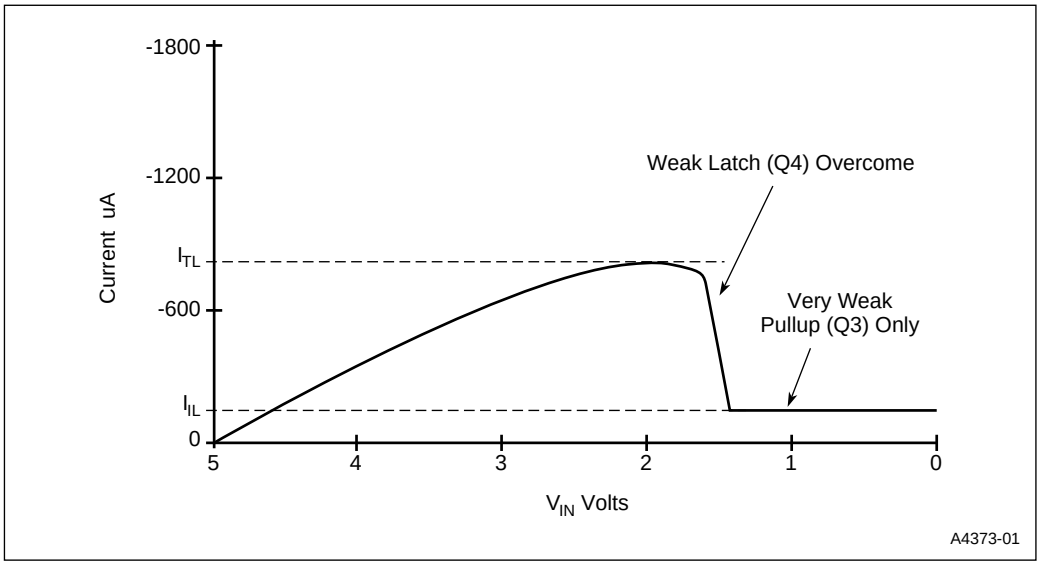

Figure 2. Quasi-bidirectional Port DC Characteristics ("1" Written to Port Pin)

IMPLICATION: Customers using the quasi-bidirectional pins as input should analyze their applications to see if their external circuitry can handle 80 µA of current from the quasi-bidirectional pins during the transition period described above.

002. T_{VDXH} Specification Changed to T_{OSC} + 60 (from T_{OSC} + 50)

PROBLEM: The specification for T_{VDXH} (input data setup to clock rising edge) has changed to T_{OSC} + 60 ns.

SPECIFICATION CLARIFICATIONS

001. Improved System Reset Circuit

PROBLEM: The following improved system reset circuit shown in Figure 3 may be used in conjunction with the *80C196KB User's Guide* (270651-003).

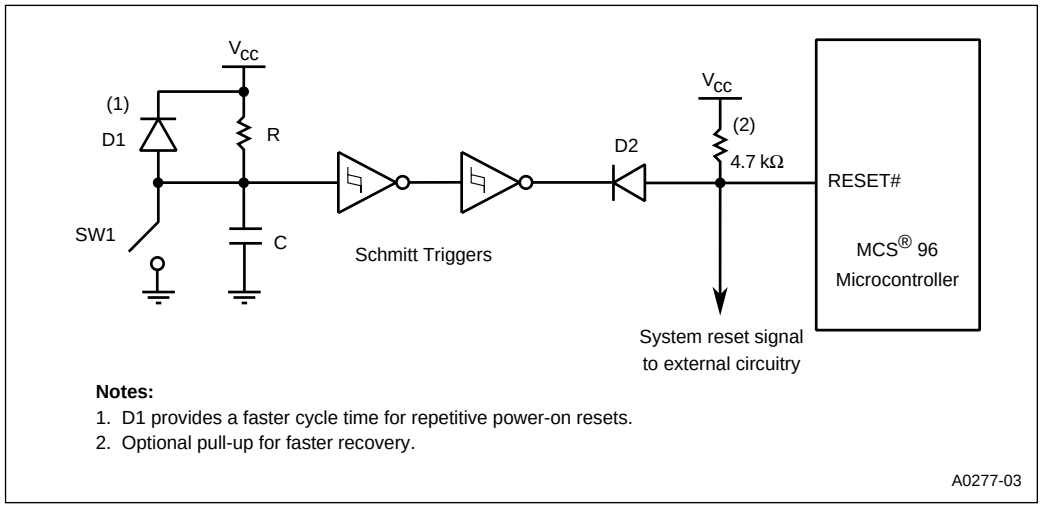

Figure 3. Improved System Reset Circuit

The system reset circuit in the *80C196KB User's Guide* has been used successfully by many customers for a long period of time. Both circuits should be evaluated in the user's system.

The main difference between the two circuits is the addition of a 4.7 KΩ pull-up resistor. In some systems, the internal pull-up resistor on the RESET# pin is not sufficient, resulting in a slow rise time. Therefore, the external pull-up resistor was added to allow a more predictable rise time on the RESET# input. The external pull-up resistor is optional, but it may help ensure a clean reset, either for the 8XC196KB or for the external system.

The improved system reset circuit will be included in the next revision of the *80C196KB User's Guide*.

DOCUMENTATION CHANGES

None for this revision of this specification update.