83C196EA
SPECIFICATION UPDATE

Release Date: July, 1996

Order Number: 272872-001

The 83C196EA may contain design defects or errors known as errata. Characterized errata that may cause the 83C196EA's behavior to deviate from published specifications are documented in this specification update.

CONTENTS

REVISION HISTORY 1

PREFACE 2

SUMMARY TABLE OF CHANGES 4

IDENTIFICATION INFORMATION 7

ERRATA 8

SPECIFICATION CHANGES 14

SPECIFICATION CLARIFICATIONS 14

DOCUMENTATION CHANGES 14

REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 83C196EA Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
83C196EA CHMOS 16-Bit Microcontroller datasheet (Automotive)	272788-001
83C196EA Microcontroller User's Manual	272804-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes,specification clarifications, or documentation changes which apply to the 83C196EA product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A	#	#			
9600001	X			8	Fix	Incorrect A/D Channels Converted
9600002	X			9	Fix	P5.4 Pullup Not Disabled During ONCE Mode (I/O three-state)
9600003	X			9	Fix	AD Scan Mode Does Not Function
9600004	X			9	Fix	A/D Inaccuracy
9600005	X			10	Fix	Serial Port Default Baud Rate 4800 Baud in Test ROM Mode
9600006	X			10	Fix	PTS Block Move
9600007	X			11	Fix	TIJMP / PIH Missed Interrupts
9600008	X			11	Fix	On-Chip RISM “next” Commands
9600009	X			11	Fix	SDU Interrupt on Branch with Wait States
9600010	X			12	Fix	WR# Active Low on Falling Edge of ALE
9600011	X			12	Fix	P2.6 Pullup
9600012	X			12	Fix	Emulator CLKE Pin Inactive During Reset
9600013	X			13	Fix	Emulator Peripheral Interrupt Handler Conflict
9600014	X			13	Fix	Emulator Missed Data Match
9600015	X			13	Fix	READY# Function Not Enabled in ICE Mode

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	A#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

Bottom mark: AS83C196EA

ERRATA

9600001. Incorrect A/D Channels Converted

PROBLEM: Bits 0 and 1 and bits 2 and 3 of the A/D channel decoder were incorrectly swapped. This causes a different channel than expected to be converted. For example, writing the A/D command register bits ACH3-ACH0 with 0001B will cause channel 2 to be converted instead of the expected channel 1.

IMPLICATION: Mapping of A/D channels differs from intended design.

WORKAROUND: . Use the table below to find what value written to the A/D command register corresponds to the desired actual channel conversion.

	A-Step	B-Step
Write A/D Command Register (ACH3-ACH0)	Converts Channel/Pin	
0	0	0
1	2	1
2	1	2
3	3	3
4	8	4
5	10	5
6	9	6
7	11	7
8	4	8
9	6	9
10	5	10
11	7	11
12	12	12
13	14	13
14	13	14
15	15	15

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600002. P5.4 Pullup Not Disabled During ONCE Mode (I/O three-state)

PROBLEM: During ONCE mode, P5.4 is actively pulled up. ONCE mode is used to electrically isolate the component during testing or programming of other devices connected to an application (most often external EPROM or flash memories).

IMPLICATION: Any device that expects P5.4 to be three-stated in ONCE mode will instead see a logic '1' driven on P5.4. Since P5.4 is typically not used for interfacing to external memories, this erratum is not expected to impact the intended usage of ONCE mode.

WORKAROUND: If this pin needs to be three-stated during ONCE mode, the user must supply an isolation buffer/device.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600003. AD Scan Mode Will Function on the B-step

PROBLEM: A-step scanning could get stuck on one channel for some V_{cc}/Temp conditions.

IMPLICATION: A/D scan mode is not useable.

WORKAROUND: Use an interrupt service routine to read a channel result and start an A/D conversion on the next desired channel.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600004. A/D Inaccuracy

PROBLEM: The analog-to-digital converter on the 83C196EA is a successive approximation type. There is a resistor ladder with 255 taps that are used to directly generate the first 8 bits of the conversion. A capacitive voltage divider is used with the resistor ladder to generate the two LSBs. The upper 8 bits of the result directly address the ladder; the lower two bits select another ladder tap, which is capacitively summed with the tap selected by the upper 8 bits.

As a conversion starts, the result register is loaded with 10 0000 0000b**.** This selects the middle tap of the ladder. A binary search is then performed to find the voltage that most closely matches the sampled voltage. For example, if the voltage is greater than the midpoint, tap 11 0000 0000b will be tried next. If not, 01 0000 0000b will be tested.

Inaccuracy on the 83C196EA A-step

The analog-to-digital converter has exhibited an inaccuracy of about 6 LSBs with missed codes throughout the operating range. The missed codes are systematic in that the two LSBs always appear to return 11; thus, codes ending in 00, 01, and 10 tend to be missed.

IMPLICATION: The root cause was traced to a layout error in which signals in the analog portion of the converter were incorrectly wired. This error caused the selected test voltage to **decrease** as the two LSBs of a 10-bit conversion incremented from 00 to 11. Thus, when the current voltage being tested was within about 4 LSBs of (but less than) the sampled voltage, the A/D would incorrectly continue the search lower than the current point.

WORKAROUND: None

STATUS: Intended fix on B-step. The layout has be fixed so that the multiplexer which is controlled by the two LSBs is correctly wired to the resistor ladder. Refer to Summary Table of Changes to determine the affected stepping(s).

9600005. Serial Port Default Baud Rate 4800 Baud in Test ROM Mode

PROBLEM: The default baud rate for the serial port in test-ROM execution mode is 4800 baud (should be 9600 baud).

IMPLICATION: Default baud rate of most tools is 9600 baud. This erratum causes a baud rate of 4800 baud, requiring changes to tools (emulators, etc.) from the normal convention.

WORKAROUND: External devices must connect at 4800 baud and may use RISM calls to set the EA baud rate register to 9600 baud (or other speeds desired).

STATUS: Intended fix on B-step. The default baud rate on the EA B-step will be 9600 baud. Refer to Summary Table of Changes to determine the affected stepping(s).

9600006. PTS Block Move

PROBLEM: It was found that the PTS block move routine always updated the destination pointer, regardless of the state of the DU bit in the PTS control block. This was traced to an error in the microcode for the PTS block move instruction and has been fixed.

IMPLICATION: PTS block move is not useable on the A-step.

WORKAROUND: None

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600007. TIJMP / PIH Missed Interrupts

PROBLEM: If an interrupt to a PIH block occurs at the same time as the PIH_VEC_IDX SFR is being read, the interrupt will be lost. The root cause was found to be a signal to load the PIH interrupt pending register occurred one state too early. This caused the slave pending register to be loaded from the master at the same time as interrupts were being cleared from the slave due to the read of PIH_VEC_IDX SFR.

IMPLICATION: Interrupts may be missed under above described conditions.

WORKAROUND: Intended fix on B-step. The fix was to delay the transfer from master to slave when the PIH_VEC_IDX SFR is being read.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600008. On-Chip RISM “Next” Commands

PROBLEM: The test ROM code that implements the “next” form (write_next_byte, ...) of the RISM commands incorrectly tested the wrong bit to decode “next” commands from standard commands (write_byte).

IMPLICATION: “Next” RISM commands (in test ROM mode) do not work correctly.

WORKAROUND: Use only standard RISM commands write_word, write_byte, read_word, read_byte.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600009. SDU Interrupt on Branch with Wait States

PROBLEM: The SDU is able to generate an interrupt breakpoint based on an address match. If the breakpoint is located in memory that is accessed with wait states, and the breakpoint location is a branch instruction, the breakpoint will not be detected.

IMPLICATION: The SDU breakpoint detection does not work if the breakpoint is on a branch instruction and is located in memory using wait states.

WORKAROUND: None. Do not set SDU breakpoints on branch instructions.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600010. WR# Active Low on Falling Edge of ALE

PROBLEM: The EA bus controller has the ability to dynamically change its external bus width and type (6/8 bit bus and multiplexed/demultiplexed types). For the first 8-bit demultiplexed bus cycle following a 16-bit multiplexed bus cycle, the WR# signal incorrectly goes low on the falling edge of ALE on the A-step instead of near the rising edge of ALE.

IMPLICATION: In systems that interface to both 16-bit multiplexed and 8-bit demultiplexed memory devices, the 83C196EA presents the WR# signal to the external memory devices for a shorter period of time than expected.

WORKAROUND: None.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600011. P2.6 Pullup

PROBLEM: By holding certain pins on the 83C196EA low/high upon reset, test modes can be entered. To prevent unwanted entry into these modes, the pins are typically pulled up/down on reset. On the A-step, P2.6 was weakly pulled high. Design methodology dictates that this pin should have a medium pullup. It is important to note, however, that no test mode entry problems have been observed.

IMPLICATION: None expected. Improvement made to match design methodology for more secure prevention of unwanted test mode entry.

WORKAROUND: None.

STATUS: On the B-step, P2.6 will have a medium pullup (like other test mode entry pins). Refer to Summary Table of Changes to determine the affected stepping(s).

9600012. Emulator CLKE Pin Inactive During Reset

PROBLEM: During reset, the CLKE signal is inactive on the A-step.

IMPLICATION: Affects in-circuit emulator designs only.

WORKAROUND: Emulator dependent.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600013. Emulator Peripheral Interrupt Handler Conflict

PROBLEM: When the 83C196EA in-circuit emulation circuitry (ICE) is enabled, there is a bus conflict between the peripheral interrupt handlers and the ICE.

IMPLICATION: Affects in-circuit emulator designs only. Interrupts from the PIHs will not work on the A-step.

WORKAROUND: None.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600014. Emulator Missed Data Match

PROBLEM: For some locations, ICE breakpoint circuitry looking for a data match does not get internally transferred correctly, resulting in a missed data match.

IMPLICATION: Affects in-circuit emulator designs only. Breakpoint on data will not work correctly in all cases.

WORKAROUND: None.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600015. READY# Function Not Enabled in ICE Mode

PROBLEM: Upon ICE mode entry, the READY# pin/function was incorrectly not enabled on the A-step.

IMPLICATION: Affects in-circuit emulator designs only. Since READY# is usually reconstructed, this errata is expected to have little effect.

WORKAROUND: Emulator initialization software needs to configure the port pin P5.6/READY# for system function.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

None for this revision of this specification update.