87C196JQ
SPECIFICATION UPDATE

Release Date: January, 1997
Order Number: 272857-002

The 87C196JQ may contain design defects or errors known as errata. Characterized errata that may cause the 87C196JQ's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the new Specification Update Document. It contains all identified errata published prior to this date.
01/08/97	002	Added documentation changes 001–003.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
87C196KR/KQ 87C196JV/JT 87C196JR/JQ Advanced 16-bit CHMOS Microcontroller datasheet	270827-006
8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual	272258-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 87C196JQ product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings			Page	Status	ERRATA
	D#	#	#			
001	X			9	NoFix	External Addressing of Locations 1B00-1BDFH

Specification Changes

Number	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

Number	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	D#	#	#			
001	X			10		EPA Timer Reset/Write Conflict
002	X			10		Valid Time Matches
003	X			10		P6_Pin.4-.7 Not Updated Immediately
004	X			10		Write Cycle During Reset
005	X			10		Indirect Shift Count Value
006	X			11		P2.7 (CLKOUT)
007	X			11		EPA Overruns
008	X			13		Indirect Addressing With AutoIncrement

Documentation Changes

Number	Document Revision	Page	Status	DOCUMENTATION CHANGES
001	272258-002	15	Doc	High address inputs to the low EPROM should be A14:8 in Figure 15-18.
002	272258-002	16	Doc	Addresses 201DH and 201FH should contain FFH in Table 4-2.

Documentation Changes

Number	Document Revision	Page	Status	DOCUMENTATION CHANGES
003	272258-002	16	Doc	In Table 7-2, P2_DIR description change.

IDENTIFICATION INFORMATION

Markings

D-step devices can be identified by the letter “D” following the eight-digit FPO number on the top of the package.

ERRATA

001. External Addressing of Locations 1B00–1BDFH

PROBLEM: Affected devices cannot access external memory locations 1B00–1BDFH. Writing to these locations does not generate a bus cycle. Reading from these locations returns the value FFH, but does not generate a bus cycle.

IMPLICATION: Applications cannot access external locations 1B00H–1BDFH.

WORKAROUND: Applications must access external memory that may reside at 1B00–1BDFH at an alternative external memory location.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. EPA Timer Reset/Write Conflict

PROBLEM: If software writes to the EPA timer at the same time that an EPA channel resets that timer, it is indeterminate which action will take precedence. Software should not write to a timer that is being reset by EPA signals.

002. Valid Time Matches

PROBLEM: A timer must increment or decrement to the compare value in order for a match to occur. Loading a timer with a value that is equal to an EPA compare value does cause a match. Likewise, with an EPA compare value of 0, a timer reset does not cause a match.

003. P6_REG.4-.7 Not Updated Immediately

PROBLEM: A value written to any of the upper four bits of P6_REG is temporarily held in a buffer until the corresponding P6_MODE bit is cleared, at which time the value is loaded into the P6_REG bit. A value read from a P6_REG bit is the value currently in the register, not the value in the buffer. Therefore, any change to a P6_REG bit can be read only after the corresponding P6_MODE bit is cleared.

004. Write Cycle During Reset

PROBLEM: If a reset occurs while the microcontroller is writing to an external memory device, the contents of the external memory device may be corrupted.

005. Indirect Shift Count Value

PROBLEM: The SHRL and SHLL instructions function correctly with count values 0–31, inclusive. However, a shift count value of XX100000B causes 32 shifts, which results in no shift taking place. With all other count values, the upper 3 bits are masked off and the remaining bits specify the number of shifts. Also, a shift count value of XX1XXXXXB causes the overflow flag and the overflow-trap flag to be set.

IMPLICATION: Customers using SHRL and SHLL instructions with a count value greater than 31 will be affected.

WORKAROUND: Ensure that the count value never exceeds 31.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

006. P2.7 (CLKOUT)

PROBLEM: P2.7 (CLKOUT) does not operate in open drain mode.

007. EPA Overrruns

PROBLEM: The EPA can lock up if overruns are handled incorrectly. Overruns occur when an EPA input transitions at a rate that cannot be handled by the EPA interrupt service routine. If no overrun handling strategy is in place, and if the following three conditions exist, a situation may occur where both the capture buffer and the EPAx_TIME register contain data, and no EPA interrupt pending bit is set:

- an input signal with a frequency high enough to cause overruns is present on an enabled EPA pin, and
- the overwrite bit is set (EPAx_CON.0 = 1; old data is overwritten on overrun), and
- the EPAx_TIME register is read at the exact instant that the EPA recognizes the captured edge as valid.

The input frequency at which this occurs depends on the length of the interrupt service routine as well as other factors. Unless the interrupt service routine includes a check for overruns, this situation will remain the same until the device is reset or the EPAx_TIME register is read. The act of reading EPAx_TIME allows the buffered time value to be moved into EPAx_TIME. This clears the buffer and allows another event to be captured. Remember that the act of transferring the buffer contents to the EPAx_TIME register is what actually sets the EPAx interrupt pending bit and generates the interrupt.

WORKAROUND: Any one of the following methods can be used to prevent or recover from an EPA overrun situation.

- Clear EPAx_CON.0

  When the overwrite bit (EPAx_CON.0) is zero and both the EPAx_TIME register than the buffer are full, the EPA does not consider a captured edge until the EPAx_TIME register is read and the data in the capture buffer is transferred to EPAx_TIME. This prevents overruns by ignoring new input capture events when both the capture buffer and EPAx_TIME contain valid capture times. The OVRx pending bit in EPA_PEND is set to indicate that an overrun occurred.

- Enable the OVRx interrupt and read the EPAx_TIME register within the ISR

If an overrun occurs, the overrun (OVRx) interrupt will be generated. The OVRx interrupt will then be acknowledged and its interrupt service routine will read the EPAx_TIME register. After the CPU reads the EPAx_TIME register, the buffered data moves from the buffer to the EPAx_TIME register. This sets the EPA interrupt pending bit.

- Check for pending EPAx interrupts before exiting an EPAx ISR

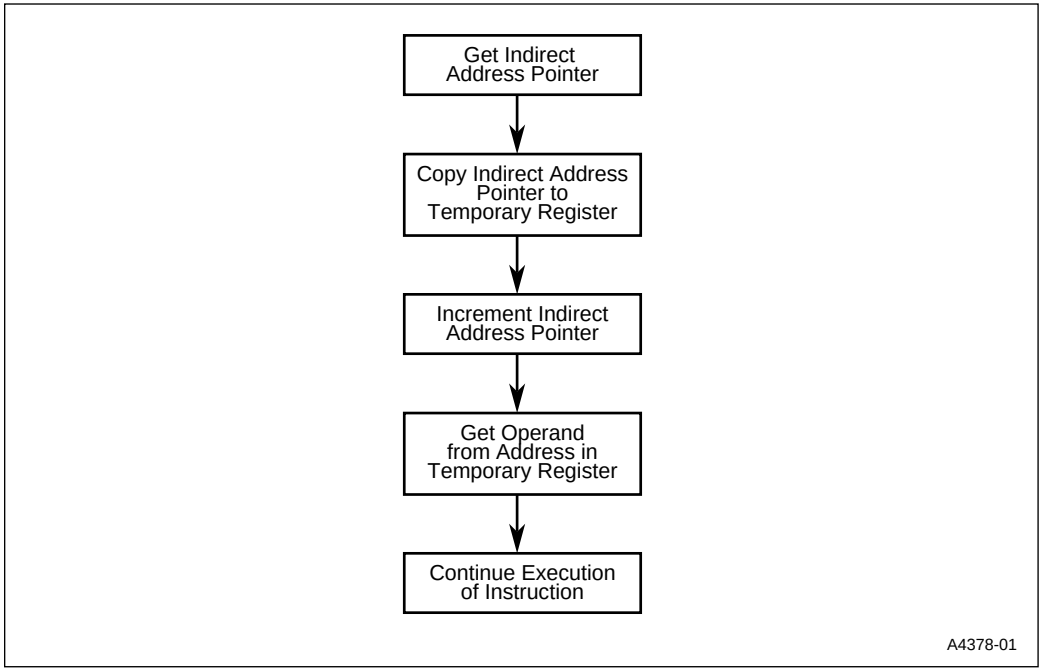
  Another method for avoiding this situation is to check for pending EPA interrupts before exiting the EPA interrupt service routine. This is an easy way to detect overruns and additional interrupts. It can also save loop time by eliminating the latency necessary to service the pending interrupt. However, this method cannot be used with the peripheral transaction server (PTS).

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

008. Indirect Addressing With AutoIncrement

PROBLEM: For indirect addressing with autoincrement, a pointer that points to itself results in an access to the incremented pointer address rather than the original pointer address.

The CPU stores the pointer's value in a temporary register, increments the pointer, then accesses the operand at the address contained in the temporary register, as shown in this flowchart.



Therefore, if the pointer points to itself, the CPU accesses the operand at the incremented address contained in the pointer.

For example, assume ax = 1CH and bx = 40H. The following code causes the CPU to access the operand at the incremented address:

```
ld    ax,#ax
ldb   bx,[ax]+


ld    1CH,#1CH;1CH←1CH;load location 1CH with value 1CH
ldb   40H,[1CH]+;temp←1CH;save 1CH into temp register
              ;1CH←1DH;increment the contents of 1CH
              ;40H←1DH;load the contents of location 1CH
                   ;(location 1CH
                   ;now contains the value 1DH) into 40H
```

WORKAROUND: Avoid using an indirect address pointer that points to itself.

For example, assume ax = 1CH, bx = 1DH, and cx = 40H. The following code causes the CPU to access the operand at the intended, unincremented address:

```
ld    ax,#bx      ;where bx ≠ ax
ldb   cx,[ax]+


ld    1CH,#1DH;1CH←1DH;load location 1CH with value 1DH
ldb   40H,[1CH]+;temp←1DH;save 1DH (contents of 1CH) into temp
                ;register
              ;1CH ←1EH;increment the contents of 1CH
              ;40H←1DH;load the contents of temp into 40H
```

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

DOCUMENTATION CHANGES

001. High address inputs to the low EPROM should be A14:8 in Figure 15-18.

ITEM: The next revision of the user's manual will include the following corrected graphic.

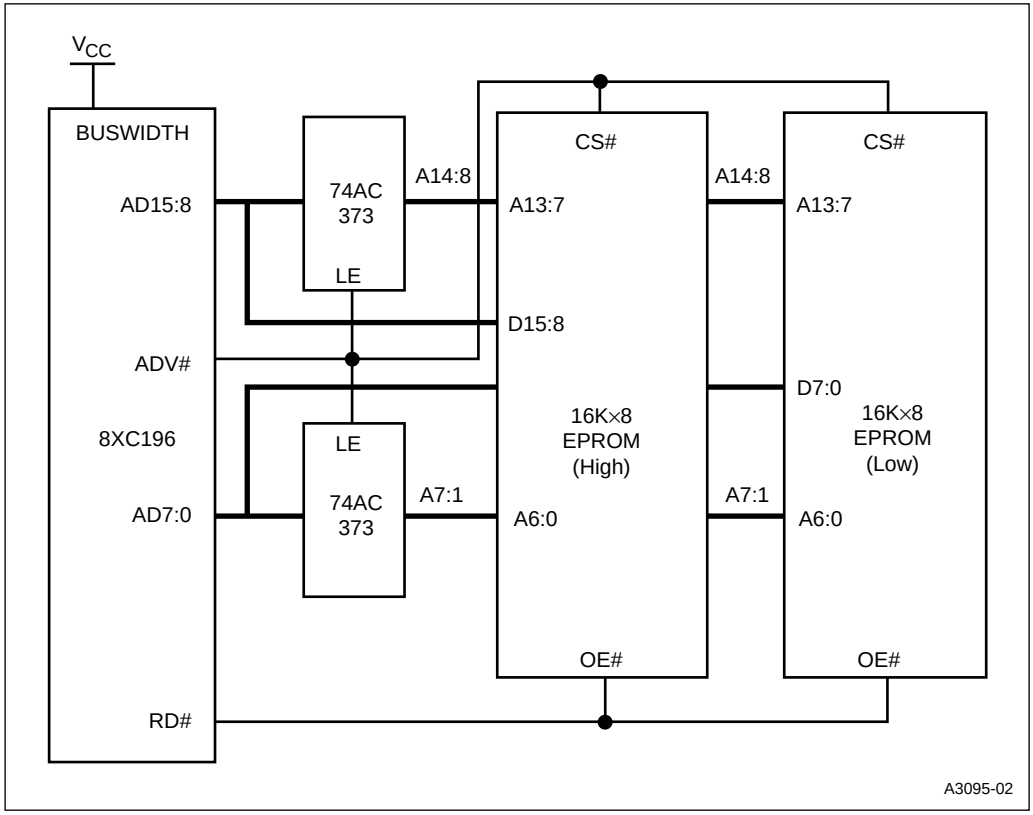


Figure 1. 16-bit System with EPROM

002. Addresses 201DH and 201FH should contain FFH in Table 4-2.

ITEM: The next revision of the user's manual will include the following corrected table.

Table 0-1. Special-purpose Memory Addresses

Hex Address	Description
207F 205E	Reserved (each byte must contain FFH)
205D 2040	PTS vectors
203F 2030	Upper interrupt vectors
202F 2020	Security key
201F	Reserved (must contain FFH)
201E	Reserved (must contain FFH)
201D	Reserved (must contain FFH)
201C	Reserved (must contain FFH)
201B	Reserved (must contain 20H)
201A	CCB1
2019	Reserved (must contain 20H)
2018	CCB0
2017 2016	OFD flag (see page 13-12 and page 16-8)
2015 2014	Reserved (each byte must contain FFH)
2013 2000	Lower interrupt vectors

003. In Table 7-2, P2_DIR description change.

ITEM: The next revision of the user's manual will include the following corrected register description.

Mnemonic	Address	Description
P2_DIR	1FCBH	Port Direction Register Each bit controls the configuration of the corresponding pin. Clearing a bit configures the corresponding pin as a complementary output; setting a bit configures the corresponding pin as an open-drain output or a high-impedance input.