87C196JV 20 MHz
ADVANCED 16-BIT CHMOS MICROCONTROLLER

Automotive

- **−40°C to +125°C Ambient**
- **High Performance CHMOS 16-Bit CPU**
- **48 Kbytes of On-Chip EPROM**
- **Up to 1.5 Kbyte of On-Chip Register RAM**
- **512 Bytes of Additional RAM (Code RAM)**
- **Register-Register Architecture**
- **6 Channel/10-Bit A/D with Sample/Hold**
- **35 Prioritized Interrupt Sources**
- **Up to Seven 8-Bit (56) I/O Ports**
- **Full Duplex Serial I/O Port**
- **Dedicated Baud Rate Generator**
- **High Speed Peripheral Transaction Server (PTS)**
- **Two 16-Bit Software Timers**
- **6 High Speed Capture/Compare (EPA)**
- **Full Duplex Synchronous Serial I/O Port (SSIO)**
- **Two Flexible 16-Bit Timer/Counters**
- **Flexible 8-/16-Bit External Bus**
- **1.4 μs 16 x 16 Multiply**
- **2.4 μs 32/16 Divide**
- **52-Pin PLCC Package**
- **Oscillator Fail Detect**

The 87C196JV A-step (JV-A), is a new member of the MCS® 96 microcontroller family. This device is a memory scalar of the 87C196JT A-step (JT-A) and is designed for strict functional and electrical compatibility. The 87C196JV has the highest 52-lead memory density of the MCS 96 microcontroller family, with 48K of on-chip EPROM, 1.5K of on-chip register RAM, and 512 bytes of additional RAM (Code RAM). The high memory integration of the 87C196JV supports high-functionality in a low pin-count package and the use of the high level programming language C.

The MCS 96 microcontroller family members are all high-performance microcontrollers with a 16-bit CPU. The 87C196JV is composed of the high-speed (20 MHz) core as well as the following peripherals: 48 Kbytes of Program EPROM, up to 1.5 Kbyte of Register RAM. 512 bytes of code RAM (16-bit addressing modes) with the ability to execute from this RAM space, a 6 channel-10-Bit/ ±3 LSB analog to digital converter with programmable S/H times with conversion times <5 μs at 16 MHz, an asynchronous/synchronous serial I/O port (8096 compatible) with a dedicated 16-bit baud rate generator, an additional synchronous serial I/O port with full duplex master/slave transceivers, a flexible timer/counter structure with prescaler, cascading, and quadrature capabilities, 6 modularized multiplexed high speed I/O for capture and compare (called Event Processor Array) with 250 ns resolution and double buffered inputs, a sophisticated prioritized interrupt structure with programmable Peripheral Transaction Server (PTS). The PTS has several channel modes, including single/burst block transfers from any memory location to any memory location, a PWM and PWM toggle mode to be used in conjunction with the EPA, and an A/D scan mode.

Additional SFR space is allocated for the EPA and can be ''windowed'' into the lower Register RAM area.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

February 1996 **Order Number: 272580-003**

ARCHITECTURE

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CPU FEATURES

- Powerdown and Idle Modes
- 20 MHz Operating Frequency
- A High Performance Peripheral Transaction Server (PTS)
- 35 Interrupt Vectors
- 512 Bytes of Additional Code RAM
- 1.5 Kbyte of Additional Register RAM
- "Windowing" Allows 8-Bit Addressing to Some 16-Bit Addresses
- 1.4 μs 16 x 16 Multiply
- 2.4 μs 32/16 Divide
- Oscillator Fail Detect

PERIPHERAL FEATURES

- Programmable A/D Conversion and S/H Times
- 6 Capture/Compare I/O with 2 Flexible Timers
- 4 Additional Software Timers
- Synchronous Serial I/O Port for Full Duplex Serial I/O
- Total Utilization of ALL Available Pins (I/O Mux'd with Control)
- 2 16-Bit Timers with Prescale and Cascading
- Up to 12 Externally Triggered Interrupts

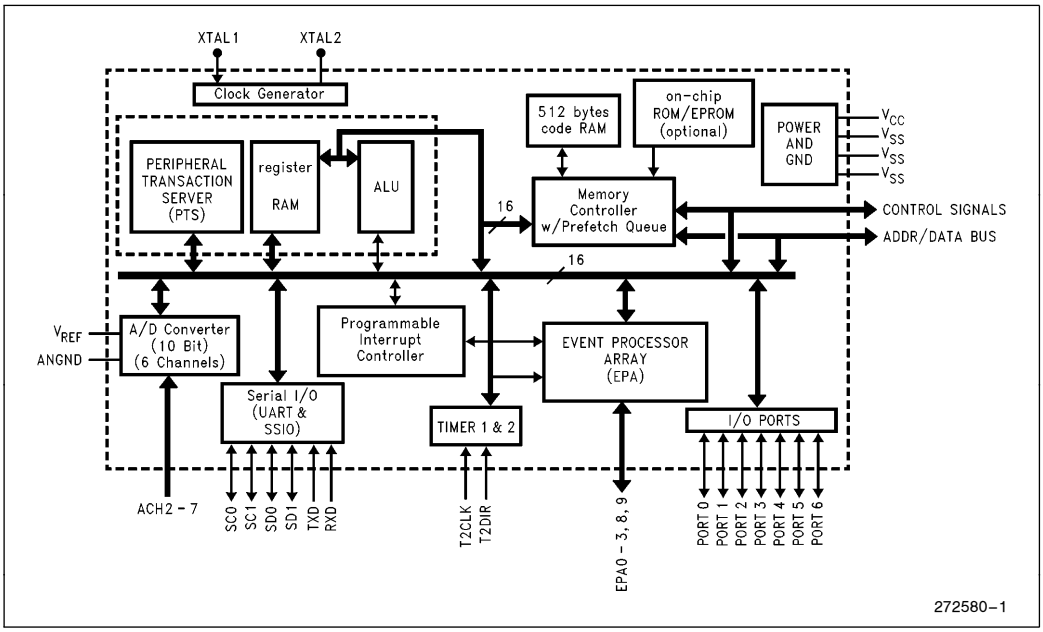

Figure 1. Block Diagram

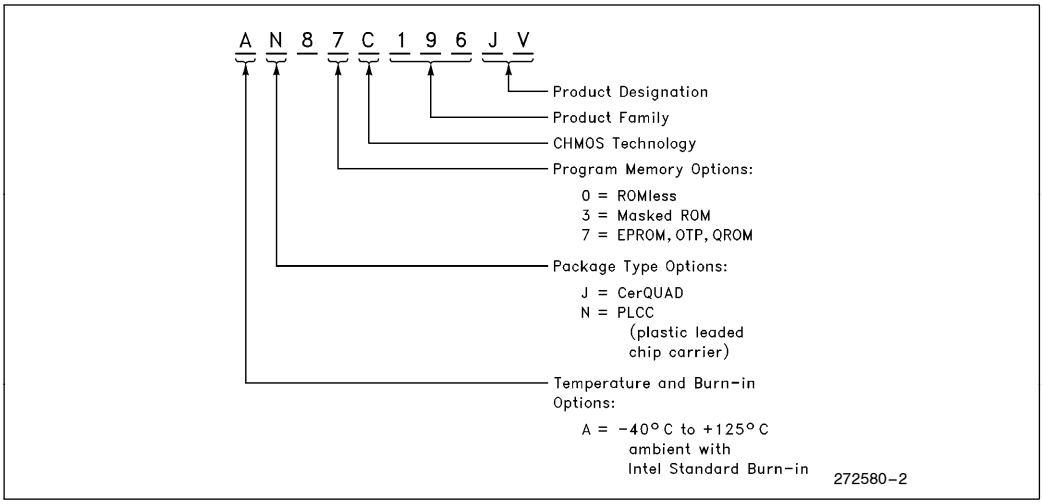

Figure 2. The 8XC196JV Family Nomenclature

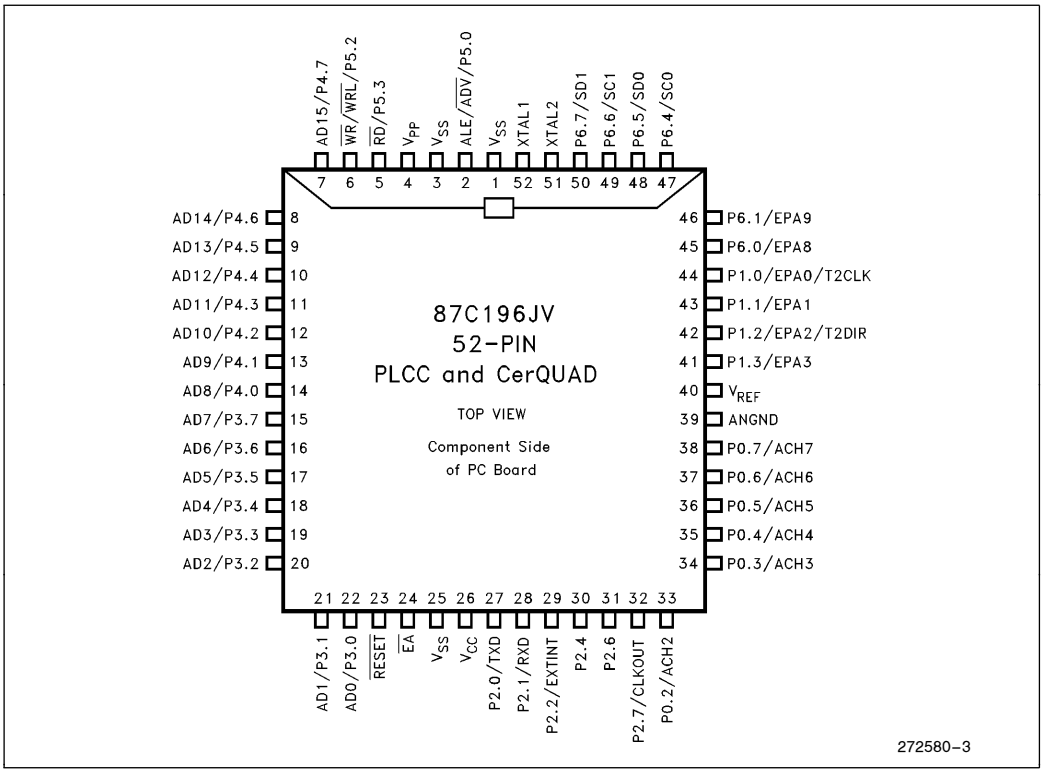

Figure 3. Package Diagram

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}, V_{SS}, V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected to a single ground plane.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
$\overline{\text{RESET}}$	Reset input to the chip. Input low for at least 16 state times will reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, bytes are read from 2018H and 201AH loading the CCBs, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip EPROM/ROM. $\overline{\text{EA}}$ equal to a low causes accesses to these locations to be directed to off-chip memory. $\overline{\text{EA}}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{\text{EA}}$ latched at reset.
P5.0/ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is active only during external memory accesses. Also LSIO when not used as ALE.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
P5.3/$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is active only during external memory reads or LSIO when not used as $\overline{RD}$.
P5.2/$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR, $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active during external memory writes. Also an LSIO pin when not used as $\overline{WR}$/$\overline{WRL}$.
P1.0/T2CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however it may also be used as a TIMER2 Clock input. The TIMER2 will increment or decrement on both positive and negative edges of this pin.
P1.2/T2DIR	Dual function I/Opin. Primary function is that of a bidirectional I/O pin, however it may also be used as a TIMER2 Direction input. The TIMER2 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–3 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH2–7	6-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
P6.4–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.

ELECTRICAL CHARACTERISTICS

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ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5V to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation..... 0.5W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature under Bias	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	20	MHz(4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current (−40°C to +125°C Ambient)			95	mA	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While Device in Reset)
I_{CC1}	Active Mode Supply Current (Typical)		60		mA	
I_{REF}	A/D Reference Supply Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	40	mA	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		50	TBD	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$ (Note 6)
V_{IL}	Input Low Voltage (All Pins)	−0.5V		0.3 V_{CC}	V	
V_{IH}	Input High Voltage (All Pins)	0.7 V_{CC}		V_{CC} + 0.5	V	(Note 7)

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OL}	Output Low Voltage (Outputs Configured as Push/Pull)			0.3 0.45 1.5	V V V	I_{OL} = 200 μA(3, 5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Push/Pull)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA(3, 5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
I_{LI}	Input Leakage Current (Std. Inputs, P3/4)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$(2)
I_{LI1}	Input Leakage Current (Port 0—A/D Inputs)			±2	μA	$V_{SS} \le V_{IN} \le V_{REF}$
I_{IH}	Input High Current (NMI Pin)			+175	μA	$V_{SS} \le V_{IN} \le V_{CC}$
V_{OH2}	Output High Voltage in RESET	V_{CC} − 1V			V	I_{OH} = −15 μA(1)
I_{OH2}	Output High Current in RESET	−30 −75 −90		−120 −240 −280	μA μA μA	V_{OH2} = V_{CC} − 1.0V V_{OH2} = V_{CC} − 2.5V V_{OH2} = V_{CC} − 4.0V
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	
V_{OL3}	Output Low Voltage in RESET (RESET pin only)			0.3 0.5 0.8	V V V	I_{OL3} = 4 mA (Note 8) I_{OL3} = 6 mA I_{OL3} = 8 mA
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPU}	Weak Pullup Resistance (Approx)		150K		Ω	(Note 6)

NOTES:
1. All BD (bidirectional) pins except CLKOUT. CLKOUT is excluded due to not being weakly pulled high in reset. BD pins include Port1, Port2, Ports 3, 4 and 5 and Port6.
2. Standard Input pins include XTAL1, $\overline{EA}$, $\overline{RESET}$ and Port 1/2/3/4/5/6 when configured as inputs.
3. All Bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is Static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date. Target values are ±10 mA.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and V_{REF} = V_{CC} = 5.0V.
7. V_{IH} Max for Port 0 pins = V_{REF} + 0.5V.
8. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns, F_{OSC} = 20 MHz.

The system must meet these specifications to work with the 87C196JV

Symbol	Parameter	Min	Max	Units
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 25	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 50	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns

AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns, F_{OSC} = 20 MHz.

The 87C196JV will meet these specifications.

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	4.0	20.0	MHz(1)
T_{OSC}	Oscillator Period (1/Fxtal)	50	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(2)
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	− 10	15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Falling Edge to CLKOUT Rising	− 20	15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns
T_{LHLL}	ALE/$\overline{ADV}$ High Period	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Setup to ALE/$\overline{ADV}$ Falling Edge	T_{OSC} − 15		ns
T_{LLAX}	Address Hold after ALE/$\overline{ADV}$ Falling Edge	T_{OSC} − 40		ns
T_{LLRL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 30		ns

AC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

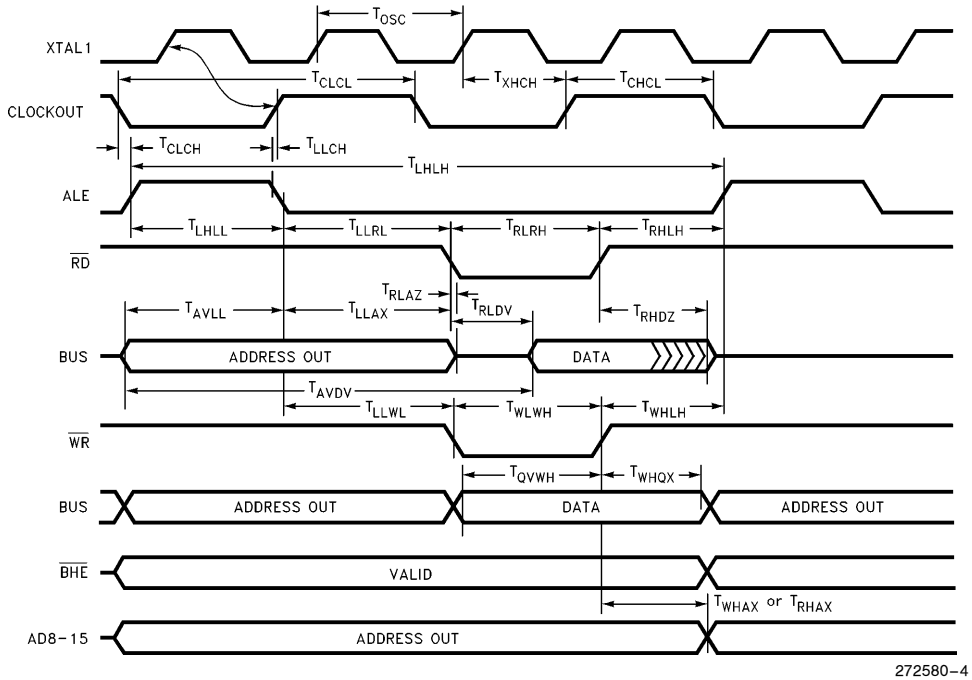
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns, F_{OSC} = 20 MHz.

The 87C196JV will meet these specifications.

Symbol	Parameter	Min	Max	Units
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$		ns
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns(5)
T_{LLWL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	-5	25	ns
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 23$		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	-10	15	ns
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 20$		ns
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 25$		ns
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	$T_{OSC} - 10$	$T_{OSC} + 15$	ns(3)
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 30$(4)		ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 30$(4)		ns

NOTES:
1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. T_{RLAZ} (max) = 5 ns by design.

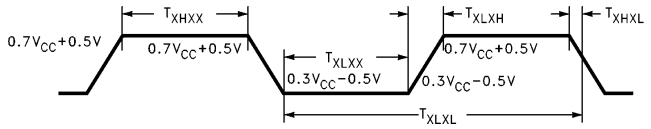
System Bus Timing



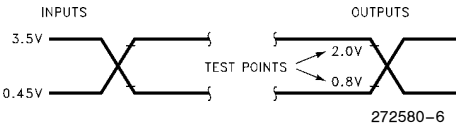
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4.0	20	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	50	250	ns
T_{XHXX}	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS

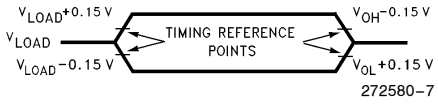


AC TESTING INPUT, OUTPUT WAVEFORMS



NOTE:
AC Testing Inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS



NOTE:
For timing purposes a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

THERMAL CHARACTERISTICS

Device and Package	θ_{JA}	θ_{JC}
AN87C196JV (52-Lead PLCC)	42°C/W	15°C/W

NOTES:
1. θ_{JA} = Thermal resistance between junction and the surrounding environment (ambient). Measurements are taken 1 ft. away from case in air flow environment.
   θ_{JC} = Thermal resistance between junction and package surface (case).
2. All values of θ_{JA} and θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ±2°C/W.
3. Values listed are at a maximum power dissipation of 0.50W.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "t" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
R— $\overline{RD}$
W— $\overline{WR}$/$\overline{WRH}$/$\overline{WRI}$
X— XTAL1
Y— READY

EPROM SPECIFICATIONS

AC EPROM PROGRAMMING CHARACTERISTICS

Operating Conditions: Load Capacitance = 150 pF; T_C = 25°C ±5°C, V_{REF} = 5.0V ±0.5V, V_{SS}, ANGND = 0V. V_{PP} = 12.5V ±0.25V; $\overline{EA}$ = 12.5V ±0.25V; F_{OSC} = 5.0 MHz

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(3)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run time programming is done with F_{OSC} = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
2. Programming Specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses use 300 T_{OSC} + 100 μs.

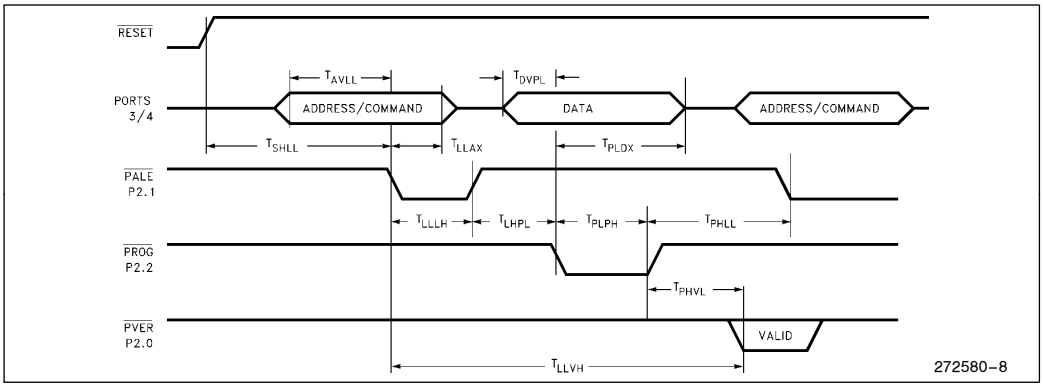
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		100	mA

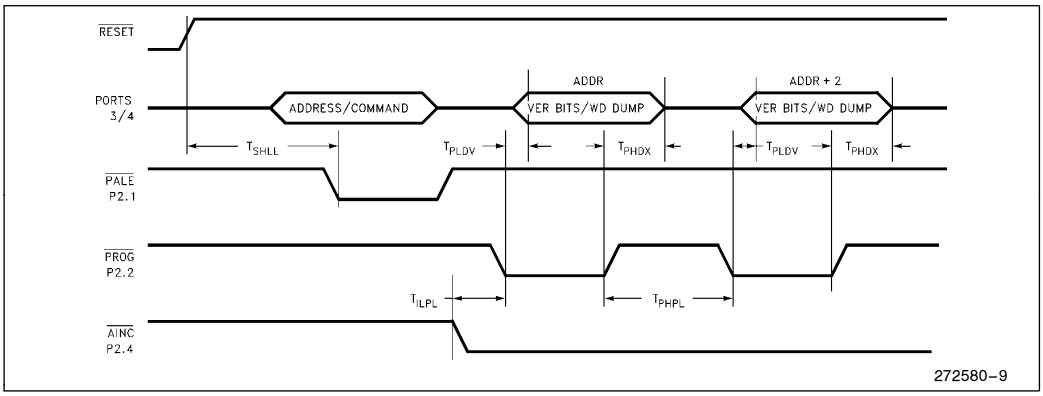
NOTE:
V_{PP} must be within 1V of V_{CC} while V_{CC} < 4.5V. V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} > 4.5V.

EPROM PROGRAMMING WAVEFORMS

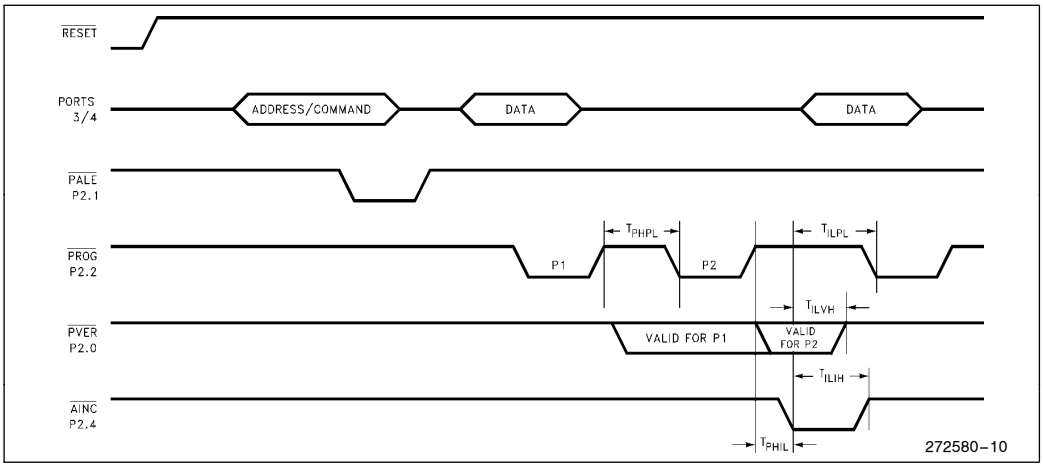
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



A TO D CONVERTER SPECIFICATIONS

The speed of the A/D converter in the 10-bit or 8-bit modes can be adjusted by setting the AD__TIME special function register to the appropriate value. The AD__TIME register only programs the speed at which the conversions are performed, not the speed at which it can convert correctly.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be within 0.5V of V_{CC} since it supplies both the resistor ladder and the digital portion of the converter and input port pins.

For testing purposes, after a conversion is started, the device is placed in the IDLE mode until the conversion is complete. Testing is performed at V_{REF} = 5.12V and 20 MHz operating frequency.

There is an AD__TEST register that allows for conversion on ANGND and V_{REF} as well as zero offset adjustment. The absolute error listed is without doing any adjustments.

A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Automotive Ambient Temperature	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2, 3)	V
T_{SAM}	Sample Time	2.0		μs(4)
T_{CONV}	Conversion Time	15	18	μs(4)
F_{OSC}	Oscillator Frequency	4	20	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. Testing is performed at V_{REF} = 5.12V.
4. The value of AD__TIME must be selected to meet these specifications.

Parameter	Typical*(1)	Min	Max	Units**
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	−3 +3	LSBs
Full Scale Error	±2			LSBs
Zero Offset Error	±2			LSBs
Non-Linearity			±3	LSBs
Differential Non-Linearity		> −0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1, 2, 3)
Feedthrough	−60			dB(1, 2)
V_{CC} Power Supply Rejection	−60			dB(1, 2)
Input Resistance		750	1.2K	Ω(1)
DC Input Leakage		0	2	μA

NOTES:
*These values are expected for most parts at 25°C but are not tested or guaranteed.
**An ''LSB'', as used here, has a value of approximately 5 mV. (See Automotive Handbook for A/D glossary of terms).
1. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
2. DC to 100 KHz
3. Multiplexer Break-Before-Make Guaranteed.

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

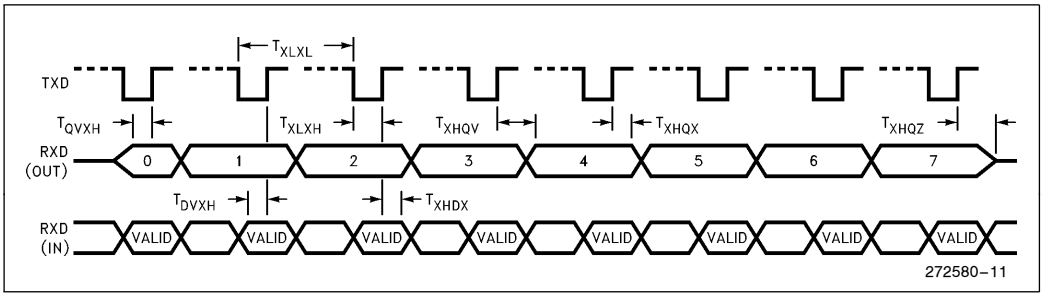
Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = 100 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	$8\ T_{OSC}$		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	$4\ T_{OSC} - 50$	$4\ T_{OSC} + 50$	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	$3\ T_{OSC}$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	$2\ T_{OSC} - 50$		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		$2\ T_{OSC} + 50$	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	$2\ T_{OSC} + 200$		ns
T_{XHDX}(8)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(8)	Last Clock Rising to Output Float		$5\ T_{OSC}$	ns

NOTES:
8. Parameter not tested.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE 0

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



52-LEAD DEVICE DESIGN CONSIDERATIONS

The 87C196JV A-step is a memory scalar of the 52-lead 87C196JT A-step designed for strict functional and electrical compatibility. Both the 87C196JV and 87C196JT are 52-lead members of the Kx product family. Some functions that are on 68-lead devices are not supported on 52-lead devices because of the reduced pin-count. Following are the functionality differences between 52-lead Kx family members and 68-lead Kx family members.

68-Lead Functions Unsupported on the 52-Lead 87C196JV:
- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT and SLPCS Pin Support
- HLD/HLDA Functionality
- External Clocking/Direction of Timer1
- WRH or BHE Functions
- Dynamic Buswidth
- Dynamic Wait State Control

The following is a list of recommended practices when using 52-lead Kx devices:

(1) **External Memory.** Use an 8-bit bus mode only. There is neither a $\overline{WRH}$ or BUSWIDTH pin. The bus cannot dynamically switch from 8- to 16-bit or vice versa. Set the CCB bytes to an 8-bit only mode, using $\overline{WR}$ function only.

(2) **Wait State Control.** Use the CCB bytes to configure the maximum number of wait states. If the READY pin is selected to be a system function, the device will lockup waiting for READY. If the READY pin is configured as LSIO (default after $\overline{RESET}$), the internal logic will receive a logic ''0'' level and insert the CCB defined number of wait states in the bus cycle. DON'T USE IRC = ''111''.

(3) **NMI Support.** The NMI is not bonded out. Make the NMI vector at location 203Eh vector to a Return instruction. This is for glitch safety protection only.

(4) **Auto-Programming Mode.** The 52-lead device will ONLY support the 16-bit zero wait state bus during auto-programming.

(5) **EPA4 through EPA7.** Since the JT/JR/JQ devices use the KR silicon, these functions are in the device, just not bonded out. A programmer can use these as compare only channels or for other functions like software timer, start and A/D conversion, or reset timers.

(6) **Slave Port Support.** The Slave port can not be used on 52-lead devices due to P5.4/SLPINT and P5.1/SLPCS not being bonded-out.

(7) **Port Functions.** Some port pins have been removed. P5.7, P5.6, P5.5, P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The PxREG, PxSSEL, and PxIO registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

Additionally, these port pins should be setup internally by software as follows:

1. Written to PxREG as ''1'' or ''0''.
2. Configured as Push/Pull, PxIO as ''0''.
3. Configured as LSIO.

This configuration will effectively strap the pin either high or low. *DO NOT Configure as Open Drain output ''1'', or as an Input pin. This device is CMOS.*

(8) **EPA Timer RESET/Write Conflict.** If the user writes to the EPA timer at the same time that the timer is reset, it is indeterminate which will take precedence. Users should not write to a timer if using EPA signals to reset it.

(9) **Valid Time Matches.** The timer must increment/decrement to the compare value for a match to occur. A match does not occur if the timer is loaded with a value equal to an EPA compare value. Matches also do not occur if a timer is reset and 0 is the EPA compare value.

(10) **P6__PIN.4–.7 Not Updated Immediately.** Values written to P6__REG are temporarily held in a buffer. If P6__MODE is cleared, the buffer is loaded into P6__REG.x. If P6__MODE is set, the value stays in the buffer and is loaded into P6__REG.x when P6__MODE.x is cleared. Since reading P6__REG returns the current value in P6__REG and not the buffer, changes to P6__REG cannot be read until/unless P6__MODE.x is cleared.

(11) **Write Cycle during Reset.** If RESET occurs during a write cycle, the contents of the external memory device may be corrupted.

(12) **Indirect Shift Instruction.** The upper 3 bits of the byte register holding the shift count are not masked completely. If the shift count register has the value 32 × n, where n = 1, 3, 5, or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

(13) **P2.7 (CLKOUT).** P2.7 (CLKOUT) does not operate in open drain mode. On the 87C196JV CLKOUT is active during RESET.

87C196JV ERRATA

No known errata at this time.

87C196JR/JQ D-STEP TO 87C196JV A-STEP DESIGN CONSIDERATIONS

1. Memory Scalar

The 87C196JV A-step is a memory scalar of the 87C196JR D-step.

	87C196JR D-Step	87C196JV A-Step
Register RAM	18h to 1FFh	18h to 3FFh and 1C00h to 1DFFh
Internal (Code) RAM	400h to 4FFh	400h to 5FFh
Internal ROM/EPROM	2000h to 5FFFh	2000h to DFFFh

2. 1B00–1BDFh External Addressing

The 87C196JR/JQ D-step cannot access external memory locations 1B00h–1BDFh. This JR/JQ D-step errata has been corrected on the 87C196JV A-step. A bus cycle does not occur when these addresses are accessed. If attempting to read from 1B00h–1BDFh a value of FFh is returned even though a read cycle is not generated. Writing to these locations will not generate an external bus cycle either.

87C196JR/JQ C-STEP TO JV A-STEP DESIGN CONSIDERATIONS

This section documents differences between the 87C196JR C-step (JR-C) and the 87C196JV A-step (JV-A). For a list of design considerations between 68-lead and 52-lead devices, please refer to the 52-lead Device Design Considerations section of this data sheet. Since the 87C196JQ is simply a memory scalar of the 87C196JR, the term ''JR'' in this section will refer to both the JR and JQ versions of the device unless otherwise noted.

The JR-C is simply a 87C196KR C-step (KR-C) device packaged within a 52-lead package. This reduction in pin count necessitated not bonding-out certain pins of the KR-C device. The fact that these ''removed pins'' were still present on the device but not available to the outside world allowed the programmer to take advantage of some of the 68-lead KR features.

The JV-A is a fully-optimized 52-lead device based on the 87C196JT A-step device which is based on the JR-D step device. The JT-A design database was used to assure that the JV-A would be fully compatible with the KR-C, JR-C, JR-D and other Kx family members. The main difference in the JV-A and JT-A as compared to the JR-C is that several of the unused (not bonded-out) functions on the JR-C were removed altogether on the JT-A.

Following is a list of differences between the JR-C and the JV-A, JT-A:

1. Port 3 Push-Pull Operation

It was discovered on JR-C that if Port 3 is selected for push-pull operation (P34__DRV register) during low speed I/O (LSIO), the port was driving data when the system bus was attempting to input data. It is rather unlikely that this errata would affect an application because the application would have to use Port 3 for both LSIO and as an external addr/data bus. None the less, this errata was corrected on the JT-A and JV-A.

2. V_{OH2} Strengthened

The DC Characteristics section of the Automotive KR Data Sheet contains a parameter, V_{OH2} (Output High Voltage in RESET (BD ports)) which is specified at $V_{CC} - 1V$ min at $I_{OH2} = -15\ \mu A$. This specification indicates the strength of the internal weak pull-ups that are active during and after reset. These weak pull-ups stay active until the user writes to PxMODE (previously known as PxSSEL) and configures the port pin as desired.

These pull-ups do not meet this V_{OH2} spec on the JR-C. The weak pull-ups on specified JT-A and JV-A ports have been enhanced to meet the published specification of $I_{OH2} = -15\ \mu A$.

3. ONCE Mode

ONCE mode is entered by holding a single pin low on the rising edge of $\overline{\text{RESET}}$. On the KR, this pin is P5.4/SLPINT. The JR-C does not support ONCE mode since P5.4/SLPINT (ONCE mode entry pin) is not bonded-out on these devices. To provide ONCE mode on the JT-A and JV-A, the ONCE mode entry function was moved from P5.4/SLPINT to P2.6/HLDA. This will allow the JT-A and JV-A to enter ONCE mode using P2.6 instead of removed pin P5.4.

4. PORT0

On the JR-C, P0.0 and P0.1 are not bonded out. However, these inputs are present in the device and reading them will provide an indeterminate result.

On the JT A-step and JV-A the analog inputs for these two channels at the multiplexer are tied to V_{REF}. Therefore, initiating an analog conversion on ACH0 or ACH1 will result in a value equal to full scale (3FFh). On the JT A-step and JV-A the digital inputs for these two channels are tied to ground, therefore reading P0.0 or P0.1 will result in a digital ''0''.

5. PORT1

On the JR-C, P1.4, P1.5, P1.6 and P1.7 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with JT A-step, JV A-step and future devices, it is recommended that the corresponding bits associated with the removed pins NOT be used to conditionally branch in software. These bits should be treated as reserved.

On the JT A-step and JV A-step unused port logic for these four port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been ''hard-wired'' to provide the following results when read:

Register Bits		When Read
P1__PIN.x	(x = 4,5,6,7)	1
P1__REG.x	(x = 4,5,6,7)	1
P1__DIR.x	(x = 4,5,6,7)	1
P1__MODE.x	(x = 4,5,6,7)	0

Writing to these bits will have no effect.

6. PORT2

On the JR-C, P2.3 and P2.5 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though is not available to the outside world. However, to maintain compatibility with JT A-step, JV A-step and future devices, it is recommended that the corresponding bits associated with the removed pins not be used to conditionally branch in software. These bits should be treated as reserved.

On the JT-A and JV-A, unused port logic for these two port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been ''hardwired'' to provide the fdllowing results when read:

Register Bits		When Read
P2__PIN.x	(x = 3,5)	1
P2__REG.x	(x = 3,5)	1
P2__DIR.x	(x = 3,5)	1
P2__MODE.x	(x = 3,5)	0

Writing to these bits will have no effect.

7. PORT5

On the JR-C, P5.1, P5.4, P5.5, P5.6 and P5.7 are not bonded out but are present internally on the device.

This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with JT A-step, JV A-step and future devices, it is recommended that the corresponding bits associated with the removed pins not be used to conditionally branch in software. These bits should be treated as reserved.

On the JT A-step and JV A-step unused port logic for these five port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been ''hardwired'' to provide the following results when read:

Register Bits		When Read
P5__PIN.x	(x = 1,4,5,6,7)	1
P5__REG.x	(x = 1,4,5,6,7)	1
P5__DIR.x	(x = 1,4,5,6,7)	1
P5__MODE.x	(x = 1,4,6)	0
P5__MODE.x	(x = 5) (EA# = 0)	1
P5__MODE.x	(x = 5) (EA# = 1)	0
P5__MODE.x	(x = 7)	1

Writing to these bits will have no effect.

8. PORT6

On the JR-C, P6.2 and P6.3 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with JT A-step, JV A-step and future devices, it is recommended that the corresponding bits associated with the removed pins not be used to conditionally branch in software. These bits should be treated as reserved.

On the JT A-step and JV A-step, unused port logic for these two port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been ''hardwired'' to provide the following results when read:

Register Bits		When Read
P6__PIN.x	(x = 2,3)	1
P6__REG.x	(x = 2,3)	1
P6__DIR.x	(x = 2,3)	1
P6__MODE.x	(x = 2,3)	0

Writing to these bits will have no effect.

9. 8XC196JQ Internal to External Memory Roll-over Point

8XC196JQ devices are simply 8XC196JR devices with less memory. Both the JQ-C and JQ-D are fabricated from the JR-C and JR-D respectfully. The difference between JQ and JR devices is that memory locations beyond the supported boundaries on the JQ are not tested in production and should not be used. Any software which relies upon reading or writing these locations may not function correctly. Following are the supported memory maps for these devices:

	JQ C- and D-Step	JR C- and D-Step
Register RAM	18h to 17Fh	18h to 1FFh
Internal (Code) RAM	400h to 47Fh	400h to 4FFh
Internal ROM/EPROM	2000h to 4FFFh	2000h to 5FFFh

It is important to note that the internal to external memory roll-over point for both the JR and JQ devices is the same (6000h and above goes external). Two guidelines the programmer should follow to insure no problems are encountered when using JQ devices are:

a) For JQ devices, the program must contain a jump to a location greater than 5FFFh before the 12K boundary (4FFFh) is reached. This is necessary only if greater than 12K of program memory is required with a JQ device and portions of the program execute from internal ROM/EPROM.

b) For JQ devices with EA# tied to ground, use only internal program memory from 2000h to 4FFFh. Do not use the unsupported locations from 5000h to 5FFFh.

10. EPA Channels 4 through 7

The JR C-step device is simply a 68-lead KR-C device packaged in a 52-lead package. The reduced pin-out is achieved by not bonding-out the unsupported pins. EPA4–EPA7 are among these pins that are not bonded-out. The fact that EPA4–EPA7 are still present allows the programmer to use these channels as software timers, to start A/D conversions, reset timers, etc. All of the port pin logic is still present and it is possible to use the EPA to toggle these pins internally. Please refer to the 52-Lead Device section in this Data Sheet for further information.

On the JT A-step and JV A-step the EPA4–EPA7 logic has NOT been removed from the device. This allows the programmer to still use these channels (as on the JR C-step) for software timers, etc. The only difference is that the associated port pin logic has been removed and does not exist internally. To maintain JR C-step to JT A-step and JV A-step compatibility, programmers should make sure that their software does not rely upon the removed port pin logic.

11. EPA Overruns

EPA ''lock-up'' can occur if overruns are not handled correctly, refer to Intel Techbit #DB0459 *''Understanding EPA Capture Overruns'',* date 12-9-93. Applies to EPA channels with interrupts and overruns enabled (ON/RT bit set to 1).

12. Indirect Addressing with Auto-Increment

For the special case of a pointer pointing to itself using auto-increment, an incorrect access of the incremented pointer address will occur instead of an access to the original pointer address. All other indirect auto-increment accesses will not be effected. Please refer to Techbit #MCO593.

Incorrect sequence: Results in ax being incremented by 1 and the contents of the address pointed to by ax+1 to be loaded into bx.

```
ld   ax,#ax
ldb  bx,[ax]+
```

Suggested sequence: Results in the contents of the address pointed to by ax to be loaded into bx and ax incremented by 1.

```
ld  ax,#bx; where ax does not equal bx
ldb cx,[ax]+
```

87C196JT TO 87C196JV DESIGN CONSIDERATIONS

1. The additional register RAM on the 87C196JV is mapped to 1C00h to 1DFFh. On the 87C196JT this memory range is mapped as external memory.
2. The 87C196JV has 48K of EPROM located from 2080h to DFFFh. The JT has 32K of EPROM located from 2080h to 9FFFh. Memory accesses between 1E00h and FFFFh go external for the 87C196JV. Access between A000h to FFFFh go external for the 87C196JT.

MEMORY MAP FOR JV

DFFFh 2080h	EPROM (Internal) 48 KByte. User EPROM starts here. JV/JT and all Kx products same.
207Fh 2000h	Chip configuration bytes, PTS Vectors, Interrupt Vectors, Security Key JV/JT and all Kx products same. (See Kx User's manual Table 3.2)
1FFFh 1F00h	Internal Special Function Registers (SFR's) (16-bit addressable) JV identical to JT and rest of Kx family. JV/JT 'reserved' locations (see Figure 3.2 Kx User's Manual).
1EFFh 1E00h	Mapped as external memory on JV, JT, and rest of Kx family
1DFFh 1C00h	Additional Register RAM on JV.
1BFFh 0600h	External Memory Space on JV/JT and rest of Kx family
05FFh 0400h	Code RAM. Same on JV, JT, KT
03FFh 0018h	Register RAM. Same on JV, JT, KT
0017h 0000h	Core Special Function Registers. Same on JV, JT, and rest of Kx/Jx family

DATASHEET REVISION HISTORY

This is the (-003) version of the 87C196JV datasheet.

1. The T_{RLDV} specification was changed from $T_{OSC} - 22$ to $T_{OSC} - 25$.
2. Design Consideration (13) changed to indicate CLKOUT active during reset.
3. V_{OL3} estimate added.

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