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APPLICATION NOTE

Interfacing a 20 MHz 8XC196 to an 82527 Serial Communications Controller

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1.0 INTRODUCTION

The purpose of this application note is to describe some of the hardware and software techniques for interfacing a 20 MHz 8XC196 device to the 82527 serial communications controller. This March 1995 revision (272732-001) supersedes the January 1993 draft version, and comprehends the latest 82527 specifications included in the March 1995 datasheet (order number 272250-05). Additionally, schematic diagrams demonstrating 82527 mode 0 (8-bit multiplexed) and mode 1 (16-bit multiplexed) interfacing techniques have been included. Though this application note targets a 20 MHz 8XC196 device, it is applicable to a 16 MHz 8XC196 with additional timing margins.

2.0 82527 CPU INTERFACE MODES

The 82527 has six CPU interface modes allowing users to connect the 82527 to host-CPU's of various architectures. The CPU interface modes are:

- 8-bit multiplexed (mode 0)
- 16-bit multiplexed (mode 1)
- 8-bit multiplexed (mode 2—AS, E, R/W#)
- 8-bit non-multiplexed synchronous (mode 3)
- 8-bit non-multiplexed asynchronous (mode 3)
- serial (SPI compatible)

This application note discusses both the 8- and 16-bit (Mode 0, Mode 1) multiplexed modes or "Intel modes", of the 82527.

3.0 82527 CLOCKING STRUCTURE

The operation of the 82527 is controlled by two clocks, the system clock (SCLK) and the memory clock (MCLK). The SCLK is derived from the external oscillator, while the MCLK is based off the frequency of the SCLK. The bit timings for all CAN bus communications are based on the frequency of the SCLK, while the MCLK provides clocking for all read and write operations to the 82527 RAM via the CPU(host)/82527 interface.

The frequency of the SCLK may be equal-to or one-half the external oscillator frequency and is defined by the value of the DSC bit in the CPU interface register. The maximum frequency of the SCLK is 10 MHz as specified in the March 1995 data sheet. An 8 MHz SCLK frequency is typically sufficient to interface the 82527 to a 1 Mbit/sec CAN bus.

The frequency of the MCLK may be equal-to or one-half the frequency of the SCLK, and is defined by the value of the DMC bit in the CPU interface register. The maximum frequency of the MCLK is 8 MHz, as specified in the March 1995 data sheet.

The 82527 contains two types of registers in the RAM; these are high speed registers (locations 02H, 04H, and 05H) and normal or low speed registers (all registers except 02H, 04H, and 05H). Read and write operations to the low speed registers occur over a synchronous internal bus which is clocked by the MCLK. High speed registers 02H, 04H and 05H are decoupled from the internal bus, allowing them to be accessed more quickly by the host-CPU. High speed read registers 04H and 05H are implemented for the double read operation, the double read operation may be needed when the host-CPU has no means to slow down its read cycle to accommodate the read access time specification of the 82527.

Please refer to the 82527 Architectural Overview (order number 272410-002) for additional information regarding the double read operation.

4.0 RECOMMENDED 20 MHz 8XC196/82527 INTERFACE (MODE 0/1)

A 20 MHz 8XC196 device (with a multiplexed address/data bus) may interface to an 82527 using three wait states. For modes 0/1, the generation of the chip select (CS#) signal may be accomplished through the use of combinatorial logic, an EPLD device, or where the 82527 is the only chip present on the bus, the CS# input may also be tied low (always enabled).

For applications where three wait state external memory access is sufficient, it is not required that the READY function be used to implement the required wait states. Programming an 8XC196 for 3 wait states (CCB configured) will force 3 wait states to be inserted for all external bus cycles until the READY pin is configured to operate in the special function mode of "READY". For applications requiring faster external memory accesses, the READY pin may be configured to control the maximum number of wait states inserted during an external memory fetch. In this case, it is recommended that an EPLD device be used to generate the chip select for the 82527 and provide control of the READY signal to the 8XC196.

For interfacing an 82527 to a 20 MHz 8XC196, the following configurations are recommended or required:

1. Program the 8XC196 Chip Configuration Bits (CCBs) for three wait states.
2. Configure the 82527 to operate within an 8 MHz SCLK (system clock) and 8 MHz MCLK (memory clock).
3. Configure the External Interrupt of the 8XC196 for servicing 82527 interrupt requests.
4. Select the implementation for chip select and ready control best suited for your design requirements. Section 7 contains three schematic examples for using either mode 0 or mode 1 of the 82527 to interface to an 8XC196.

4.1 Read Timings

The read timings of the 82527 are based on the frequency of the MCLK. These timings are also dependent upon the order of operations. In particular, when either a read or write cycle follows a write operation, the read access timings may increase. This additional delay is a result of the time required by the 82527 to complete the write operation (internally store the data) before beginning the subsequent read operation.

When interfacing a 20 MHz 8XC196 to an 82527 device, the condition of a "read cycle with a previous write" as defined in the 82527 data sheet is not possible, thus the faster read access timing

$$(t_{RLDV1} = 1.5\ t_{MCLK} + 100\ ns)$$

is applicable. This section will provide you with two methods for determining when the condition of a "read cycle with a previous write" exists.

To determine if a "read cycle with a previous write" is valid, consider t_{WHRL}, the time between the rising edge of WR# and the falling edge of RD#. If t_{WHRL} is less than 2 t_{MCLK}, then the read specification for t_{RLDV1} must be $t_{RLDV1} = 3.5\ t_{MCLK} + 100$ ns. If the value of t_{WHRL} is greater than 2 t_{MCLK}, then

$$t_{RLDV1} = 1.5\ t_{MCLK} + 100\ ns.$$

Another way of determining if a "read cycle with a previous write" is valid is to consider if

$$4\ t_{MCLK}\ (82527) \leq 10\ t_{XTAL}\ (8XC196).$$

If true, the faster 82527 read access timings of

$$t_{RLDV1} = 1.5\ t_{MCLK} + 100\ ns$$

should be used. Keep in mind this equation is not valid for PTS or BMOV instructions.

The 8XC196 is specified to meet the following timings.

t_{AVLL}—Address Valid to ALE Falling Edge	Tosc − 15 ns
t_{LLRL}—ALE Falling Edge to RD# Falling Edge	Tosc − 30 ns

The 82527 must meet the following system timings using *3 wait states.

t_{AVDV}—Address Valid to Data Valid	9 Tosc* − 55 ns

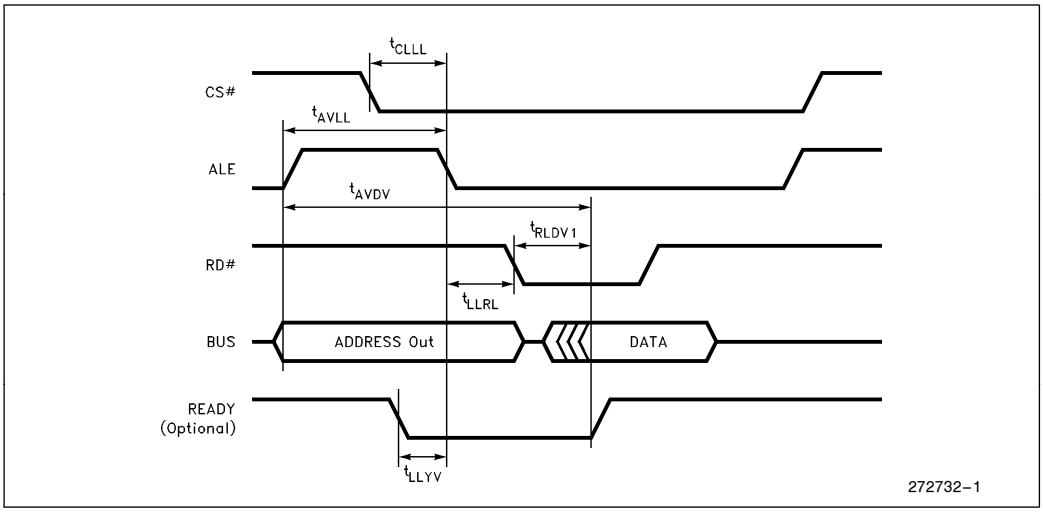
The following 82527 AC timings must be considered when interfacing to an 8XC196.

t_{RLDV1}—READ Falling Edge to Data Valid	1.5 t_{MCLK} + 100 ns

The 8XC196 requires the 82527 to drive valid data resulting from a read operation within 9 Tosc − 55 ns (w/3 wait states) following a valid address. After the 8XC196 provides a valid address, ALE will fall no sooner than Tosc − 15 ns, RD# will fall no sooner than Tosc − 30 ns after the falling ALE, and the 82527 will drive valid data no later than 1.5 t_{MCLK} + 100 ns following the RD# falling edge.

The following equation may be used to determine if the read timings are satisfied.

$$t_{AVDV} > t_{AVLL} + t_{LLRL} + t_{RLDV1}$$
(considering 3 wait state access)



Read Bus Timing Specifications

9 Tosc − 55 ns >
(Tosc − 15 ns) + (Tosc − 30 ns) + 1.5 t_{MCLK} + 100 ns

Tosc = 50 ns (8XC196 @ 20 MHz), t_{MCLK} = 125 ns
(82527 MCLK @ 8 MHz)

395 ns > 287.5 ns

4.2 Write Timings

The write timings of the 82527 are based on the frequency of the MCLK and the frequency of write operations, similar to the read timings. If a "write operation follows a previous write", the write access timings may increase.

The definition for a "write cycle with a previous write" as stated in the 82527 data sheet, is defined by t_{WHWH}, the time between the rising edge of WR# and the next rising edge of WR#. If t_{WHWH} is less than 2 t_{MCLK}, then a previous write is pending and the write timing specification of t_{WHYZ} (end of last Write to READY float) = 2 t_{MCLK} + 100 ns must be used. If t_{WHWH} is greater than 2 t_{MCLK}, then no previous write is pending, and the write timing specification is t_{WLYZ} (WR# low to READY float) = 145 ns.

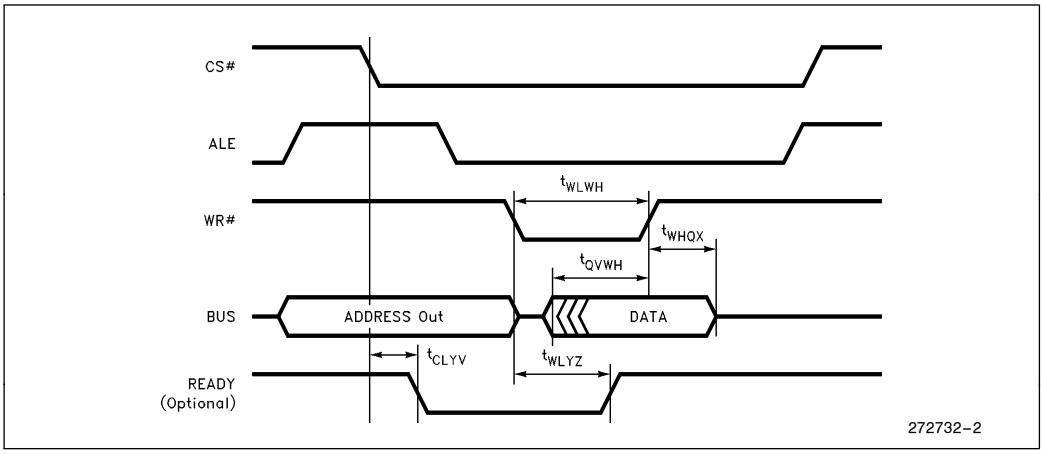
The following 8XC196 bus timings must be considered when interfacing to an 82527.

	8XC196KR	82527
t_{WLWH}—WR# Falling Edge to WR# Rising Edge (applies to zero wait-state writes only)	Tosc − 20 ns (30 ns)	30 ns
t_{WHQX}—Input Data Hold after WR# Rising Edge	Tosc − 25 ns (25 ns)	12.5 ns
t_{QVWH}—Data Setup to WR# Rising Edge	Tosc − 23 ns (27 ns)	27 ns

The timing comparisons are based on a write operation without a pending write, and are valid for a 20 MHz 8XC196 interfacing to an 82527. As described in the Read timings section, the calculation

4 t_{MCLK} (82527) ≤ 10 t_{XTAL} (8XC196)

may be used to determine if the condition of a "write cycle with a pending write" as specified in the 82527 data sheet is valid. Again, this equation is not valid for PTS or BMOV instructions.



Write Bus Timing Specifications

5.0 CHIP SELECT AND READY TIMINGS

As previously mentioned in systems where multiple devices reside on the external bus, the same logic used to derive the CS# signal to the 82527 may be used to generate the READY signal to the 8XC196. The READY output timings of the 82527 do not meet the READY setup specification for a 20 MHz 8XC196. Therefore, if the READY function is to be used, external logic capable of asserting READY within 25 ns of a valid address is required.

When the READY signal is used to control wait states, the READY signal timings of the 8XC196 must be met. A 20 MHz 8XC196 requires READY to be valid within 25 ns of a valid address. If this setup timing is not met, the 8XC196 will generate zero wait states and the read or write operation will not function properly.

The current 8XC196 Automotive data sheets specify two timing constraints which must be considered in order to insure wait states will be properly inserted into the external bus cycle. These specifications are t_{AVYV} and t_{LLYV}. The setup time for READY is given by the t_{AVYV} specification or the time from a valid address until the READY signal must be valid. In a typical design, READY is determined early in the bus cycle by decoding the address to generate the READY signal. The time to do this must be less than the READY setup time given by t_{AVYV}.

For most system designs, the t_{LLYV} specification is not needed and the t_{AVYV} specification should be used instead.

The following 8XC196 bus timings must be considered when interfacing to an 82527.

t_{AVYV}—Address Valid to READY Setup (Falling Edge)	2 Tosc − 75 ns
t_{AVLL}—Address Valid to ALE Falling Edge	Tosc − 15 ns

The following 82527 bus timing must be considered when interfacing to an 8XC196

t_{CLLL}—CS# Falling Edge to ALE Falling Edge	10 ns
t_{CLYV}—CS# Low to READY Setup	32 ns
(**Note:** C_L = 50 pF load capacitance)	V_{OL} = 1.0V
	40 ns
	V_{OL} = 0.45V

The chip select signal may be generated in the following ways.

- CS# may be connected to an 8XC196 address line. This method dedicates one-half of the 8XC196 external address space to servicing the 82527. For a 16-bit interface, this implementation also requires the use of a pass-through latch to latch the high order address to generate a CS# signal. The logic used to generate the chip select signal must have a propagation delay of 25 ns or less.

If READY control is required:

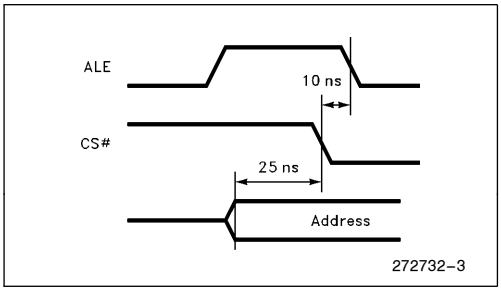
- The chip select line may be generated with combinatorial logic or an EPLD device which decodes the high address byte. If READY control is required, the logic used for generating READY must have a propagation delay of 25 ns or less. The advantage of this implementation is a smaller portion of the 8XC196 external address range is used to access the 82527.

For a basic interface:

- CS# may also be tied low (always enabled). This interface requires the 82527 be the only device on the external address/data bus. The entire external address range of the 8XC196 becomes dedicated to servicing the 82527.

The chip select signal to the 82527 must be valid 10 ns before ALE falls, as defined by the t_{CLLL} specification. Chip select generation begins when the 8XC196 sends a valid address prior to ALE falling (t_{AVLL}). The equation to calculate the time to generate the 82527 chip select is.

CS# generation < t_{AVLL} − t_{CLLL}
CS# generation < (Tosc − 15 − (10)
CS# generation < 25 ns

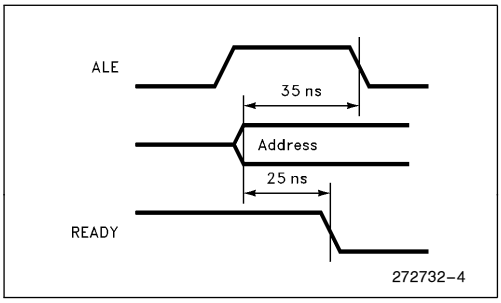


82527 CS# Setup Timing Requirements

The READY signal to the 8XC196 must be generated within t_{AVYV}. This means that READY must be valid within the READY setup time with respect to a valid address. An alternative set-up time can be calculated using the t_{LLYV} specification.

The equation to calculate the time to generate READY is:

READY generation < t_{AVYV}
READY generation < (2 Tosc − 75)
READY generation < 25 ns



20 MHz 8XC196 READY Timing Requirements

6.0 COMPARISON OF 20 MHz 8XC196 AND 82527 AC TIMINGS

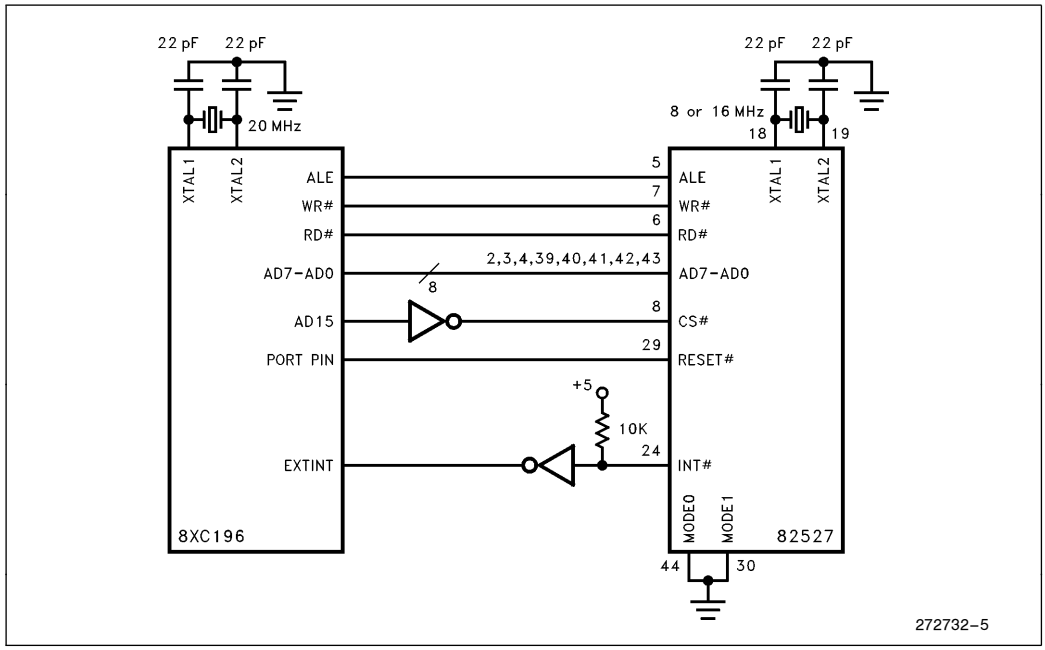
Timings the C196 must satisfy (Automotive Specifications(4))				**March 95**
Tosc = 50 ns, all timings are in ns.		**8XC196**	**82527**	**20 MHz**
t_{AVLL}	Address Valid to Falling ALE	Tosc − 15 min	7.5	35
t_{LLAX}	Address Hold after ALE Falling	Tosc − 40 min	10	10
t_{LHLL}	ALE High Period	Tosc − 10 min	30	40
t_{LLRL}	ALE Falling to RD# Falling	Tosc − 30 min	20	20
t_{CLLL}	CS# Falling to ALE Falling	(Note 1)	10	
t_{QVWH}	Data Stable to WR# Rising	Tosc − 23 min	27	27
t_{WHQX}	Data Hold after WR# Rising	Tosc − 25 min	12.5	25
t_{WLWH}	WR# Low Period	Tosc − 20 min	30	30
t_{WHLH}	WR# Rising to ALE Rising	Tosc − 10 min	8	40
t_{WHCH}	WR# Rising to CS# Rising	(Note 1)	0	
t_{RLRH}	RD# Low Period	Tosc − 10	40	40
Timings the 82527 Must Satisfy				
t_{RLDV}(2)	RD# Falling to Data Valid			
	High Speed Registers	Tosc − 22 min	55 max	28
t_{RHDZ}	RD# Rising to 82527 Data Float	Tosc	45 max	50
t_{AVDV}	Address Valid to Data Valid			
	3 Wait States	9 Tosc − 55 max	287.5	395
t_{AVYV}(3)	Address Valid to READY Setup	2 Tosc − 75 max	32	25

NOTES:
1. This is not a specific C196 specification, however using a latched C196 address.
2. The C196 is programmed for 3 wait states. In this case t_{AVDV} is the relevant timing.
3. The 82527 does not meet the READY setup requirement of the 8XC196 @ 20 MHz. If READY is to be used to control wait states, external logic capable of meeting the 8XC196 READY setup is required.
4. The timings comparison uses the current Automotive data sheets for an 8XC196 and 82527 device.

7.0 INTERFACING SCHEMATICS FOR MODE 0/MODE 1

The next three pages contain schematic diagrams illustrating possible bus interfaces between the 8XC196 and 82527. These diagrams are intended to provide a reference for designing an interface best suited to the goals of your project. The pin number information provided for the 82527 pertains only to the 44-ld PLCC package version.

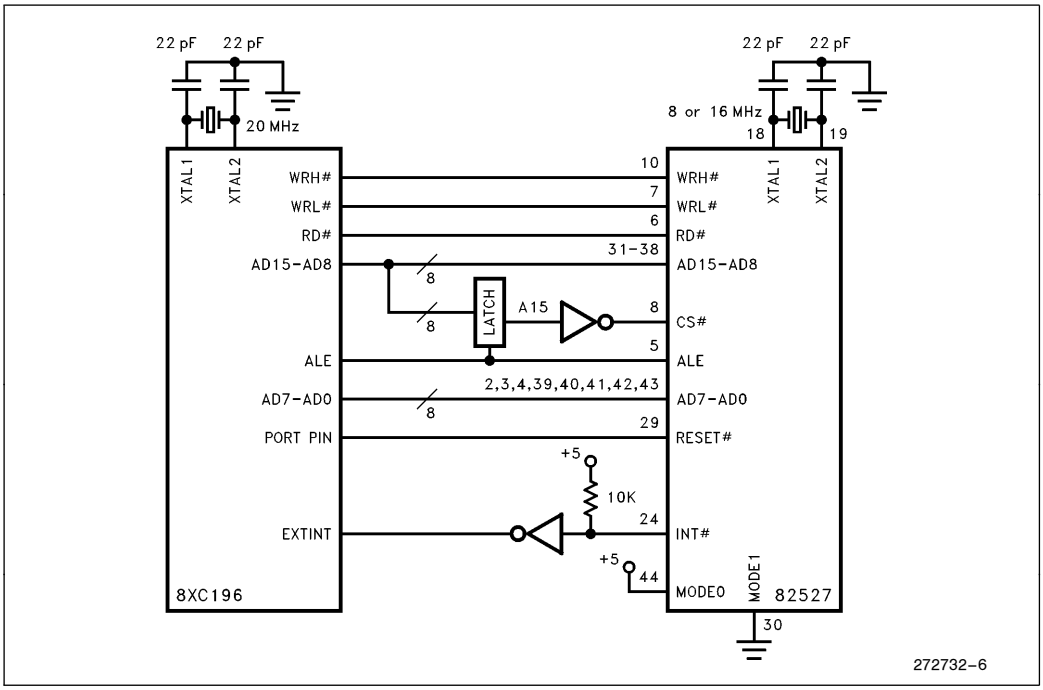
7.1 Mode 0, 8-Bit Multiplexed Interface



8XC196 to 82527 8-Bit Mode 0 Multiplexed Interface

The above diagram demonstrates an 8XC196 with an 8-bit multiplexed external address/data bus interfacing to the 82527. The 82527 is configured for 8-bit multiplexed mode 0. The CS# signal is derived from the high order address line A15. The RESET# signal for the 82527 is generated using an available port pin on the 8XC196, this signal may also be derived by an RC network. The reset pin on the 82527 must be driven low for a minimum of 1 ms after V_{CC} is in the operating range to guarantee a proper device reset. The 8XC196 must be programmed for 3 wait state external bus cycles. The function of P5.4/READY must be LSIO, and not READY, else external logic will be required to generate READY for the 8XC196 (refer to section 5.0). Both devices are clocked by Quartz crystals, please consult the crystal manufacturer specifications for proper load capacitance.

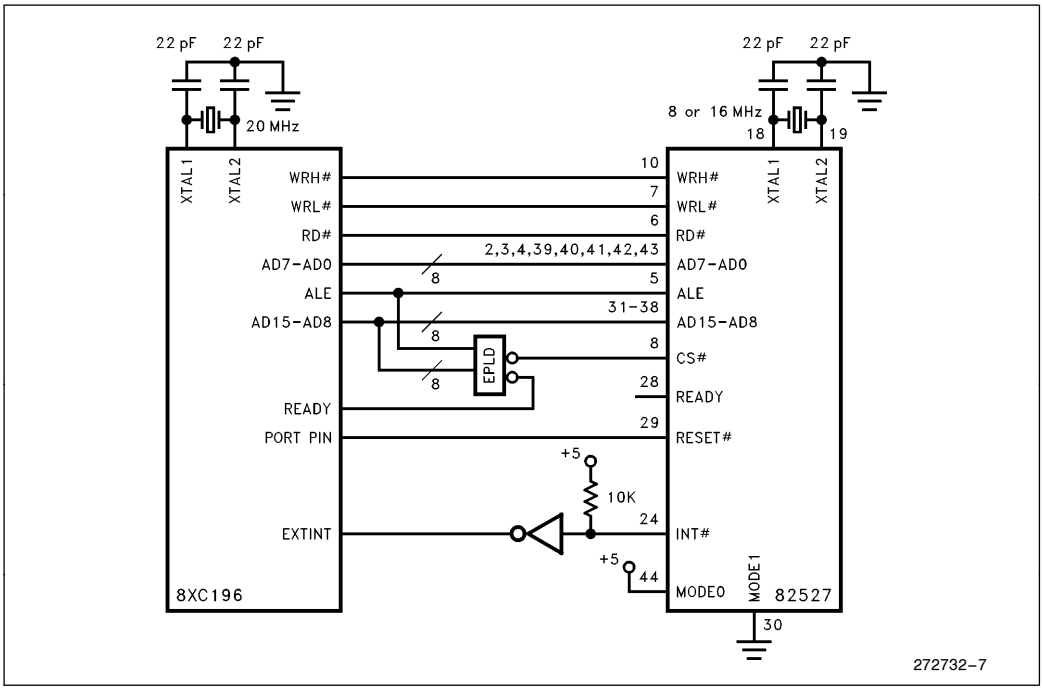
7.2 Mode 1, 16-Bit Multiplexed Interface



8XC196 to 82527 16-Bit Mode 1 Multiplexed Interface

This schematic demonstrates a 16-bit interface between the 8XC196 and the 82527. This implementation utilizes a pass-through latch and inverter to generate the chip select for the 82527 from the high order address information. The maximum propagation delay of the combinatorial logic used to generate the chip select for the 82527 is 25 ns (refer to section 5.0). No READY control is implemented, thus the 82527 is assumed to be the only device residing on the bus, or all external access are assumed to be 3 wait state accesses. The 8XC196 is programmed for 3 wait state external access. The 82527 RESET is implemented using an available port pin from the 8XC196, the reset signal may also be generated using an RC network. The 8XC196 bus control mode is set to Write Strobe mode, this is defined by the CCB's. Standard Bus-control mode may also be used as long as external logic is used to generate the WRL# and WRH# signals to the 82527. The INT# output of the 82527 is an open-drain output, a 10 KΩ external pull-up resistor is sufficient.

7.3 Mode 1, 16-Bit Multiplexed Interface w/READY



8XC196 to 82527 16-Bit Mode 1 Multiplexed Interface with Ready Control

This is another example of a 16-bit interface between the 8XC196 and the 82527. This interface uses an EPLD device to generate the chip select to the 82527 and the READY signal to the 8XC196. Both the CS# and READY setup times must be met to insure proper operation (refer to section 5.0). The 8XC196 is programmed for 3 wait state external access. The 82527 RESET is implemented using an available port pin from the 8XC196, the reset signal may also be generated using an RC network. The 8XC196 bus control mode is set to Write Strobe mode, this is defined by the CCB's. Standard Bus-control mode may also be used as long as external logic is used to generate the WRL# and WRH# signals to the 82527. The INT# output of the 82527 is an open-drain output, a 10 KΩ external pull-up resistor is sufficient. This implementation allows a smaller address range to be defined for providing access the 82527. In addition, control of the READY signal allows for wait state control when addressing other external devices which may reside on the bus.