



AB-45

**APPLICATION
BRIEF**

**Converting from the 8X9XBH
or 8X9XJF to the 8XC196KB**

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1.0 INTRODUCTION

The 8XC196KB is upward compatible with the 8X9XBH and 8X9XJF. The 8XC196KB maintains the same architecture, instruction set and peripheral set as the 8X9XBH and 8X9XJF. It also provides increased performance with lower power consumption and enhanced features.

The purpose of this document is to aid designers who are moving from the 8X9XBH or the 8X9XJF to the 8XC196KB. It assumes a thorough understanding of the 8X9XBH or the 8X9XJF. This document will only identify the differences between the 8X9XBH and 8X9XJF and the 8XC196KB. For more information on any differences consult the current Embedded Micro-controllers and Processors handbook and corresponding data sheets.

For the remainder of this document, the 8X9XBH will be referred to as the "BH", the 8X9XJF as the "JF", and the 8XC196KB as the "KB". Unless otherwise noted, all references to the BH also apply to the JF.

2.0 MEMORY MAP

ON-CHIP ROM/EPROM-The BH ROM and EPROM devices have 8 Kbytes of on-chip memory. The JF has 16 Kbytes. The KB has 8 Kbytes.

ON-CHIP RAM-The BH has 232 bytes of register RAM. The JF has 232 bytes of register RAM plus 256 bytes of executable internal RAM (code RAM). The KB has 232 bytes of register RAM.

RESERVED LOCATIONS-The KB uses some of the reserved locations to support new features.

WINDOW SELECT REGISTER-The Window Select Register on the KB uses a windowing scheme to expand the SFR space to support new features and make the SFR's readable and writable. The available windows are Window 0, Window 14 and Window 15.

3.0 CCB

CCB BIT 0-The KB uses bit 0 in the CCB to enable/disable Power Down mode. This bit is reserved on the BH.

4.0 INSTRUCTIONS

NEW INSTRUCTIONS-There are 6 new instructions on the KB:

1. PUSHA
2. POPA
3. IDLPD
4. CMPL
5. BMOV
6. DJNZW

EXECUTION TIMES-There are 3 oscillator periods per state on the BH. There are 2 oscillator periods per state on the KB. This decreases the instruction execution time. Also, many instructions on the KB require fewer states than on the BH. Timing loops based on instruction execution times should be recalculated for the KB.

FLAGS-The DIV and DIVB instructions leave the overflow flag undefined on the BH. The flag is set or cleared as appropriate on the KB.

5.0 STACK POINTER

OPERATIONS RELATIVE TO THE STACK POINTER (SP)-For indexed and indirect operations relative to the stack pointer (SP), the address is calculated using the un-updated version of the stack pointer on the BH. The KB uses the updated version. For example, the offset for LD TEMP, [SP] and LD TEMP, nn[SP] instructions may need to be changed by a count of 2.

6.0 INTERRUPTS

SHARED INTERRUPTS-On the BH, interrupt vector locations were shared for the RI and TI interrupts, HSI Data Available and HSI FIFO Full interrupts, EXTINT and ACH.7 interrupts, and Timer1 and Timer2 overflow interrupts. The KB supports this interrupt structure and also provides separate interrupts for each event, available under software control.

NEW INTERRUPTS-The KB supports the following new interrupts:

- NMI
- TRAP
- Unimplemented Opcode
- EXTINT1
- Timer2 Capture
- HSI4 (4 or more entries in FIFO)

NMI-On the BH, NMI vectors directly to location 0000H. On the KB it vectors through location 203EH. To be compatible with the BH location 203EH must be loaded with 0000H.

NEW STATUS REGISTERS-The KB has INT_PEND1 and INT_MASK1 registers to support the new interrupts.

PRIORITIES-The original interrupts have the same relative priorities on the KB as on the BH. However, the new interrupts all have higher priority than the original interrupts.

PUSHA AND POPA-The KB has two new instructions, PUSHA and POPA, to save the PSW, INT_MASK, INT_MASK1 and WSR on the stack.

INSTRUCTIONS WHICH INHIBIT INTERRUPTS-On the BH the EI, DI, POPF and PUSHF instructions and SIGND, the signed prefix for multiply and divide instructions, inhibit interrupts from being acknowledged until after the next instruction has been executed. On the KB the PUSHA, POPA and TRAP instructions also do this.

INTERRUPT LATENCY-Maximum interrupt latency on the BH is 70 states. This includes 42 states for execution of the longest instruction (NORML) and 24 states for the response time. On the KB the maximum interrupt latency is 61 states. This includes 39 states for the NORML instruction and 18 states for response time.

7.0 PWM

PWM PERIOD-The period of the PWM output is 256 states on the BH. On the KB the pulse width can be 256 states or 512 states, as selected in software.

READING THE PWM-The PWM register can be read on the KB in Window 15.

PWM TIMINGS-The state times of the KB are shorter than the BH. For PWM outputs which require exact timings you may need to recalculate the PWM register value.

8.0 TIMER1

TIMINGS BASED ON TIMER1-The state times on the KB are different than the BH. Any timings based on Timer1 should be recalculated for the KB.

WRITING TO TIMER1-On the BH Timer1 can be changed by writing to location 0CH. Writing any value to location 0CH will set the Timer1 and Timer2 to 0FFFFH. On the KB Timer1 can be programmed by writing to location 0AH in Window 15. This will set Timer1 to the value written to 0AH.

9.0 TIMER2

MAXIMUM TRANSITION SPEED-On the BH the maximum transition speed of inputs to Timer2 is once per eight state times. The maximum transition speed on the KB is once per eight state times in normal mode and once per state time in Fast Increment Mode.

COUNTING UP AND DOWN-Timer2 on the BH only counts up. Timer2 on the KB can count up or down.

T2 OVERFLOW INTERRUPTS-On both devices an overflow on Timer2 can cause an interrupt. The KB can also interrupt when Timer2 crosses the 7FFFH/8000H boundary. An overflow interrupt vectors to location 2000H on the BH. On the KB a Timer2 overflow interrupt can vector to location 2000H or 2038H, as selected in software.

TIMER2 CAPTURE-On the KB the value in Timer2 can be captured into the T2CAPTURE register. A Timer2 Capture can generate an interrupt.

WRITING TO TIMER2-On the BH Timer2 can be changed by writing to location 0CH. Writing any value to 0CH will set Timer1 and Timer2 to 0FFFFH. On the KB Timer2 can be programmed by writing to location 0CH in Window 0. This will set Timer2 to the value written to 0CH.

10.0 HSI

INTERRUPTS-The BH can generate an interrupt when either the HSI Holding Register contains data or the FIFO contains 6 entries. Both interrupts vector to the same location. The KB, under software control, can vector to the same location for each or to separate locations. The KB can also generate an interrupt when the FIFO contains four entries.

READING AND WRITING THE CONTROL REGISTERS-The HSI_STATUS and HSI_TIME registers can be written to and IOC0 and IOC1 can be read in Window 15 on the KB.

11.0 HSO

LOCKED CAM ENTRIES-HSO entries on the KB can be locked into the CAM. They will occur continually without having to reload the CAM.

CLEARING THE CAM-The entire HSO CAM can be cleared without resetting the device on the KB.



STATUS REGISTERS-Status registers on the BH show the current state of the HSO pins and which software timer has interrupted. In addition to these, a new status register is provided on the KB to show which HSO pins have transitioned, if a Timer2 reset has occurred, or if an A/D conversion has started.

READING AND WRITING THE CONTROL REGISTERS-IOS0, IOS1 and IOS2 can be written to and HSO_COMMAND, HSO_TIME and IOC1 and IOC2 can be read in Window 15 on the KB.

12.0 SERIAL PORT

FLAGS-The KB has three new serial port flags:

- FE—Framing Error Flag
- TXE—Transmitter Empty Flag
- OE—Receive Overflow Flag

SP_STAT-SP_STAT supports the new flags on the KB:

KB SP_STAT							
7	6	5	4	3	2	1	0
RB8/ RPE	RI	TI	FE	TXE	OE	X	X

CLEARING THE FLAGS-On both devices, RI and TI are cleared every time SP_STAT is read. FE and OE are also cleared on the KB. On the KB TXE is also cleared after a transmission.

INTERRUPTS-On the BH the RI and TI interrupts both vector to the same location. The KB, under software control, can vector to the same location for each or to separate locations.

BAUD RATES-The formulas to calculate the baud rate are different on the BH and KB.

READING AND WRITING THE CONTROL REGISTERS-SP_STAT can be written and SP_CON can be read in Window 15 on the KB.

13.0 A/D

CONVERSION TIMES-The BH takes 88 states to complete a conversion. This corresponds to 22 μ s at 12 MHz. Because the KB can operate over a wider frequency range, a prescaler can be enabled to adjust the speed of the A/D. The KB takes 91 states to complete a conversion with the prescaler off (22.75 μ s at 8 MHz) and 158 states with the prescaler on (26.33 μ s at 12 MHz, 19.75 μ s at 16 MHz).

SAMPLE WINDOW-The BH has a 4 state sample window. The KB has an 8 state time window with

the prescaler off and 15 state sample window with the prescaler on.

14.0 EPROM PROGRAMMING

PROGRAMMING MODES-The KB does not support gang programming using a KB as the master programmer. The programming control signals needed for this mode do not exist on the KB.

PROGRAMMING SIGNALS-The PACT (programming active) signal is multiplexed with HSO.0 on the BH. It is multiplexed with P2.7 on the KB. The KB multiplexes P2.4 with AINC (auto increment signal). Auto increment does not exist on the BH.

PROGRAMMING PULSE WIDTH REGISTER-The KB has a Programming Pulse Width Register (PPW) to determine the width of the programming pulse in the Auto, Auto PCCB and Run-time Programming Modes.

AUTO PROGRAMMING MODE-On the KB in the Auto Programming Mode, the PPW value must be loaded into external location 4014H before the Programming Mode is entered.

SLAVE PROGRAMMING MODE-On the BH in the Slave Programming Mode, the data verify or word dump command must be issued for each address. On the KB the AINC signal can be used to automatically increment the addresses without issuing another command.

RUN-TIME PROGRAMMING-On the BH using run-time programming, the programming pulse width must be programmed in software using a software timer. A “Jump to Self” loop is recommended during programming. On the KB, the PPW controls the programming pulse width. Idle Mode is recommended instead of the “Jump to Self”.

ROM DUMP MODE-The ROM Dump Mode is entered the same way on the BH ROM and EPROM and on the KB EPROM. The KB ROM enters the mode differently. On the BH, ROM Dump Mode places indeterminate data at addresses 9000H–91FFH. No data is placed at these addresses on the KB.

SIGNATURE WORDS-The KB contains two words following the Signature Words which can be used to determine the programming voltage.

READ AND WRITE LOCK BITS-On the BH in the Auto, Auto PCCB, and Slave Programming Modes, if either the READ or the WRITE lock bits are programmed in the CCB the device cannot be programmed or verified. On the KB, if either bit is programmed, the device will do a security key verification. If the keys match, the device can be programmed and verified.



AC AND DC SPECS-The AC and DC EPROM Programming Characteristics are different for the BH and the KB. Consult the current data sheets for the specifications.

15.0 PINOUT/PIN FUNCTIONS

PIN COMPATIBILITY-The KB is pin compatible with the BH with one exception. Pin 64 (on the PGA package, pin 14 on the PLCC package) is V_{PD} on the BH. On the KB this pin is V_{SS}.

NEW PIN FUNCTION-Several pins have new additional functions on the KB. These pins are listed below.

BH Pin/Function	KB Pin/Function
P2.4/T2RST	P2.4/T2RST/AINC
P2.7/PACT	P2.7/PACT/T2CAPTURE
P2.6	P2.6/T2UP-DN
P1.7	P1.7/ $\overline{\text{HOLD}}$
P1.6	P1.6/HLDA
P1.5	P1.5/ $\overline{\text{BREQ}}$

16.0 MINIMUM HARDWARE CONSIDERATIONS

UNUSED PINS-All unused input pins on the KB must be tied high or low. No input pins can be left floating.

V_{pp}-V_{pp} must be left floating on BH EPROM devices. It must be tied to V_{CC} on all KB devices.

17.0 RESET

INTERNAL RESET TIMING-An internal reset on the BH (software reset or watchdog timer reset) will hold the RESET pin low for at least one state. On the KB, it will hold the RESET pin low for four states.

EXTERNAL RESET TIMING-To externally reset the BH the RESET pin must be held low for at least 10 XTAL1 cycles. The RESET pin must be held low for at least 4 states on the KB.

CAPACITOR ON RESET PIN-If a capacitor between RESET and V_{SS} is used to reset the device, the recommended size of the capacitor is different for the KB.

STATUS DURING RESET-The status of the control registers and the I/O pins during RESET are different on the BH and the KB. Consult the current Embedded Microcontrollers and Processors Handbook for detailed information.

18.0 EXTERNAL MEMORY INTERFACING

AC TIMINGS-The AC Timings for bus operations are different for the BH and the KB. Consult the current data sheets for specifications. Both devices will function with standard ROM/EPROM/Peripheral type memory systems.

$\overline{\text{HOLD}}$ /HLDA-The KB supports a bus exchange protocol ($\overline{\text{HOLD}}$ /HLDA) to allow other devices to gain control of the bus.

19.0 MODES

ENTERING AND EXITING POWERDOWN-Powerdown is entered and exited differently on the BH and the KB.

RAM IN POWERDOWN-The BH maintains the upper 16 bytes of RAM in powerdown mode. The KB maintains all the SFR's, all 232 bytes of RAM and most of the peripherals.

DISABLING POWERDOWN-Powerdown mode can be disabled on the KB.

NEW MODES-The KB has two new modes—Idle and ONCE modes.

20.0 POWER CONSUMPTION

POWER CONSUMPTION-Power consumption on the KB is about 1/10 that of the BH. See the current data sheets for the I_{CC}, I_{IDLE} and I_{PD} specifications.

21.0 DC CHARACTERISTICS

DC SPECS-The DC characteristics on the BH are different than those of the KB. Consult the current data sheets for specifications.

22.0 BH, KB ERRATA

STATUS OF BH, JF AND JF KB ERRATA-Consult the current data sheets for detailed information on BH and KB errata.

23.0 PACKAGES

AVAILABLE PACKAGES-Consult the current data sheets for the available packages.

