87C51

SPECIFICATION UPDATE

Release Date: July, 1996

Order Number 272884-001

The 87C51may contain design defects or errors known as errata. Characterized errata that may cause the 87C51's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333 other Countries 708-296-9333

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 87C51 Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270646-007
MCS®-51 Microcontroller Family User's Manual	272383-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 87C51 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	#	#	#			
						None for this revision of this specification update.

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	D#	#	#			
001	X			9		Asynchronous Port Reset
002	X			9		Four Interrupt Priority Levels
003	X			10		Power Off Flag
004	X			10		ALE Disable
005	X			10		Serial Port Automatic Address Recognition
006	X			11		Serial Port Framing Error Detection
007	X			12		Program Memory Lock
008	X			13		Lock Bit/Encryption Array Programming
009	X			15		Signature Bytes

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

D-step devices can be identified by the letter “A” following the eight-digit FPO number on the top of the package.

ERRATA

None for this revision of this specification update.

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. Asynchronous Port Reset

PROBLEM: In order to reset the current 87C51 C-step port pins, the oscillator must be running. At least 19 oscillator periods must occur after a logic 1 is applied to the RST input before the pins are driven to their reset state.

On the new D-step, the clock does not have to be running for the ports to assume their reset value. The port pins are driven to their reset state as soon as a valid high is applied to the RST pin.

AFFECTED PRODUCT: D-step devices.

002. Four Interrupt Priority Levels

PROBLEM: A second Interrupt Priority register (IPH) has been added allowing four priority levels. The figure below shows this second register. The added register becomes the MSB of the priority select bits and the existing IP register acts as the LSB. Table 1 shows the bit values and priority levels associated with each combination.

IPH Address = 0B7H Reset Value = X000 0000

---	PPCH	PT2H	PSH	PT1H	PX1H	PTOH	PXOH
7	6	5	4	3	2	1	0

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IPL.x	
0	0	Level 0 (Lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (Highest)

Table 1. Priority Level Bit Values

AFFECTED PRODUCT: D-step devices.

003. Power Off Flag

PROBLEM: The Power Off Flag (POF), bit 4 in special function register PCON (PCON.4), is set by hardware when Vcc rises from 0 to 5 volts. POF can also be set or cleared by software. Checking the bit status allows the user to distinguish between a "cold start" reset and a "warm start" reset. Vcc must remain above 3 volts for POF to retain a 0.

AFFECTED PRODUCT: D-step devices.

004. ALE Disable

PROBLEM: If desired, ALE operation can be disabled when executing internal program code by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX instruction. Otherwise, the pin is weakly pulled high.

AFFECTED PRODUCT: D-step devices.

005. Serial Port Automatic Address Recognition

PROBLEM: When enabled, the automatic address recognition feature allows the Receive Interrupt (RI) flag to be set only when the received byte corresponds to either a Given or Broadcast address.

To enable the feature, bit SM2 in the SCON special function register must be set. If SM2 = 1 in modes 2 or 3, RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast address. If SM2 = 1 in mode 1, RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast address.

The Given address is specified by the contents of two new special function registers: SADDR (0A9H) and SADEN (0B9H). The UART's individual address is defined in SADDR. SADEN is a mask byte that defines don't cares in the given address. The broadcast address is specified by the logical OR of SADDR and SADEN with zeros defined as don't cares. The following example illustrates how the two registers specify an address.

SADDR (UART Address)	0 1 0 1 0 1 1 0
SADEN (Address Mask)	1 1 1 1 1 1 0 0
Given Address	0 1 0 1 0 1 X X
Broadcast Address	1 1 1 1 1 1 1 X

The new feature maintains compatibility with the existing scheme. On reset, the SADDR and SADEN registers are initialized to 00H. This defines the Given address and Broadcast address to be XXXX XXXX (all don't cares).

AFFECTED PRODUCT: D-step devices.

006. Serial Port Framing Error Detection

PROBLEM: Framing Error Detection allows the serial port to check for valid stop bits in modes 1, 2, and 3. A missing stop bit can be caused, for example, by noise on the serial lines, or transmission by two CPUs simultaneously.

If the stop bit is missing, a Framing Error (FE) bit is set. The FE bit can be checked in software after each reception to detect communication errors. Once set, the FE bit must be cleared in software. A valid stop bit will not clear the FE bit.

The FE bit is located in SCON and shares the same bit address as SM0. A new control bit in the PCON register, SMOD0 (location PCON.6), determines whether the SM0 or FE bit is accessed. If SMOD0 = 0, accesses to SCON.7 are to SM0. If SMOD0 = 1, accesses to SCON.7 are to FE. The PCON and SCON registers are shown below with the new bits added.

PCON Address = 087H Reset Value = 000X 0000

SMOD1	SMOD0	---	POF	GF1	GF0	PD	IDL
7	6	5	4	3	2	1	0

SMOD1: SMOD1 is the same as SMOD of the C step.

SMOD0: '0' - access to SCON.7 is to SM0 '1' - access to SCON.7 is to FE

SCON Address = 098H Reset Value = 0000 0000

SM0 / FE	SM1	SM2	REN	TB8	RB8	TI	RI
7	6	5	4	3	2	1	0

FE: set to '1' when a framing error occurs in UART

To maintain compatibility with C-step devices, the SMOD0 bit is initialized to '0' on reset, directing any SCON.7 accesses to SM0.

AFFECTED PRODUCT: D-step devices.

007. Program Memory Lock

PROBLEM: The 87C51 D-step now offers a three-level program lock system and a 64-byte Encryption Table. Table 2 lists the Lock Bits and their corresponding influence on the controller. Consult Table 3 for the signals required to program the lock bits and encryption array. Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full functionality.

	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on reset, and further programming of the EPROM is disabled
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Table 2. Lock Bits

AFFECTED PRODUCT: D-step devices.

008. Lock Bit/Encryption Array Programming

PROBLEM: With the addition of a third lock bit and 32 more encryption bytes, a need to program these features becomes necessary. Table 3 indicates the configuration required to program the additional protection features.

Mode	RST	PSEN	ALE/PROG	EA/Vpp	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code	H	L	L*	Vpp	L	H	H	H	H
Verify Code	H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0-3FH	H	L	L*	Vpp	L	H	H	L	H
Bit 1	H	L	L*	Vpp	H	H	H	H	H
Program Lock Bits Bit 2	H	L	L*	Vpp	H	H	H	L	L
Bit 3	H	L	L*	Vpp	H	L	H	H	L
Read Signature Byte	H	L	H	H	L	L	L	L	L

Table 3. EPROM Programming Modes

Vpp = +12.75V +/- 0.25V

* ALE/PROG is pulsed low for 100 us for programming

AFFECTED PRODUCT: D-step devices.

009. Signature Bytes

PROBLEM: One signature byte has been added increasing the total number of signature bytes to three. To read these bytes, follow the procedure for EPROM verify, but activate the control lines provided in Table 3 for Read Signature Byte. The table below shows the location and contents of each signature byte.

Location	Contents
30H	89H (Intel device)
31H	58H (FX-core product)
60H	51H (87C51)

AFFECTED PRODUCT: D-step devices.

DOCUMENTATION CHANGES

None for this revision of this specification update.