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APPLICATION BRIEF

Interfacing the 82786 Graphics Coprocessor to the 8051

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INTERFACING THE 82786 GRAPHICS COPROCESSOR TO THE 8051

CONTENTS

Interfacing the 82786 to the 8051 presents some interesting challenges, but can be accomplished with a little additional logic and software. Since the 82786 looks like a DRAM controller to the host CPU, wait states are often required when accessing the coprocessor. Since wait states are not supported by the 8051, latching transceivers and dummy read and write cycles are used to communicate with the 82786. Byte swapping is also required in the external logic to allow the 8 bit 8051 to read and write the 16 bit graphics memory supported by the 82786. This byte swapping is accomplished with the latching transceivers as well. All of the control logic is implemented in an Intel 5C060 EPLD, allowing the entire interface to fit into three 24 pin DIPs.

HARDWARE

Figure 1 shows the interface between the 8051 bus and the 82786. Figure 2 shows a typical 8051 CPU design needed to complete the circuit. In this design the 82786 is mapped into an 8K byte window in 8051 data memory space. The upper address bits are used as a "page select" and are provided by I/O pins on the 8051. The 5C060 EPLD contains the control logic for the transceivers and address decoding for the 82786. An equivalent circuit for the EPLD is shown in Figure 3; the ".ADF" file is shown in Figure 4. The 82786 data memory is mapped into one 8K block (A000H–BFFEH), the 82786 registers are mapped into another (8000H–807EH), and the transceivers are mapped into a third block of memory (C000H–C001H).

OPERATION

Operation of the interface is as follows. For reading the graphics memory, the 8051 sets the upper address bits (PORT 1.0–1.3) and then performs a dummy read operation to the desired location in graphics memory (A000H thru BFFEH). The dummy read cycle provides the address and RD/WR information to the 82786, which runs a cycle and deposits the 16 bit result into the latching transceivers at the end of the read cycle, as indicated by SEN. This event clears the BUSY flip flop in the EPLD. When the BUSY signal goes inactive, the 8051 reads the low byte from the latching transceiver at address C000H and the high byte free address C001H.

For write cycles, the 8051 writes the low byte of the word into the latch at address C000H and the high byte into address C001H. Next the upper address bits are set with PORT1 and a dummy write cycle is performed in graphics memory at the desired address (A000H–BFFEH). Like in the read example, the 82786 runs a memory cycle at this point, enabling the outputs of the latching transceivers at the proper time in the write cycle, as indicated by SEN going active.

Accessing the registers inside the 82786 is done in exactly the same fashion, except that the 82786 is addressed in locations 8000H through 807EH. This causes the EPLD to drive the M/IO pin low during these cycles.

DESIGN NOTES

74F543's are used for the latching transceivers in this design, although 74HCT646's could be used to reduce the total power consumption. Some changes to the EPLD would be required in this case. The interface assumes that all memory accesses to the 82786 are word references; accordingly, BHE is grounded at the 82786. All addresses generated by the 8051 must be even byte addresses, the only byte operations allowed are the reads and writes to the latching transceivers. The design shown here incorporates hardware workarounds for the earlier "C-step" 82786; the current "D-step" part will work in the design as well. Additional information regarding the 82786 can be found in the "82786 Graphics Coprocessor User's Manual", Intel publication number 231933.

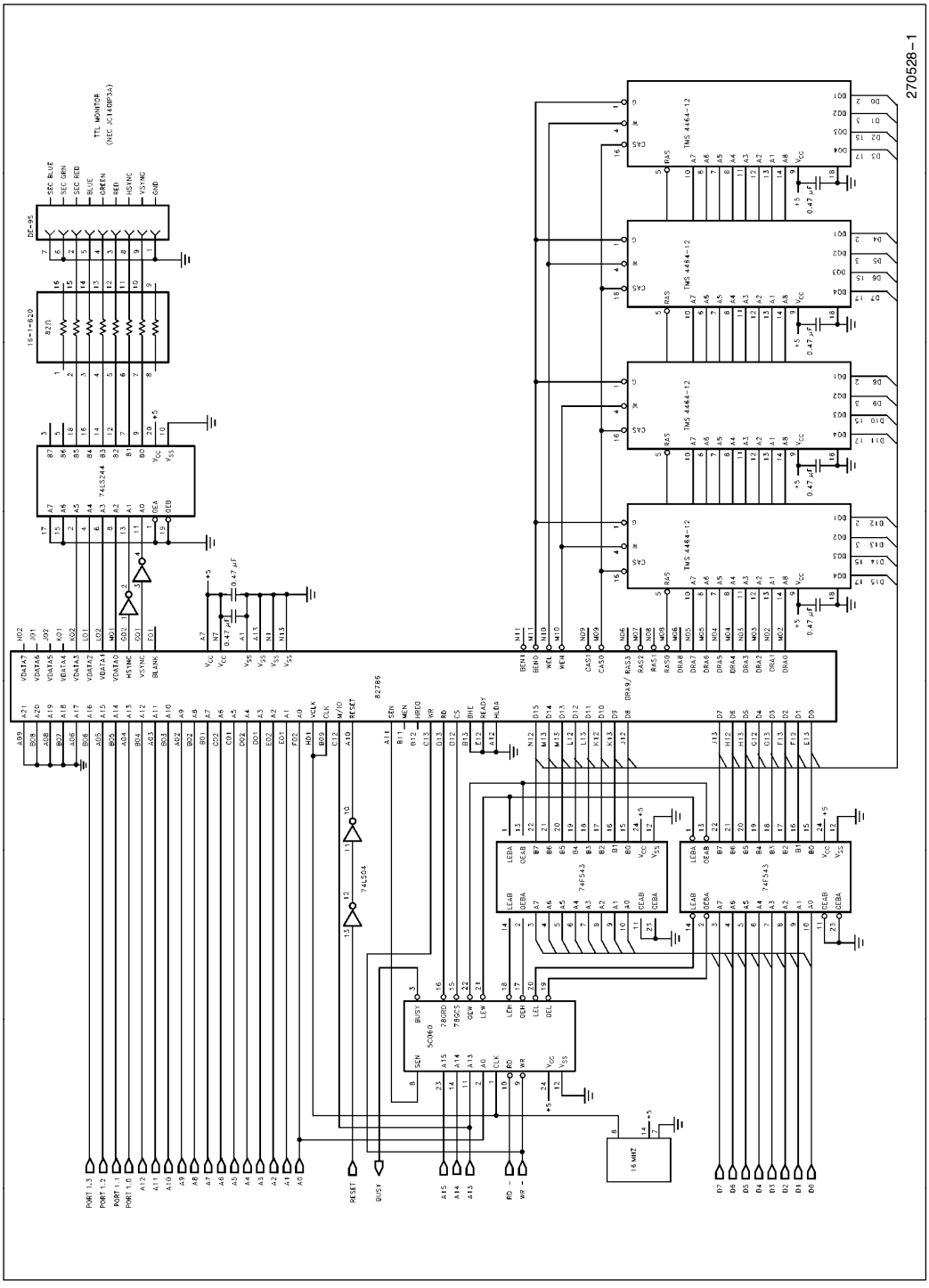
270528-1
TTL MONITOR
(NEC JC1402P34)
DE-9S
SEC BLUE
SEC GRN
SEC RED
BLUE
GREEN
RED
HSYNC
VSYNC
GND
16-1-820
82Ω
74LS244
TMS 4464-12
0.47 µF
82786
74S04
74F543
16 MHZ
PORT 1.3
PORT 1.2
PORT 1.1
PORT 1.0
RESET
BUSY
RD –
WR –
D7
D6
D5
D4
D3
D2
D1
D0

Figure 1

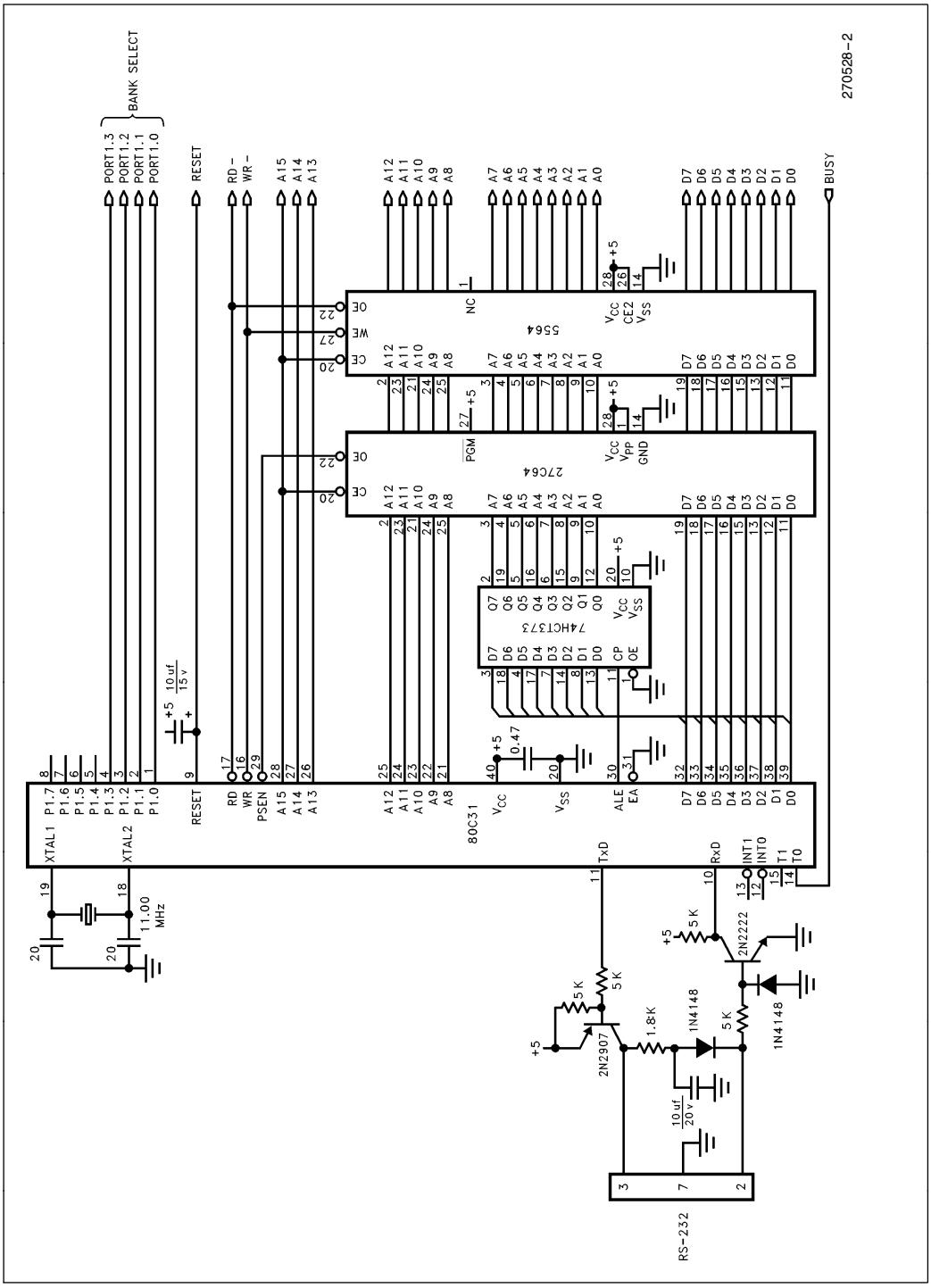
270528-2
BANK SELECT
PORT1.3
PORT1.2
PORT1.1
PORT1.0
RESET
RD –
WR –
A15
A14
A13
BUSY
5564
27C64
74HCT373
80C31
NC
PGM
+5
10 uf
15 v
0.47
11.00
MHz
5 K
1.8 K
2N2907
2N2222
1N4148
10 uf
20 v
RS-232
XTAL1
XTAL2
RESET
RD
WR
PSEN
ALE
EA
TxD
RxD
INT1
INT0
T1
T0

Figure 2

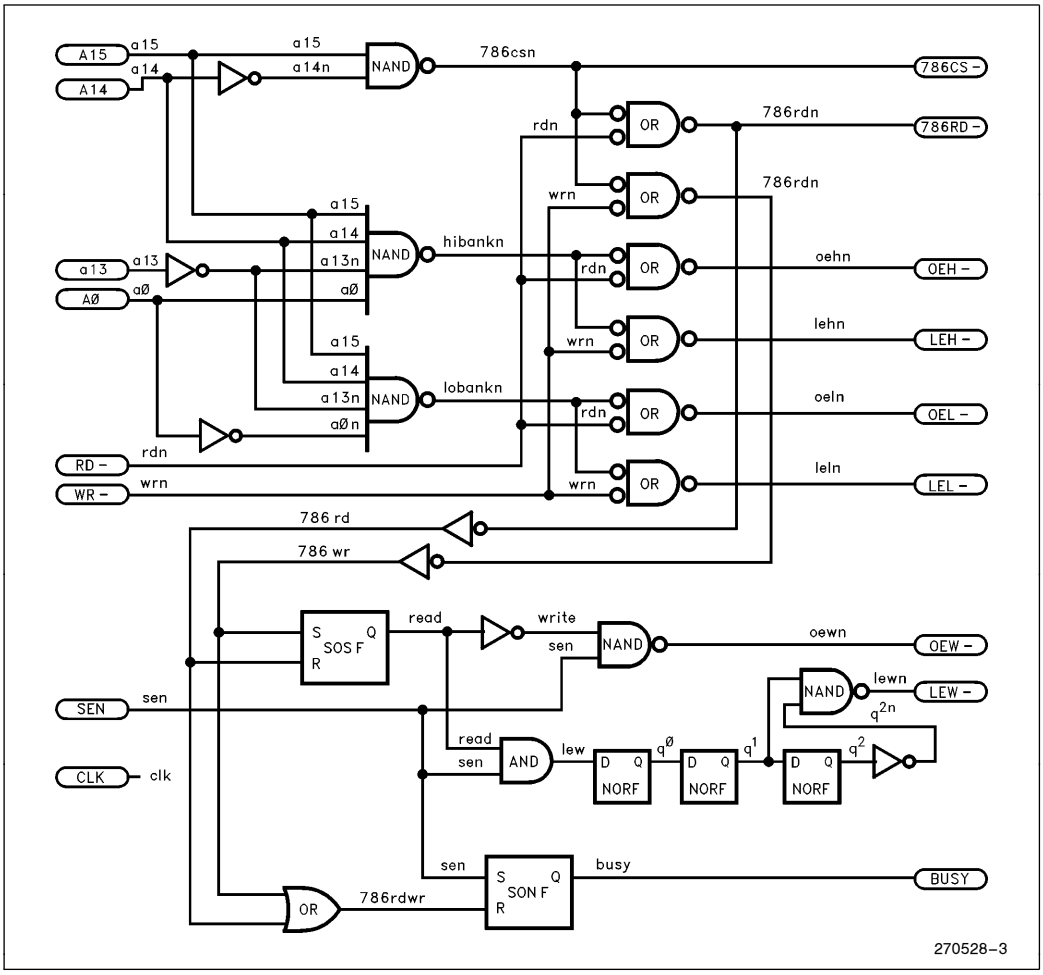

Figure 3. 8051/82786 Control EPLD (5C060-55) Equivalent Circuit

```
INTEL
August 11, 1987
1-003
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5C060
8051/82786 Control Logic for 8051 Demo Board
786 I/O      8000H-807FH
786  Memory    A000H-BFFFH
Registers    C000H,C001H
OPTIONS: TURBO=ON
PART: 5C060
INPUTS: A15@23,A14@14,A13@11,A0@2,RD/@10,WR/@9,SEN@8,CKK
OUTPUTS: 786CS/@15,786RD/16,0EH/@17,LEH/@18,0EL/@19,LEL/@20,
LEW/@21,0EW/@22,READ@4,BUSY@3
NETWORK:
a15 = INP (A15)
a14 = INP (A14)
a13 = INP (A13)
a0 = INP (A0)
rdn = INP (RD/)
wrn = INP (WR/)
sen = INP (SEN)
clk = INP (CLK)
a14n = NOT (a14)
a13n = NOT (a13)
a0n = NOT (a0)
786csn = NAND (a15,a14n)
786CS/ = CONF (786csn,VCC)
786rdn = OR (786csn,rdn)
786RD/ = CONF (786rdn,VCC)
hibankn = NAND (a15,a14,a13n,a0)
lobankn = NAND (a15,a14,a13n,a0n)
oehn = OR (hibankn,rdn)
0EH/ = CONF (oehn,VCC)
lehn = OR (hibankn,wrn)
LEH/ = CONF (lehn,VCC)
oeln = OR (lobankn,rdn)
0EL/ = CONF (oeln,VCC)
leln = OR (lobankn,wrn)
LEL/ = CONF (leln,VCC)
oewn = NAND (sen,write)
0EW/ = CONF (oewn,VCC)
lew = AND (sen,read)
q0 = NORF (lew,clk,GND,GND)
q1 = NORF (q0,clk,GND,GND)
q2 = NORF (q1,clk,GND,GND)
q2n = NOT (q2)
lewn = NAND (q1,q2n)
LEW/ = CONF (lewn,VCC)
786wr = NOR (786csn,wrn)
786rd = NOT (786rdn)
READ,read = SOSF (786rd,clk,786wr,GND,GND,VCC)
write = NOT (read)
786rdwr = OR (786rd,786wr)
BUSY = SONF (786rdwr,clk,sen,GND,GND,VCC)
END$
```

Figure 4.