



8XC251Sx (8XC251SA, SB, SP, SQ) SPECIFICATION UPDATE

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The 8XC251Sx may contain design defects or errors known as errata. Characterized errata that may cause the 8XC251Sx's behavior to deviate from published specifications are documented in this specification update.



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The 8XC251 may contain design defects or errors known as errata. Current characterized errata are available on request.

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REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
08/07/96	002	Added specification clarification, TRHDZ1 timing.
09/18/96	003	Modified the workaround for specification clarification number 001.

PREFACE

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
<i>8XC251SB Embedded Microcontroller User's Manual</i>	272617-001
<i>8XC251SA, 8XC251SB, 8XC251SP, 8XC251SQ Embedded Microcontroller User's Manual</i>	272795-001
<i>Introducing the MCS[®] 251 Microcontroller - the 8XC251SB</i>	272670-001
<i>Maximizing Performance Using the MCS[®] 251 Microcontroller — Programming the 8XC251SB</i>	272671-001
<i>Migrating from the MCS[®] 51 Microcontroller to the MCS 251 Microcontroller (8XC251SB) — Software and Hardware Considerations</i>	272672-001
<i>8XC251SA/SB/SP/SQ High Performance CHMOS Microcontroller datasheet</i>	272783-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to 8XC251 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)

or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page): Page location of item in this document.

Status

Doc: Document change or update will be implemented.

Fix: This erratum is intended to be fixed in a future step of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Eval: Plans to fix this erratum are under evaluation.

Row

|

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A	B	C			
9600001	X			7	Fixed	Negative Flag
9600002	X			7	Fixed	Wsb - Wait States for Memory Region 01
9600003	X			8	Fixed	EJMP at Upper Boundary of any 64K-Byte Region of Memory
9600004	X			9	Fixed	Short Jumps from Memory Region FF: to FE:
9600005	X	X		10	Fix	Interrupt when CPU is Executing User Code not in FF:Region
9600006		X		11	Fix	Carry Flag
9600007	X	X		12	Fix	Watchdog Timer in the Idle Mode
9600008		X		12	Fix	Data Memory Across 256Byte boundary Region with INC DRK, #Short

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	A	B	C			
			X	13	Doc	TRDHZ1 Timing.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision . of this specification update.

IDENTIFICATION INFORMATION

Markings

B-step devices are identified by the marking, Intel (R) (C) '94 '95 B.

C-step devices are identified by the marking Intel (R) (C) '94 '95 C.



ERRATA

9600001. Negative Flag

PROBLEM: The Negative (N) Flag of PSW1 should be set or cleared corresponding to bit 15 of the result. Instead, it corresponds to bit 7 of the result.

IMPLICATION: The affected instructions are listed below:

- a) SRL WRj
- b) SRA WRj
- c) SLL WRj
- d) INC WRj, #short
- e) DEC WRj, #short

WORKAROUND: There are two ways to work around this erratum:

a) Follow the affected instructions listed above with an operation that will rectify the Negative (N) flag correctly. For example:

```
SRL WRj
ANL WRj, #0FFFFH
```

```
SLL Wrj
ANL WRj, WRj
```

b) Check bit 15 of the result vs. relying on the N flag for sign.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All the 8xC251SB devices on A-1 stepping are affected.

9600002. WSB - WAIT STATES For MEMORY REGION 01

PROBLEM: The WSb bit of configuration byte CONFIG1 is intended to configure 0 or 1 wait states for all MOVX (including MOVX @DPTR and MOVX @Ri) instructions for the region 01:0000H-01:FFFFH. However, in 8XC251SB A-1 stepping devices, the MOVX @Ri uses WSa of the configuration byte CONFIG0 instead of WSb.

IMPLICATION: The error affects the generating wait state by using WSb bit of configuration byte CONFIG0 during MOVX instruction at region 01:0000H to 01:FFFFH.

WORKAROUND: There are two ways to work around this erratum:



a) Configure both W_{Sa} and W_{Sb} bits with the same wait state if both MOVX @DPTR and MOVX @Ri instructions are used and require the same wait state.

b) If it is required that W_{Sb} be configured different from W_{Sa}, then limit usage of the MOVX instruction to the MOVX @DPTR format rather than the MOVX @Ri format.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All the 8xC251SB devices on A-1 stepping are affected.

9600003. EJMP At UPPER BOUNDARY Of ANY 64K-BYTE REGION Of MEMORY

PROBLEM: The EJMP instruction is intended for extended jumps from one 64K-byte region of memory to another 64K-byte region of memory. However, when EJMP occurs at the upper boundary of any 64K-byte region of memory, the Program Counter (PC) will land in the wrong 64K-byte region of memory.

Example:

The code: "FEFFFD 8A00XXXX EJMP #00XXXXH"

should branch to address 00XXXXh, but it branches to address region 01XXXXh instead. The operation of this instruction is shown below:

(PC)	<---- (PC) + 2	PC = FEFFFFh
(PC.23:16)	<---- (Addr.23:16)	PC = 00FFFFh
(PC)	<---- (PC) + 2	PC = 010001h*
(PC.15:0)	<---- (Addr.15:0)	PC = 01XXXXh

* Note: Overflow occurs when incrementing the PC for the lower two bytes of destination address. The overflow has incremented the PC.23:16 and caused a deviation from wazzu the destination Addr.23:16.

Instructions affected : EJMP

IMPLICATION: The erratum affects the function of EJMP instruction at the upper boundary region.

WORKAROUND: Avoid this instruction being used at the upper boundary of any 64K-byte memory region.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All the 8xC251SB devices on A-1 stepping are affected.

9600004. SHORT JUMPS FROM MEMORY REGION FF: To FE:

WAZZU PROBLEM: The short jump instruction is intended for a +127 or -128 byte jump relative to the current instruction. However, a short jump from the address in the lower boundary of region FF: will not branch to the address in upper boundary of region FE: even though the destination address is within this -128 byte range. Instead of landing at address in region FE:, it will remain at address in region FF:.

Example:

```
The code with "FEFFF0      ORG FEFFF0h
                FFFFF0 00  REL_ADR: NOP
                FF0002      ORG FF0002h
                FF0002 80EC  SJMP REL_ADR"
```

should branch to address FEFFF0h, but it branches to address FFFFF0h in the same region FF: instead.

IMPLICATION: Instructions affected : SJMP, CJNE, DJNZ, JB, JBC, JC, JE, JG, JLE, JNB, JNC, JNE, JNZ, JSG, JSGE, JSL, JSLE, JZ

Please note that there is no errata for short jumps from upper boundary of region FE: to lower boundary of region FF: ; and no errata for short jumps from upper boundary of region 00: to lower boundary of region 01: and vice-versa.

WORKAROUND: Avoid these instructions being used for a short jump from the lower boundary of region FF: to the upper boundary of region FE:

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All the 8xC251SB devices on A-1 stepping are affected.

960005. Interrupt When CPU Is Executing User Code Not In FF: Region

PROBLEM: For 8XC251SB, the Reset Vector and Interrupt Vectors are defined at the FF: region. If there is an interrupt occurs, the CPU is not able to jump to the Interrupt Vector when the CPU is executing the user code at regions other than FF:.

Example:

If the user code size is 128K-Byte, the first 64K-Byte of the user code is located at FF: region and the other 64K-Byte of the user code is located at FE: region. The Reset Vector and Interrupt Vector for External Interrupt 0 (INT0) are defined at the FF: region as shown below.

```

                                ORG FF:0000h
FF0000 02 0100                LJMP MAIN
                                ORG FF:0003h
FF0003 02 0300                LJMP EXT_INT0
                                ORG FF:0100h
FF0100 12 0200                MAIN: LCALL INITIALIZE_INT0
                                ORG FF:0300h
FF0300 C0D0                   EXT_INT0: PUSH PSW
                                .
                                .
                                RETI

```

When the CPU is executing the user code from the FE: region, if an External Interrupt (INT0) occurs, the CPU is not able to jump to Interrupt Vector (EXT_INT0) as defined at FF: region.

IMPLICATION: This error affects additional interrupt vectors to be initialized at other memory regions.

WORKAROUND: Bit 4 (INTR bit) of Configuration Byte (Config1) must be set to 1. All needed Interrupt Vectors must be defined at other regions (other than FF: region) as well.

For an example, if the user code size is 128K-Byte and the first 64K-Byte of the user code and the Interrupt Vector for External Interrupt 0 is defined at FF: region, that is

```
ORG FF:0003h
```

LJMP EXT_INT0

then there are two possible ways of locating the other 64K-Byte of user code and the workaround:

1) If the other 64K-Byte of user code is located at FE: region, the following instructions must be added to the user code at FE: region,

```
ORG FE:0003h
EJMP EXT_INT0
```

2) if the other 64K-Byte of user code is located at 00: region, the following instructions must be added to the user code at 00: region.

```
ORG 00:0003h
EJMP EXT_INT0
```

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All the 8xC251SB A-1 and 8XC251SA/SB/SP/SQ B-1 stepping devices are affected.

9600006. Carry Flag

PROBLEM: The Carry (CY) Flag of PSW and PSW1 should be set or cleared corresponding to the last bit (bit 7) shifted out from a 8-bit Register after completion of the SLL instruction.

After execution of this instruction, the Carry (CY) Flag is not set or cleared corresponding to the last bit (bit 7) shifted out from a 8-bit Register.

IMPLICATION: The only affected instruction is listed below:

```
SLL Rm
```

WORKAROUND: Avoid this instruction.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s)..

AFFECTED PRODUCTS: All the 8xC251SA/SB/SP/SQ devices on B-1 stepping are affected.

9600007. Watchdog Timer In The Idle Mode

PROBLEM: During the hardware or software WatchDog Timer operation in the Idle Mode, it should RESET the controller and wake up from the Idle Mode after the counter overflow. The controller fails to perform this operation.

IMPLICATION: This error affects the usage of hardware and software watchdog timer during the idle mode.

WORKAROUND: There is no work around for this erratum. This erratum is fixed in the 8XC251SA/SB/SP/SQ next stepping (C stepping).

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All the 8xC251SB devices on A-1 stepping and 8XC251SA/SB/SP/SQ B-1 stepping are affected.

9600008. Data Memory Across 256byte Boundary Region With Inc Drk, #Short

PROBLEM: If the DRk registers contains the address for data memory, the INC DRk, #short instruction where short is either 1, 2 or 4 is not working across the 256Bytes (FFH) boundary region.

Example: If the content of DR4 register is 0000 00FEH, which is the address for data memory, the following instructions i.e.

```
INC    DR4, #2H
```

should increase the content of DR4 register i.e., data memory address to 0000 0100H. But the DR4 register does not contain 0000 0100H.

Instructions affected : INC DRk, #short

IMPLICATION: This error affects the instruction INC DRk, #short.

WORKAROUND: Replace INC DRk, #short with ADD DRk, #short.

Example:

By using the same example shown above, the work around should be

```
ADD    DR4, #2H
```

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All 8xC251SA/SB/SP/SQ devices on B-1 stepping.

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. TRHDZ1 Timing

PROBLEM: The TRHDZ1 (Instruction Float After RD#/PSEN# High) specification on the 8XC251Sx when operating at 12 MHz is 10 ns. However, a slow memory device such as an EPROM typically takes approximately 30 – 90 ns to float its output. (This specification generically called TPHZ, may vary from one manufacturer to another.) Figure 1 and Figure 2 illustrate the TRHDZ1 timing.

The difference between the TRHDZ1 and TPHZ specifications causes contention on the data bus (P0 in nonpage page, P2 in page mode). The 8XC251Sx begins to drive the address for the next bus cycle while the memory device is still driving data from the previous bus cycle.

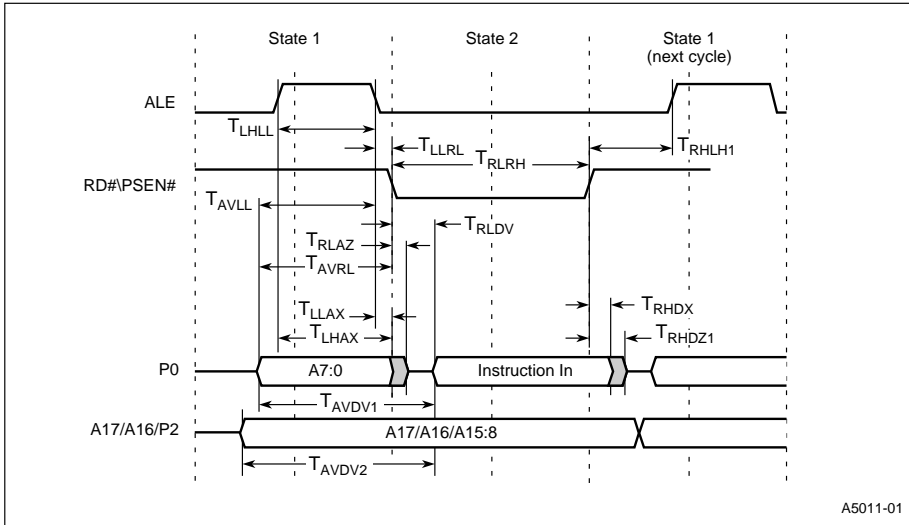


Figure 1. External Code Fetch, Nonpage Mode

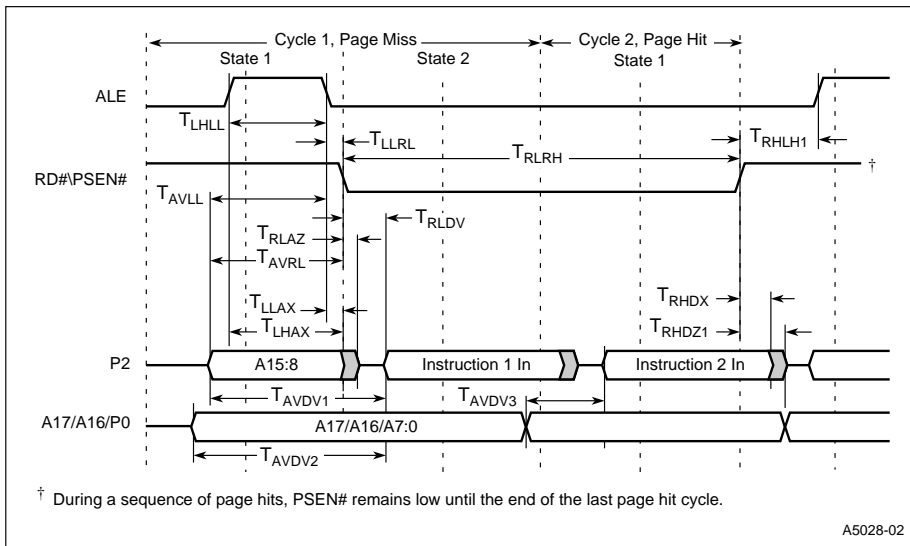


Figure 2. External Code Fetch, Page Mode

To prevent this contention, designers can use a buffer to isolate the output of the memory device from the data bus (port 0 or port 2) of the 8XC251Sx. This will prevent the slow memory device from driving the data bus during the critical period after T_{RHDZ1} expires. We suggest a buffer such as the 74F541 octal, three-state line driver shown in Figure 3.

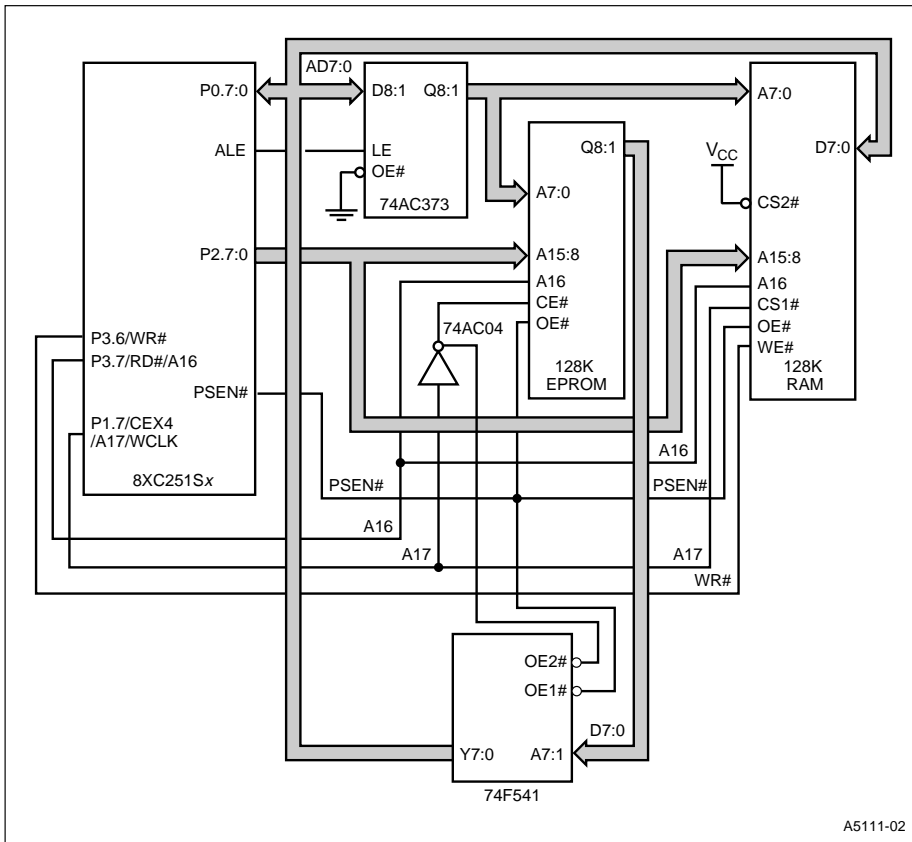


Figure 3. Example Bus Contention Solution for 8XC251Sx

Figure 3 illustrates the connections of an 8XC251Sx configured for nonpage mode with EPROM and RAM in external memory. If your system uses a different configuration, your circuit will be different from the example. The 74F541 is enabled to pass data from the EPROM to the 8XC251Sx (port 0) when OE1# and OE2# are active. Table 1 is a truth table for the 74F541.

Table 1. Truth Table for 74F541

Inputs			Outputs
OE1#	OE2#	A7:1	Y7:1
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

During a read, PSEN# turns the buffer on (OE1# and OE2# are active), connecting the EPROM's output to the 8XC251Sx's port 0.

When PSEN# goes high after a read, 1G# and 2G# are deasserted and the buffer's output switches to the high-impedance state in approximately 9.5 ns (TPHZ for a typical 74F541; the value may vary from one manufacturer to another). Thus, contention on the data bus is prevented. This or a similar hardware solution is recommended for 8XC251Sx designs in which slower memory devices do not meet the TRHDZ1 timing specification.

DOCUMENTATION CHANGES

None for this revision of this specification update.