80C186XL AND 80C188XL EMBEDDED MICROPROCESSORS

SPECIFICATION UPDATE

Release Date: July, 1996

Order Number 272895-001

The 80C186XL and 80C188XL may contain design defects or errors known as errata. Characterized errata that may cause the 80C186XL and 80C188XL's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 80C186XL and 80C188XL Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
80C186XL/80C188XL Microprocessor User's Manual	272164-003
80C186XL/80C188XL 16-Bit High-Integration Embedded Processors datasheet	272431-003

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80C186XL and 80C188XL product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A	B	C D			
9600001		X		7	Fixed	INTx/INTAx

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
001						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
001	003	15	NoFix	80C186 XL/80C188 XL Microprocessor User's Manual Errata

IDENTIFICATION INFORMATION

Markings

A-step production devices may be identified as follows:

The product is marked with a 9-character alphanumeric Intel FPO number underneath the product code number.

For A-step XL devices, the ninth character is "A".

For B-step XL devices, the ninth character is "B".

For C-step XL devices, the ninth character is "C".

For D-step XL devices, the ninth character is "D".

Regardless of sample or production status, there is a STEPID register which may be examined through software. For A-step XL devices, the register contains a value of 01H. For B-step XL devices, the register contains a value of 02H. For C-step XL devices, the register contains a value of 03H. For D-step XL devices, the register contains a value of 04H.

ERRATA

9600001. INTx/INTAx

PROBLEM: An internal problem with the Interrupt Control Unit is cascade mode can cause no acknowledge cycle on the INTA1# line after an interrupt on INT1 or on INTA0# after an interrupt on INT0.

There are two cases. Problem 1: Interrupt 1 is configured in cascaded mode and a higher priority interrupt exists. Problem 2: Interrupt 0 is configured in cascaded mode and interrupt 1 is higher priority.

Problem 1:

An interrupt acknowledge for INT1 is not generated on INTA1#. If two interrupts are in cascade mode, the interrupt acknowledge is generated on INTA0#.

Condition:

Another interrupt of higher priority occurs after the decision is made to service Interrupt 1 but before the expected acknowledge cycle on INTA1#.

Configuration:

1) Master Mode

2) INT 1 is in Cascade mode and enabled

3) An Interrupt of higher priority than INT1 is enabled (DMA, Timers, INT lines, Serial, etc.)

Problem 2:

An interrupt acknowledge for INT0 is not generated on INTA0#. If two interrupts are in cascade mode, the interrupt acknowledge is generated on INTA1#.

Condition:

Interrupt 1, configured as higher priority than interrupt 0, occurs after the decision is made to service Interrupt 0 but before the expected acknowledge cycle on INTA0#.

Configuration:

1) Master Mode

2) INT 0 is in Cascade mode and enabled

3) INT 1 is enabled and higher priority than INT0

Problem 1 Description

Note: In the cases below, the interrupt controller has already decided to service the INT1 interrupt before the higher priority interrupt occurs.

Correct operation of the device acknowledges the interrupt on INTA1# after an interrupt on INT1. Normally, this occurs even if there is a higher priority interrupt after INT1 but before the acknowledge (Figure 1).

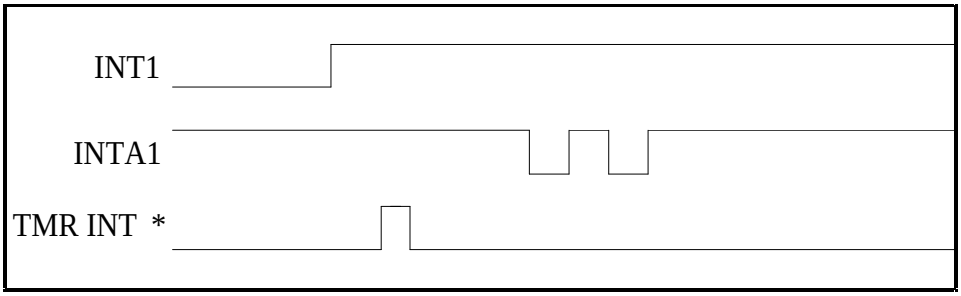

Figure 1. Correct INT 1 Acknowledge Sequence With Higher Priority Timer Interrupt

*Note: This interrupt could be any of the following: DMA, Timers, Serial, INT0, or INT2.

The errata occurs when a higher priority interrupt occurs between INT 1 and its expected acknowledge. The processor completes internal interrupt acknowledge cycles as seen on the status lines but no acknowledge cycle is sent on the INTA1# output (Figure 2).

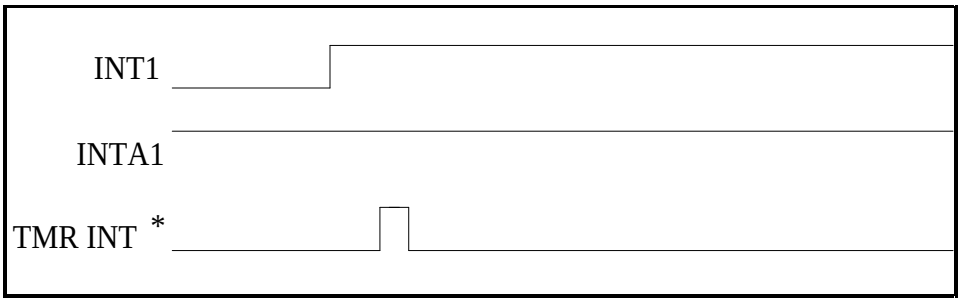

Figure 2. Incorrect INT 1 Acknowledge Sequence With A Higher Priority Timer Interrupt

*Note: This interrupt could be any of the following: DMA, Timers, Serial, INT0, or INT2.

If INT 0 and INT 1 are configured in cascade mode and a higher priority interrupt occurs between INT 1 and its expected acknowledge, then the acknowledge will appear on INTA0# instead (Figure 3).

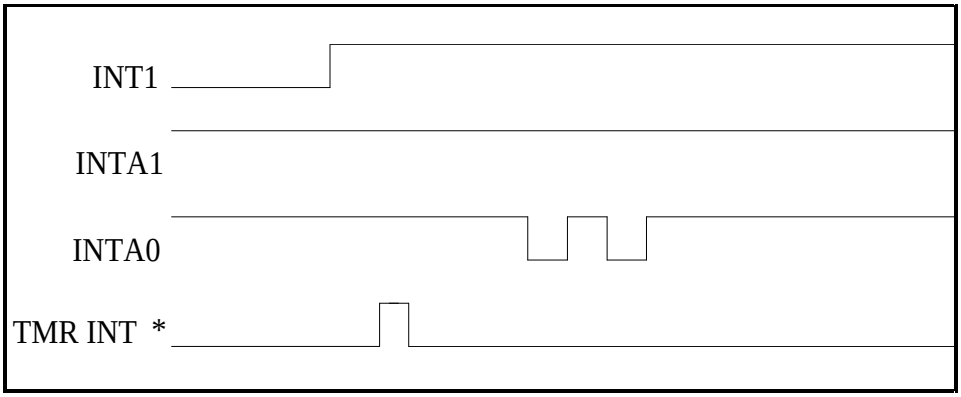

Figure 3. INT 0 And INT 1 Acknowledge Failure Due To Higher Priority Timer Interrupt

*Note: This interrupt could be any of the following: DMA, Timers, Serial, or INT 0.

Problem 2 Description

Note: In the cases below, the interrupt controller has already decided to service the INT 0 interrupt before the higher priority INT 1 occurs.

Correct operation acknowledges INT 0 on INTA0#. Normally, this occurs even if there is a higher priority INT 1 after INT 0 but before the acknowledge (Figure 4).

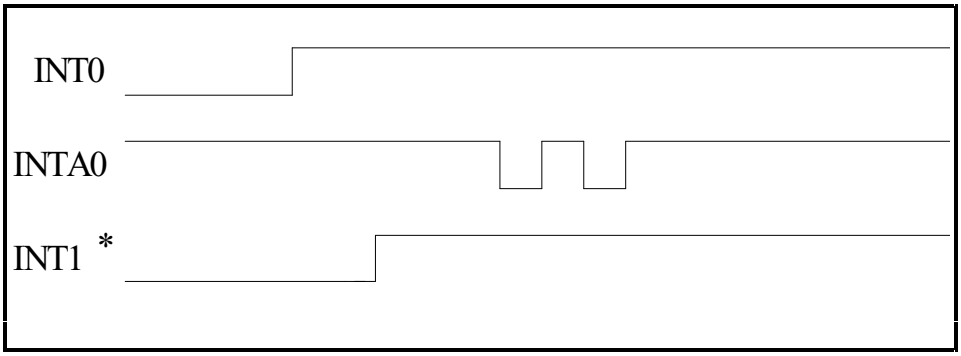

Figure 4. Correct INT 0 Acknowledge operation with a simultaneous INT 1

*Note: INT 1 is the only interrupt that causes the errata to occur.

The errata occurs when INT 1, which is higher priority than INT 0, occurs between INT 0 and its expected acknowledge. The processor completes internal interrupt acknowledge cycles as seen on the status lines but no acknowledge cycle is sent on the INTA0# output (Figure 5).

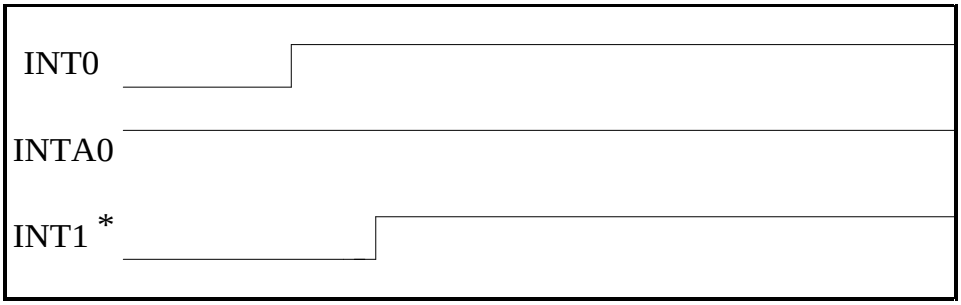

Figure 5. Incorrect INT 0 Acknowledge operation with a simultaneous INT 1

*Note: This problem occurs only if INT 1 is higher priority than INT 0.

If INT 0 and INT 1 are configured in cascade mode and the higher priority INT 1 occurs between INT 0 and its expected acknowledge, then the acknowledge will appear on INTA1# instead of INTA0# (Figure 6).

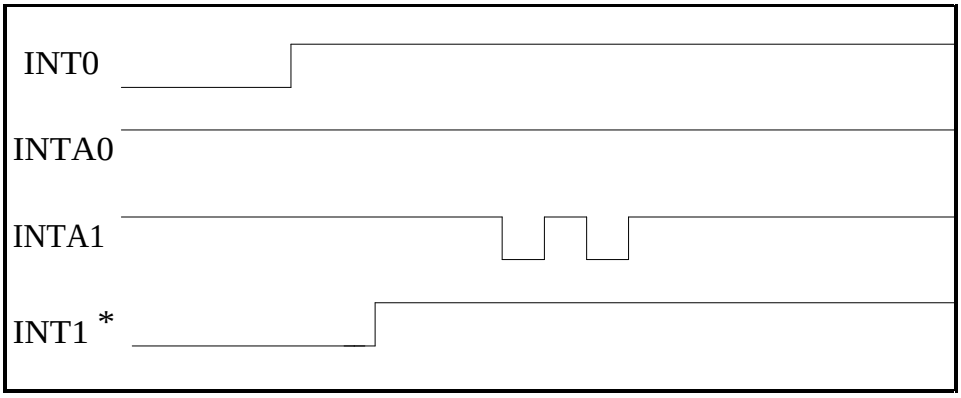

Figure 6. INT 0 and INT 1 Acknowledge Failure due to the higher priority INT 1.

*Note: This problem occurs only if INT 1 is higher priority than INT 0.

IMPLICATION: If two cascaded interrupt controllers are used, the interrupt acknowledge can be sent to the wrong controller. This can cause no acknowledge cycle on the INTA1# line after an interrupt on INT1 or on INTA0# after an interrupt on INT0.

In a system with a single external interrupt controller, the errata will cause no acknowledge to be sent on the INTA# output. Internally, the device still functions normally, only the state of the output pin is incorrect. The Interrupt Request Register and Interrupt Service Register will operate normally.

The 186 will still run two back-to back interrupt acknowledge cycles. If the external interrupt controller does not receive the two interrupt acknowledge pulses, it will never drive the interrupt type onto the data bus. Therefore, the 186 will read an invalid interrupt type.

Software workaround:

	CONDITION	WORKAROUND
1)	Only INT 1 is configured in cascade mode and is lower priority than at least one other interrupt.	Use only INT 0 in cascade mode instead, or make INT 1 the highest priority interrupt, or implement hardware workaround.
2)	INT 1 and INT 0 are both in cascade mode.	Use only one interrupt in cascade mode, or implement hardware workaround.
3)	Only INT 0 is configured in cascade mode and is lower priority than INT 1.	Make INT 0 higher priority than INT 1, or implement hardware workaround.

Master Mode	Cascade Mode	INT 1 Priority vs any other interrupt	INTA1 Problem	INTA0 Problem	Workaround
Yes	INT0 and INT1	N/A	Yes	Yes	Use only one interrupt line in cascade mode or H/W workaround
Yes	INT1 only	Lower	Yes	No	Change to INT0 or make INT1 highest priority
Yes	INT1 only	Higher	No	No	N/A
Yes	INT0 only	N/A	No	Yes	See Table 2
No	N/A	N/A	No	No	N/A

Table 1. Software workarounds for problem 1

Master Mode	Cascade Mode	INT 0 Priority vs any INT 1	INTA0 Problem	INTA1 Problem	Work around
Yes	INT0 and INT1	N/A	Yes	Yes	Use only one interrupt line in cascade mode or H/W workaround
Yes	INT0 only	Lower	Yes	No	Make INT0 highest priority
Yes	INT0 only	Higher	No	No	N/A
Yes	INT1 only	N/A	No	Yes	See Table 1
No	N/A	N/A	No	No	N/A

Table 2. Software workarounds for problem 2

Hardware Workaround:

1) Pull data bus lines 0 to 7 to a known value (using pull-up resistors) to force a defined value on the bus when the errata occurs.

   These resistors will pull the floated bus to 0FFH during the 186 interrupt acknowledge cycle. A type 255 interrupt will be read from the bus and executed. An interrupt service routine for a type 255 interrupt should be included in the software. This solution allows a graceful recovery from the errata condition. If the current design uses interrupt type 255, the resistors can be selectively connected to Vcc or Ground to define an unused interrupt type.

2) Program cascaded interrupt inputs on the 186 to be level sensitive; otherwise, the 186 does not recognize that the interrupt is still active.

3) Write a simple service routine for the interrupt type defined in step 1.

   Now that the system has recovered from the errata, the original interrupts must be serviced. The higher priority interrupt will execute next. Finally the interrupt request from the external interrupt controller must be serviced.

4) Write a simple service routine for an 8259 interrupt 7 (only for cases with two external interrupt controllers).

   In systems with two external interrupt controllers. When the errata occurs because of a higher priority internal interrupt, the wrong INTA# signal will become active. If an 8259 receives an acknowledge and no interrupt is present, it assumes a spurious interrupt occurred and issues an interrupt 7. The service routine for this interrupt must be included in the software.

5) Issue non-specific End of Interrupt commands in INT 0 and INT 1 service routines (only for cases with two external interrupt controllers).

   The situation where the interaction between INT 0 and INT 1 causes the errata is a special case. This situation will occur as just described, the INTA# pulse will be issued to the wrong 8259. In this situation, the interrupt input to the wrong 8259 is active when the acknowledge occurs. The acknowledged 8259 will drive its interrupt type onto the bus, and the CPU will service that interrupt. The only difficulty is what happens internally to the 186. The incorrect Interrupt Request and Service Bits have been set. To recover from this, the interrupt service routine must issue a non-specific End of Interrupt command. At this point, the wrong interrupt has been serviced correctly and because the interrupt inputs are configured to be level sensitive, the initial interrupt is now serviced.

STATUS: Fixed on C-Stepping. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS:

80C186 XL/80C188 XL
80C186 EA/80C188 EA
80C186 EB/80C188 EB
80L186 EA/80L188 EA
80L186 EB/89L188 EB

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

001. 80C186 XL/80C188 XL Microprocessor User's Manual Errata

ISSUE: Please make the following corrections to the *80C186XL/80C188XL Microprocessor User's Manual* and keep this errata sheet with your manual for future reference. These changes will be included in a future revision of this manual.

Page	Change
6-10, Figure 6-8. PACS Register Definition	The register diagram should go from U19 through U10, not U19 through U13. In the Bit Mnemonic column, "U19:13" should be changed to "U19:U10." In the Function column, "U19:13 are compared with A19:13" should be changed to "U19:10 are compared with A19:10." Also note that the first active 1k byte boundary of the PCS chip select starts at the first 1k boundary; ***not*** at 0H.
8-17, Figure 8-8. Interrupt Mask Register	The reset state for INT3:0 should be Fh, DMA1:0 should be 3h, TMR should be 1h
9-5, Figure 9-3.	The stem below Conditional statement "Counter = Compare 'A' ?" should be a "YES" and the stem to the right should be a "NO."