186 FAMILY EVAL BOARD SPECIFICATION UPDATE

Release Date: July, 1996

Order Number 272893-001

The 186 Family Eval Board may contain design defects or errors known as errata. Characterized errata that may cause the 186 Family Eval Board's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

his document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 186 Family Eval Board Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
EV80C186EA/XL Evaluation Board User's Manual	272124-001
EV80C186EB Evaluation Board User's Manual	272068-002
EV80C186EC Evaluation Board User's Manual	272125-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, and documentation changes which apply to the 186 Family Evaluation board product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	EA/XL	EB	EC			
9600001			X	7	NoFix	System Expansion Considerations
9600002			X	7	NoFix	Flash Vpp Switch

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	EA/XL	EB	EC			
001		X		8	NoFix	Serial Connector (P2)
002		X		8	NoFix	Expansion Buffer Control (U25 And U27)

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
001	001	9	NoFix	EA_EXP PLD (U26)
002	001	10	NoFix	Refresh Problem
003	001	10	NoFix	Unconnected Header Pins

IDENTIFICATION INFORMATION

Markings

Product # EV80C186EA/XL

EV80C186EB

EV80C186EC

ERRATA

9600001. System Expansion Considerations

PROBLEM: The present configuration assumes GCS1# is used for all Expansion Bus accesses.

IMPLICATION: If you plan to use the GCS2# through GCS7# (chip-select function) for system expansion, this is not possible in the present system configuration. These pins can be used as port pins.

WORKAROUND: However, by modifying the EC_PLD2 equations, the other General Chip Select lines could be used to access expansion memory. The equations controlling the expansion bus buffers would have to be modified to allow reading and writing of data. Specifically, the “NUMERICS” reference should be removed from the nHI_XCR_EN, nX_XC_EN and the nLO_XCR_EN signal equations.

Note: The revised JEDEC file for EC_PLD2 can be found on the Applications BBS under filename EVEC_FIX.ZIP.

STATUS: There are no plans to correct this behavior. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: EV80C186EC Evaluation Board

9600002. Flash Vpp Switch

PROBLEM: Page 1-12 of the *EV80C186EC Evaluation Board User’s Manual* (Order Number 272125-001) makes a reference to FLASH Vpp Switch. This operation is not functional.

Page F-4 of the User’s Manual, the circuit schematics show the presence of an inverter IC, U7. This IC does not exist on the board (which makes the FLASH Vpp Switch operation invalid).

Do Not switch the E1 jumper to position BC while the EPROMs are on the board. This will damage the EPROMs.

IMPLICATION: FLASH Vpp Switch is not functional.

WORKAROUND: N/A

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: EV80C186EC Evaluation Board

SPECIFICATION CHANGES

001. Serial Connector (P2)

PROBLEM: The evaluation board schematics on page A-7 of the *EV80C186EB Evaluation Board User's Manual* (Order Number 272068-002) is incorrect. Connector P2 is labeled as a DB9 Female connector. On the actual board, this connector is a DB9 Male.

IMPLICATION: As a result, all signals are reversed. TXD0 (P2-3) is unaffected (it is centered on the connector).

WORKAROUND: RXD0 needs to be connected to P2-4 and CTS0 needs to be connected to P2-7. Also, ground must be connected to pin P2-1. A simple way to fix this problem is to flip-over the ribbon cable attached to the female part of the connector.

AFFECTED PRODUCTS: *EV80C186EB Evaluation Board User's Manual*

002. Expansion Buffer Control (U25 And U27)

PROBLEM: This problem initiates in the PLD at U16. U16-16 is not the PASSIVE output connected to the LED array. U16-16 is an output, an inverted DT/R signal. U16-13 is not grounded, it is connected to the 80C18xEB DT/R output (U8-16).

On the schematics, the DIR pins of the 74AC245 buffers are connected to the DT/R output of the processor. This is not the case. U25-1 and U27-1 (DIR) pins are connected to U16-16, the inverted DT/R signal.

IMPLICATION: This configuration will not work (buffers will drive data in the wrong direction).

WORKAROUND: To correct the problem, cut the trace from U16-16 to U25-1 and U27-1. Connect a wire from U16-13 to U25-1 and U27-1. This connects the processor DT/R signal to the buffer direction control.

AFFECTED PRODUCTS: EV80C186EC Evaluation Board

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update

DOCUMENTATION CHANGES

001. EA_EXP PLD (U26)

ISSUE:

1.) PLD Equation prohibits reads from the Expansion Bus in the EV80C186EA/XL Evaluation Board. The existing equation:

DRT = !DTR # DTR & EXPDEN

always evaluates to 1 when EXPDEN = 1 (Expansion bus cycle in progress). This causes the output of the PLD to go low. The 74AC245 buffers will always write data to the expansion bus but not read data from the expansion bus. To function correctly, the equation needs to be changed to:

DRT = !DTR & EXPDEN

2.) An incorrect PLD equation, in appendix D of the *EV80C186EC Evaluation Board User's Manual*, causes only certain blocks of memory space in DRAM to be refreshed in addition to mirroring for certain segments. The bug is in the following PLD equation (EC_PLD1):

old equation: M8 = (!nMUX&LA9)#(nMUX&LA18);

M8.OE = 'B' 1; /** TURN ON THE OUTPUT **/

It should be revised as the following:

new equation: M8 = (nMUX&LA9)#(!nMUX&LA18);

M8.OE = 'B' 1; /** TURN ON THE OUTPUT **/

Note: The JEDEC file for EC_PLD1 can be found on the applications BBS under filename EVEC_FIX.ZIP.

AFFECTED PRODUCTS :

1.) EV80C186EA/XL Evaluation Board

2.) EV80C186EC Evaluation Board

002. Refresh Problem

ISSUE: This does not affect boards using the Paradigm Software. In the RISM monitor, the DRAM Refresh Base Address register is programmed incorrectly. The DRAM Base address is set to 0000H, and the DRAM chip select is never activated, so the DRAM is never refreshed. This is not a problem if user code is loaded into SRAM and does not use DRAM. There are two possible fixes:

1) Revise the RISM source code and burn two new EPROMs. Make sure the EPROMs are burned so they will work with the processor type being used (186 or 188). All bytes need to be programmed in the low-byte and every other odd byte must be burned into the high-byte. It may help to view to current EPROM contents on the programmer to understand how the data is stored.

2) The RFBASE register can be reprogrammed in the user's code to refresh the correct memory range. The following code sequence will do this:

```
MOV    DX, 0FF80H    ;GCS0ST REGISTER (DRAM Chip Select)
IN     AX, DX ; READ GCS0ST CONTENTS
AND    AX, 0FFF0H    ; MASK WAIT-STATE BITS
SAR    AX, 9         ; SHIFT AX RIGHT 9 BITS
MOV    DX, 0FFB0H    ; RFBASE REGISTER
OUT    DX, AL ; REPROGRAM REFRESH BASE ADDRESS
```

The user can optionally disable DRAM refresh before executing this code, but it should make no difference if the refresh counter is set to zero when the base address is programmed.

Note: The revised HEX file for RISM code can be found on the Applications BBS under filename EVEC_FIX.ZIP.

AFFECTED PRODUCTS: EV80C186EC Evaluation Board

003. Unconnected Header Pins

ISSUE: Page 1-13 of the User’s Manual (272125-001) makes a reference to an errata on the boards marked with revision number 2.0. This errata is found on boards marked with the Rev. 1.1 label. Rev. 1.1 is the latest revision of this evaluation board, there is no Rev. 2.0 board. In addition to this errata, there are several other unconnected header pins. The following table gives a listing of the unconnected pins and their intended routes.

Header/Jumper Name	Header Pin Number/Jumper Post	Processor Pin Name	Processor Pin Number
E2 Jumper	B Post	P2.4/RXD1	20
E3 Jumper	B Post	P2.7/CTS1#	23
JP4	43	S2	80
JP5	7	P3.2/DMAI0	26
JP5	3	P3.0/RXI1	24

AFFECTED PRODUCTS: EV80C186EC Evaluation Board