



AP-735

**APPLICATION
NOTE**

**Building a PC-Compatible
Embedded System Using the
Intel386™ EX Processor
and the RadiSys® R380EX™
Embedded System Controller**

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1.0 Introduction	1
1.1 Why PC-Compatibility is attractive for embedded designs	1
2.0 System Overview	1
3.0 The System Core	1
4.0 Embedded PC Reference Design Description	1
4.1 Embedded PC Reference Design Block Diagram	2
5.0 RadiSys R380EX Embedded System Controller Overview	4
5.1 Intel386 EX Processor Support	4
5.2 ROM/Flash ROM Interface	4
5.3 DRAM/Flash Memory Controller	4
5.4 Keyboard/Mouse Controller	5
5.5 Real Time Clock	5
5.6 Enhanced IDE Interface	5
5.7 ISA Bus Interface	6
5.8 Intel386 EX Processor Local Bus Interface	6
5.9 LBA Cycles	6
5.10 LDEV Cycles	6
5.11 Power Management	7
5.12 SMI and Clock Switching	7
5.13 Halt or Shutdown	7
5.14 Programmable Chip Selects	8
5.15 16-bit Digital I/O Port	8
5.16 Data Bus Transceiver Control	8
6.0 Functional Description of the Intel386™ EX Processor	9
6.1 Clock Generation and Power Management Unit	10
6.2 Chip Select Unit	10
6.3 Interrupt Control Unit	10
6.4 Timer/Counter Unit	10
6.5 Watchdog Timer Unit	10
6.6 Asynchronous Serial I/O Unit	11
6.7 Synchronous Serial I/O Unit	11
6.8 Parallel I/O Unit	11
6.9 DMA and Bus Arbiter Unit	11
6.10 Refresh Control Unit	12
6.11 JTAG Boundary Scan Unit	12

6.12 Interval Timers	12
6.13 Port 92	12
6.14 Watchdog Timer	12
6.15 SIO 0 & 1	12
7.0 I/O Devices	12
7.1 I/O Map	12
7.1.1 External I/O	13
7.1.2 Keyboard/mouse	13
7.1.3 RTC	13
7.1.4 IDE	14
7.1.5 LCD VGA	14
7.1.6 PCMCIA Controller	14
8.0 Hardware Interrupts	14
9.0 Additional Design Features	15
9.1 Intel Flash with Flash File System	15
9.2 3.3V Operation	15
9.3 POST Code Display and Logic Analyzer Connections	15
9.4 ISA Bus and PC/104 Bus	15
9.5 Ethernet	15
9.6 System BIOS	16
9.7 IC Works W48C54A-59 Frequency Generator	16
10.0 Summary	16
11.0 Highlights of Other System Components	16
11.1 The IC Works W48C54A-59 Frequency Generator	16
11.2 Intel's SmartVoltage Boot Block Flash	17
11.2.1 Product Highlights	17
11.2.2 Product Description	17
11.3 Cirrus Logic CL-GD6245: LCD VGA Controller	18
11.3.1 Product Highlights	18
11.3.2 Product Description	18
11.4 Cirrus Logic CL-PD6710: PC Card Host Adapters	18
11.4.1 Product Highlights	18
11.4.2 Product Description	18
11.5 The SMC91C94 Ethernet Controller	19
11.5.1 Product Highlights	19
11.5.2 Product Description	19
11.6 The SMC FDC37C665GT—Advanced High-Performance Multi-Mode Parallel Port Super I/O Floppy Disk Controller	20
11.6.1 Product Highlights	20

12.0 Contact Information	21
12.1 Intel Corporation	21
12.2 RadiSys Corporation	21
12.3 IC Works	21
12.4 Cirrus Logic	21
12.5 SMC	21

FIGURES

Figure 1.	Block diagram of the Intel EXPLR2 Embedded PC Reference Design	3
Figure 2.	Intel386™ EX Microprocessor Block Diagram	9
Figure 3.	IC Works W48C54A-59 Pinout	17

TABLES

Table 1.	Reference Design I/O Map	13
Table 2.	Interrupt Mapping	15
Table 3.	Output Frequency Selection	16
Table 4.	Related Intel Documents	21

1.0 Introduction

The Intel EXPLR2 Embedded PC Reference Design was developed to enable shorter design cycles by providing a proven design as a starting point. It can be characterized as a PC-like platform, and highlights the features of its embedded component core which is based on the Intel386™ EX processor and the RadiSys® R380EX* Embedded System Controller. The Intel EXPLR2 Embedded PC Reference Design Kit can be used “as is” or as a building block to enhance a specific solution.

The Embedded PC Reference Design incorporates a complete set of PC peripherals, from keyboard controller and real time clock, on through an LCD VGA controller and Ethernet controller. The features of this design were chosen to provide the designer with a very complete set from which to start an embedded computer design. By choosing a subset from this proven design, embedded designers are able to concentrate on creating the specific circuitry unique to their design, rather than “sweating the details” of creating an embedded PC from scratch.

1.1 Why PC-Compatibility is attractive for embedded designs

Designers understand PCs and perceive that they are easier to use than alternatives. The PC has a familiar, well-understood architecture. It is attractive as a building block, which alleviates the need for an embedded systems expert to design the “smarts” for the device you are really trying to build. Because it is “PC-compatible,” a wide range of software and tools are available which would not be true for a “from the ground up, full-custom” design. This can lead to a faster development cycle and a shorter time to market. The monetary and schedule costs of at least the proof of concept hardware and software is lower because of the wide variety and availability of off the shelf hardware and tools.

2.0 System Overview

The Embedded PC Reference Design uses the Intel386 EX processor which has a static Intel386 CX processor core and a host of integrated peripherals, including DMA and interrupt controllers, serial and parallel ports, chip selects, timers/counters, JTAG, and power/system management features. Its 26-bit addressing provides a large 64MB memory address space.

Since the Embedded PC Reference Design utilizes the highly integrated Intel386 EX processor, it does not require

the addition of a standard PC chip set. Instead, it uses the RadiSys R380EX Embedded System Controller which includes a DRAM controller, keyboard/mouse controller, Real Time Clock (RTC), Digital I/O, Enhanced IDE interface, Power Management, SMI support and ISA Bus Interface. The Reference Design also incorporates a number of additional technologies which may be used as building blocks for a myriad of applications.

This design includes the set of features required for most DOS* and Windows* based embedded applications. It is self-contained, and includes an LCD VGA Controller, single slot PCMCIA controller, and expansion capabilities via the ISA Bus and PC/104 connectors. The design includes a Cirrus Logic* GD6245 LCD VGA graphics controller and a Cirrus Logic PD6710 PCMCIA controller on the ISA bus. The R380EX integrates the RTC and the keyboard/mouse controller, as well as provides the IDE disk interface and PC/104 and ISA bus interface.

Even though the implementation is mostly PC-compatible, some software drivers and BIOS customization are required to handle the re-assignment of the DMA channels, interrupts, and other capabilities.

3.0 The System Core

At the core of the EXPLR2 Embedded PC Reference Design are the Intel386 EX processor, the RadiSys R380EX Embedded System Controller, Intel Boot Block Flash memory and a DRAM SIMM. These four items provide a complete minimum PC-compatible core system on which to build. The following sections describe in more detail these and other functional blocks within the system.

4.0 Embedded PC Reference Design Description

The Intel EXPLR2 Embedded PC Reference Design is DOS and Windows compatible, and uses a PC-like BIOS. It features several products and technologies:

- Embedded Intel386 EX Processor
- Intel 4Mb Boot Block Flash Memory
- Intel Flash Memory devices utilized with a Flash File System
- RadiSys R380EX Embedded System Controller with integrated RTC and Keyboard/Mouse controller
- LCD VGA Controller
- PCMCIA Slot

- PC/104 and ISA Bus connectors

The Embedded PC Reference Design functional features include:

- Pipelined, zero wait state, page mode operation
- 512KB to 64 MB using standard FPM or EDO DRAM SIMMs in two x32 SIMM sockets
- LCD VGA Graphics Controller (512KB DRAM frame buffer)
- Support for color and monochrome LCDs
- RTC with Extended Battery Backed RAM (part of R380EX)
- PS/2 Style Keyboard and Mouse Interface (part of R380EX)
- Enhanced IDE Hard Disk Interface (part of R380EX)
- PCMCIA 2.0 (single slot)
- 2 Asynchronous Serial Ports (COM1 and COM2)
- ISA Bus and PC/104 Bus connectors

The features of the Intel386 EX processor are used extensively to minimize the requirement for a chip set and external logic. The interrupt controller, chip select unit, wait state generator, SIOs, and dynamic bus sizing are all used.

NOTE: Although this is a complete functional unit, the design is modular, allowing for addition and modification of features to meet the specific requirements of a target application. While a schematic page has been included in this reference design demonstrating an Ethernet interface, it was not integrated and tested in the original design.

4.1 Embedded PC Reference Design Block Diagram

Figure 1 shows the Embedded PC Reference Design system block diagram.

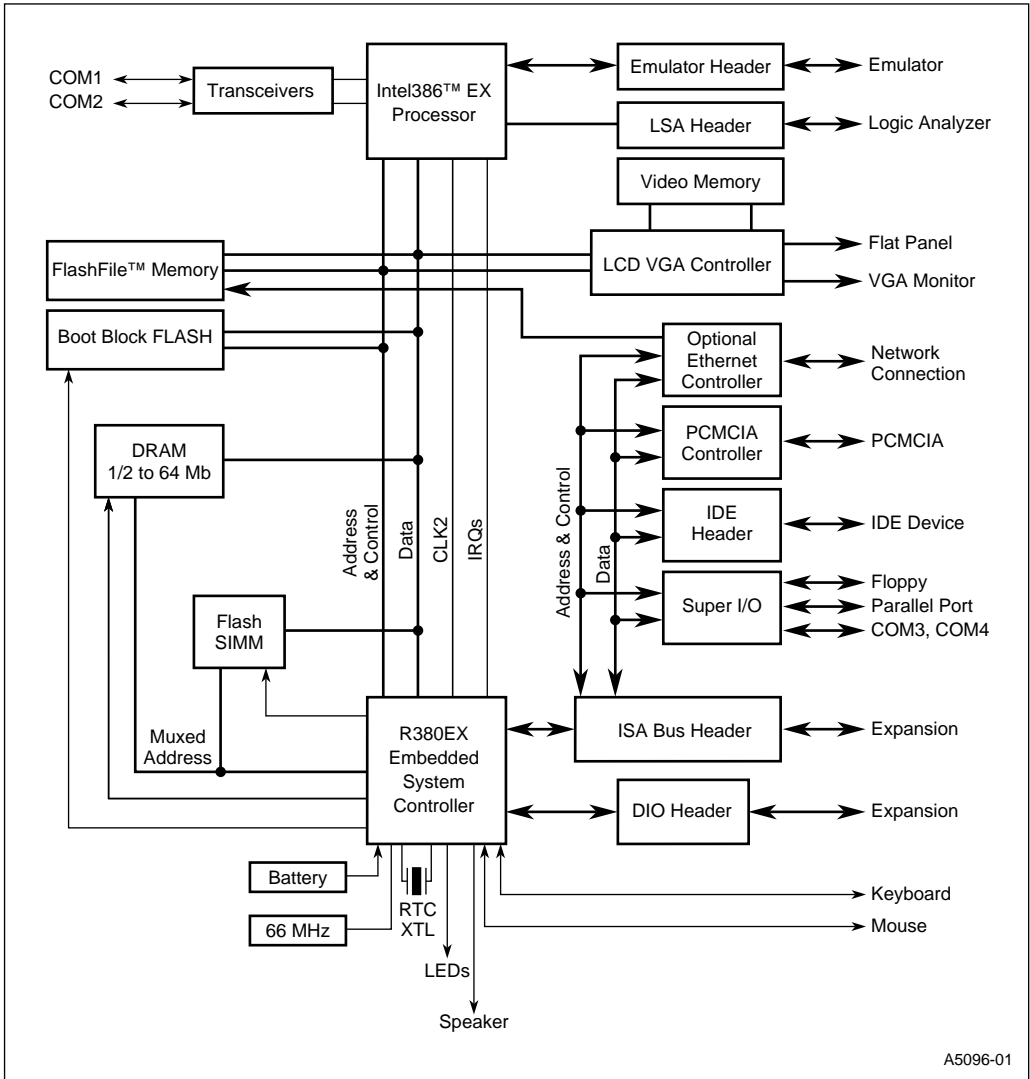


Figure 1. Block diagram of the Intel EXPLR2 Embedded PC Reference Design

5.0 RadiSys R380EX Embedded System Controller Overview

The RadiSys R380EX Embedded System Controller is a member of the RadiSys family of embedded core logic specifically designed to support the Intel386 EX processor. The R380EX directly incorporates features needed for a PC-compatible embedded system design, and provides a simple, low-cost, “glueless” interface to additional chips like a video controller or a PCMCIA controller.

The functional design of the R380EX is directly incorporated from the PC architecture. The R380EX includes a DRAM controller, keyboard/mouse controller, real time clock, enhanced IDE interface, and ISA bus controller. The DRAM controller is compatible with both fast-page-mode (FPM) and extended-data-out (EDO) DRAM. It can be configured to support both DRAM SIMMs and flash SIMMs for greater system flexibility. The keyboard/mouse controller and real time clock are designed to be PC-compatible. The enhanced IDE interface supports a maximum transfer rate of approximately 6MB per second. The ISA bus controller has a separate data bus, and manages the ISA signals to ensure a “quiet” bus for cycles not directed to the ISA address space.

The power management capabilities of the R380EX include clock source switching, halt detection, SMI event generation, and a programmable clock restart delay to ensure clock frequency settling when restarting the oscillator from a powerdown state. The Intel386 EX processor clock source can be switched between the CLK2OSC input divided by 1, 4, or 16, and the 32.768KHz real time clock oscillator, thereby reducing the system power consumption.

The R380EX has four user programmable I/O chip selects in addition to the Intel386 EX processor's chip selects. There are 16 bits of individually programmable digital I/O along with six bits of digital output. Additional functional blocks handle the Intel386 EX processor halt and shutdown cycles, and control the speaker and external LEDs. The main and alternate functions of many of the pins are controlled through internal registers within the R380EX. The R380EX can operate on either 5V or 3.3V.

5.1 Intel386 EX Processor Support

The R380EX connects directly to the Intel386 EX processor local bus and supports 3.3V and 5V Intel386 EX processors. It supports the Intel386 EX processor up through 33 MHz at 5V, and the 3V device up through 25 MHz.

5.2 ROM/Flash ROM Interface

The R380EX ROM/Flash ROM interface supports a variety of x8 and x16 ROM/Flash devices to hold the BIOS. Most PC-compatible implementations use an 8-bit device to hold the BIOS. The BIOS code is usually copied into shadow DRAM as part of the boot process. By using this capability of the R380EX, slow accesses to the Flash/ROM device are replaced by fast access to the shadow DRAM. This also allows “disposable” boot modules to be included in the BIOS without paying a code space penalty after they are executed. The read/write mapping which is part of the process of setting up the BIOS shadowing is controlled through two registers in the R380EX.

The R380EX configuration registers are specifically designed to support the Intel 28F00xBV-T by-8 or similar by-16 flash devices. When using an Intel 28F400BV part for example, the upper 128KB (which includes a 16KB boot block) is normally used for the BIOS. The lower 384KB can contain user code. If user code is not needed, then a smaller device could be used (e.g., 28F001BV-T). The BIOS usually consists of at least a 16KB boot block, and a 112KB System BIOS. Once shadowed, the BIOS running in DRAM can occupy up to 256KB just below 1MB of memory.

The capability for dual mapping of a single BIOS device simplifies system design. This capability enables the ROM to be visible both at the top of the full address space, and at the top of the 1MB address space as required by the processor and DOS. Register bits inside the R380EX are used to select the address location and amount of the BIOS code visible below the 1MB address boundary.

The ROM/Flash ROM interface includes the ability to selectively protect the boot-block portion of the BIOS device during a re-flash operation. Three input pins are used, in addition to software features, to enable writing to the application Flash, and regular, or boot-block portion of the BIOS flash devices. These capabilities enable units to easily have their BIOS or application software upgraded in the field.

5.3 DRAM/Flash Memory Controller

The R380EX's DRAM Controller is designed to work with up to two independent DRAM or flash SIMM modules. The memory controller can be placed into one of two modes enabling a maximum DRAM configuration of either 16MB/module, or 64MB/module. Both modes support one or two modules of DRAM or flash SIMMs. Each module

can support up to a 32 bit wide Fast Page Mode DRAM, Extended Data Out DRAM, or a flash SIMM. Each module can be from 512KB up to 16MB (or 64MB) in size.

The timing parameters for DRAM accesses are configured through the R380EX DRAM control registers.

A second, externally controlled, DRAM port can be implemented with R380EX. The DRAMHOLD# signal is an input to the R380EX that is used to request use of the DRAM interface. An external controller assumes a grant when DRAMHOLD# is asserted and all RAS and CAS lines are unasserted. The external controller is responsible for generating the required timing for the memory that it is accessing. Both the R380EX and the external controller must monitor LOCK# from the Intel386 EX processor and not take the bus from the other device if LOCK was asserted during the previous DRAM cycle.

5.4 Keyboard/Mouse Controller

The R380EX contains a PC/AT compatible keyboard controller with PS/2 compatible mouse controller extensions. The keyboard controller is clocked by BCLK (also referred to as SYSCLK), at the ISA bus system clock frequency. Response to keyboard commands is nearly immediate, usually within one BCLK, due to the fact that the keyboard controller function is internally implemented as a hard-wired state machine.

The R380EX can also be configured to use an external keyboard controller. In this case, the CS_KB# is used as the keyboard controller chip enable and the ISA Bus SA2, IOR# and IOW# signals can be used to communicate with the keyboard controller.

An external keyboard controller might be used when a non-PC-standard keyboard mapping is used, or some other special “keyboard” device is used.

5.5 Real Time Clock

The R380EX contains an integrated real-time clock, which provides the PC function of the date/time clock, alarm, programmable periodic interrupt, 114 bytes of battery backed CMOS RAM, I/O registers 070h and 071h, and the crystal and battery input.

The RTC has isolated power pins for the battery source (RTCVCC and RTCGND), a reset signal for the CMOS RAM (RTCRES#), two crystal pins (X1, and X2) for a 32.768KHz crystal and an interrupt output (RTCIRQ). The

interrupt should be connected to IRQ8 (INT4) on the Intel386 EX processor.

The RTC is integrated into the R380EX because it is part of most PC-compatible embedded designs. However, since some designs may need to use an external RTC, the ability to completely disable the RTC is provided by pulling pin MA1 high through a resistor during power-on reset (when PWRGOOD is deasserted). In this case, the R380EX contains glue logic to generate control signals RTCAS, RTCRD#, and RTCWR# for an external RTC chip. RTCAS is asserted for an I/O write access to address 070h. RTCRD# is asserted for an I/O read access of address 071h. RTCWR# is asserted for an I/O write access to address 071h. RTCRD# has the same timing as IOR#. RTCAS and RTCWR# have the same timing as IOW#.

5.6 Enhanced IDE Interface

The R380EX can support the ATA-2 specified programmed I/O mode 3 and 4 for IDE drives at a maximum transfer rate of approximately 6MB/second. The R380EX powers up with mode 0 timing to support both older IDE drives that are incapable of interfacing at mode 3 and mode 4 speeds, and to support the power-on mode of the newer EIDE drives.

The IDE interface consists of IDEWR#, IDERD#, two buffer enables (IDE_ENHI#, IDE_ENLO#) and the IDED7 pin. The IDEWR# and IDERD# signals connect directly to the IDE connector and allow the R380EX to support the higher transfer rates of Enhanced IDE drives without requiring the ISA bus IOR# and IOW# signals to violate the ISA bus pulse widths. IDE_ENHI# and IDE_ENLO# connect to the enable input of a ‘245-style bi-directional buffer for the 16-bit data path to the IDE connector.

The IDE interface also requires one or two chip selects (HDCS[1:0]#). These can be generated by using one or two of the four R380EX user programmable chip selects (CS_USR[3:0]#). HDCS0# is the primary hard disk chip select and should be programmed for assertion for accesses to I/O addresses 1F0-1F7h. HDCS1# is the secondary hard disk chip select and should be programmed for assertion for accesses to I/O addresses 3F6h and 3F7h.

IDED7 connects to the IDE connector data bit 7 and resolves conflicts with floppy disk interface access to I/O address 3F7h. ISA I/O address 3F7h is shared between an IDE device and a floppy disk controller. The R380EX resolves this conflict for bit D7 by bi-directionally buffering D7 between the SD bus and the IDE interface, except in one

special case. This case is an I/O read from address 3F7h. In this one case the R380EX does not pass IDE data bit 7 to the SD bus, but instead tri-states SD7. This allows a floppy disk controller to drive SD7 as per ISA requirements.

If the IDE interface is enabled, there is no way to disable this rebuffering. Therefore, IDE data bit 7 must always connect through the R380EX, even if the system design is such that all the other IDE data bits are connected directly to the SD bus without an intervening data transceiver.

5.7 ISA Bus Interface

The R380EX ISA bus controller manages a separate set of ISA bus data and control signals. The controller supports 8- and 16-bit transfers, including translation for 16-bit requests from the CPU to 8-bit ISA devices, and 8-bit requests to 16-bit devices. It implements a “quiet ISA bus” feature. When the R380EX sees an access that is not destined for the ISA bus (i.e., a local bus cycle, a non-DMA DRAM cycle, or a cycle internal to the R380EX), it does not drive the ISA bus data or control signals. In addition, ISA bus refresh cycles may be disabled. This reduces overall system power consumption.

The controller also produces the ISA (AT) bus clock (SYSCLK) which can be the 2X CPU clock divided by 4, 6, or 8.

The R380EX does not expand the interrupt or DMA capabilities of the Intel386 EX processor. However, fly-by DMA cycles are supported by the R380EX ISA interface logic. If additional DMA channels are required, an external DMA controller chip could be added.

In order to use the Intel386 EX processor internal DMA channels with external DMA-controlled devices, the R380EX coordinates the state machines for the ISA bus and the DRAM controllers. The R380EX provides the proper control signals for mating the memory access with the ISA I/O access.

The R380EX ISA bus controller does not implement two seldom used aspects of the ISA bus: multiple bus masters and I/O channel check. This will rarely be in issue in an embedded system.

The ISA output signals from the R380EX have 8 mA drive capability which is sufficient for most embedded systems. In those cases where higher drive is needed, external buffers can be added.

5.8 Intel386 EX Processor Local Bus Interface

The R380EX connects directly to the Intel386 EX processor local bus. There are three types of bus cycles from the Intel386 EX processor, and the R380EX supports them all:

- LBA cycles
- LDEV cycles, and
- Bus cycles handled by the R380EX, including:
 - DRAM references
 - Intel386 EX processor initiated Refresh
 - Internal registers
 - ISA bus cycles
 - Halt/shutdown
 - Interrupt Acknowledge
 - DMA cycle

5.9 LBA Cycles

The Intel386 EX processor initiates and controls LBA cycles which are indicated by the assertion of LBA#. LBA cycles designate accesses either to the internal Intel386 EX processor peripherals, or devices selected by the Intel386 EX processor chip-select unit. LBA# cycles are terminated by the Intel386 EX processor asserting READY# itself.

If the LBA cycle address is in the range defined by the R380EX BIOS Control Register, the R380EX will assert CE_BIOS#. This allows CE_BIOS# to be used during initial power-up, before the BIOS has been able to configure the R380EX. However, the R380EX will never assert WE_FLASH# during an LBA# cycle, and thus will help prevent inadvertent reprogramming of the flash.

5.10 LDEV Cycles

LDEV# cycles are primarily controlled by another local bus device and are denoted by the assertion of LDEV# by the local bus device (such as a video controller). In this case, the local bus device must meet the Intel386 EX processor READY timing and drive READY directly with a 3-state driver. These cycles can be any type of cycle (read, write, I/O, or memory). The R380EX only monitors these cycles but does not act on them.

5.11 Power Management

The R380EX contains some basic support for System Management Mode (SMM) and for power management of the system environment. The R380EX allows the system designer to pursue several different power conservation strategies individually or in combination. The R380EX contains all of the Halt detection logic, SMI generation logic, and glitchless clock switching logic to perform these functions:

- Application or OS level software can issue a Halt instruction to place the system into the low power mode described in the Halt/shutdown section.
- Software can write to the Clock/Reset Control Register to reduce the Intel386 EX processor's systems clock speed.
- An SMI (System Management Interrupt) can be generated in response to an external event or the R380EX interval timer expiring. The SMI routine can then handle powering down system peripherals or entering the hardware supported Halt state, or reducing the system clock speed.

5.12 SMI and Clock Switching

Some power management software requires support hardware to determine when a system has become inactive. To make response to this condition be as flexible as possible, an SMI interrupt is normally asserted to allow an SMI service routine to decide how to power-down various parts of the system. The R380EX supports this style of power management with several input pins and a single SMI idle latch and timer. If the idle timer is allowed to count down to zero, and the SMI function is enabled, the SMI# pin is asserted, thus alerting the Intel386 EX processor to this condition.

The idle timer is 12 bits wide and may be clocked by either a 1024 hertz or a 16 hertz clock. Both of these frequencies are derived from the RTC_X2 input clock (normally 32,768 hertz). When clocked at 1024 hertz, the idle timer can be set to expire from about 1 millisecond up to a total of about 4 seconds with about 1 millisecond granularity. When clocked at 16 hertz, an idle timer expiration time from about 62.5 milliseconds up to about 256 seconds can be achieved with about a 62.5 millisecond granularity.

The R380EX contains an SMI interrupt output pin. Sources for this interrupt in the R380EX are:

- The idle timer decrementing to zero (if enabled to assert SMI)
- The assertion of either the EXTSMIO or EXTSMII input pins (if enabled to assert SMI)
- The detection of a HALT cycle (when enabled to assert SMI)
- The setting of a software-triggerable SMI Register bit

The EXTSMI[0:1] pins have individual enable register bits, and are useful for things such as a low-battery warning in hand-held applications, and for PCMCIA system-management events.

Software may reduce the CPU/system "CLK2" clock frequency by writing to the Clock/Reset Control Register. This allows the input oscillator clock to be divided by 1, 4, or 16 to supply the CLK2OUT pin. Upon reset, the clock is automatically set to divide by four to allow the system components to easily set and track the bus phase as reset is released. The Intel386 EX processor and other local bus peripherals determine the bus phase by watching for the deassertion of reset. Since the R380EX is responsible for releasing the reset line, it also automatically changes the clock divider control bits to perform a divide by 1 within a few bus cycles after deassertion of RESETCPU. Software may also subsequently set the divider control bits to speed-up or slow-down the clock speed, depending upon whether performance or power conservation is required.

Systems which require even greater power savings can make use of self-refreshing DRAMs, and can use the Digital I/O signals of the R380EX to shutdown power to sections of the hardware.

5.13 Halt or Shutdown

The R380EX can be configured to respond to an Intel386 EX processor Halt cycle in several different ways. It can:

- (1) Return READY.
- (2) Return READY and switch the 2xCPU clock from CLK2OSC source to the 32KHz (RTC_CLK) clock. A subsequent ADS# assertion from the Intel386 EX processor initiates the switch back to the high-speed CLK2OSC source after a programmable delay is satisfied.
- (3) Return READY and generate an SMI event.
- (4) Return READY, generate an SMI event and switch to the 32KHz clock as described in (2) above.

Mode 2 above allows the system designer to bring the whole system power consumption down to a few milliamps, or even less for properly designed systems, but requires the use of self-refresh capable DRAMs.

To achieve the lowest power-consumption, the CPU clock oscillator must be powered down by either the POWERDOWN signal from the Intel386 EX processor or the OSC_OFF# signal from the R380EX. The POWERDOWN signal from the Intel386 EX processor is asserted when a HALT is executed and Power Control Register bits PC1:0 of the Intel386 EX processor are set to the 01b state.

By using the OSC_OFF# signal to disable the oscillator, the Intel386 EX processor does not need to enter its POWERDOWN state, a state in which its CLK2 input is disabled and bus phase information is lost. If the Intel386 EX processor does enter the POWERDOWN state, a PHASE1 signal is also provided by the R380EX to allow local bus peripherals to track the bus phase correctly when the halt state is exited.

If the POWERDOWN state of the Intel386 EX processor is not used, the R380EX still supports a very low power HALT state just by switching the 32KHz clock into the Intel386 EX processor's CLK2 input. This keeps the Intel386 EX processor's power consumption to less than 1mA, even without the Intel386 EX processor going into the POWERDOWN state. In the case where the Intel386 EX processor is placed into the POWERDOWN mode, the R380EX automatically detects any phase change injected by the Intel386 EX processor when it exits the POWERDOWN state by monitoring the assertion of ADS# (guaranteed by the Intel386 EX processor to be asserted during PH1 while it is operated at a 32KHz frequency). The PHASE1 output from the R380EX will also be corrected glitchlessly. Thus the Intel386 EX processor's POWERDOWN mode may also be used as long as the other local bus devices monitor the R380EX's PHASE1 signal and can deal with the phase change as well.

The Intel386 EX processor exits the HALT and/or POWERDOWN state in response to an interrupt. On the first access it makes after returning from the HALT state (when ADS# is detected) a programmable delay of up to 64 milliseconds is used to hold the CPU CLK2 line (CLK2OUT pins) high before switching back to the normal CPU clock oscillator (CLK2OSC pin). This allows the CPU clock oscillator to get back up to normal speed after the POWERDOWN signal has been removed (so that

subsequent DRAM cycles do not violate RAS/CAS pulse widths for example).

When returning from this low power state in a properly designed system, the only state information that needs to be updated should be the time of day which is normally updated as a result of an 8254 timer tick interrupt. Correction of the time of day is facilitated through the use of a HLTS status bit in the R380EX Clock Control Register. This bit is set when a HALT instruction is detected by the R380EX. The time of day timer-tick interrupt may check this bit to see if the time of day needs to be reloaded from the RTC.

In response to a Shutdown bus cycle, the R380EX simply initiates a hardware reset. In this case, both CPURESET and RESETDRV pins are driven asserted for a minimum of 32 CLK2 periods.

5.14 Programmable Chip Selects

The R380EX contains four user-programmable I/O chip selects in addition to those provided by the Intel386 EX processor. The chip selects can be programmed and used individually or they can be "daisy-chained" together to form one extended chip select output that can decode up to four discontinuous regions.

5.15 16-bit Digital I/O Port

The R380EX has a 16-bit digital I/O port, and a 6-bit digital output port. There are four registers associated with the DIO port: the DIO Data Input Register, the DIO Data Output Register, the DIO Direction Control Register, and the DIO Mux Register. The DIO Direction and Mux registers can be initialized at power-up by configuration resistors.

5.16 Data Bus Transceiver Control

A disable signal for a data bus transceiver between the CPU and DRAM is generated to eliminate the possibility of a conflict on the data bus when the CPU transitions from a read to a write cycle in earlier A- and B-step Intel386 EX processors. The transceiver can also provide TTL to CMOS level translation for the Intel386 EX processor. Additionally, it can be used to isolate the DRAM array loading of the data bus.

The Data Enable output may be connected to the OE# input of an optional external data transceiver between the CPU data bus and the DRAM and BIOS data busses. The DIR

input of the transceiver should be connected to the Intel386 EX processor RD# output.

Register control bits in the R380EX can selectively enable this output for accesses to either the DRAM or the BIOS. By providing controls for an external transceiver, this output facilitates using DRAM and/or BIOS chips that have slow output disable times that may encroach into a subsequent Intel386 EX processor write cycle and consequently fight with the CPU data outputs. Typical DRAM output disable timings are good enough that a transceiver is not recommended. However, some EPROMs may need it.

6.0 Functional Description of the Intel386™ EX Processor

The Intel386 EX processor is a fully static, 32-bit processor optimized for embedded applications. It features low power and low voltage capabilities, integration of many commonly used DOS-type peripherals, and a 32-bit programming architecture compatible with the large software base of Intel386 processors. The following sections provide an overview of the integrated peripherals.

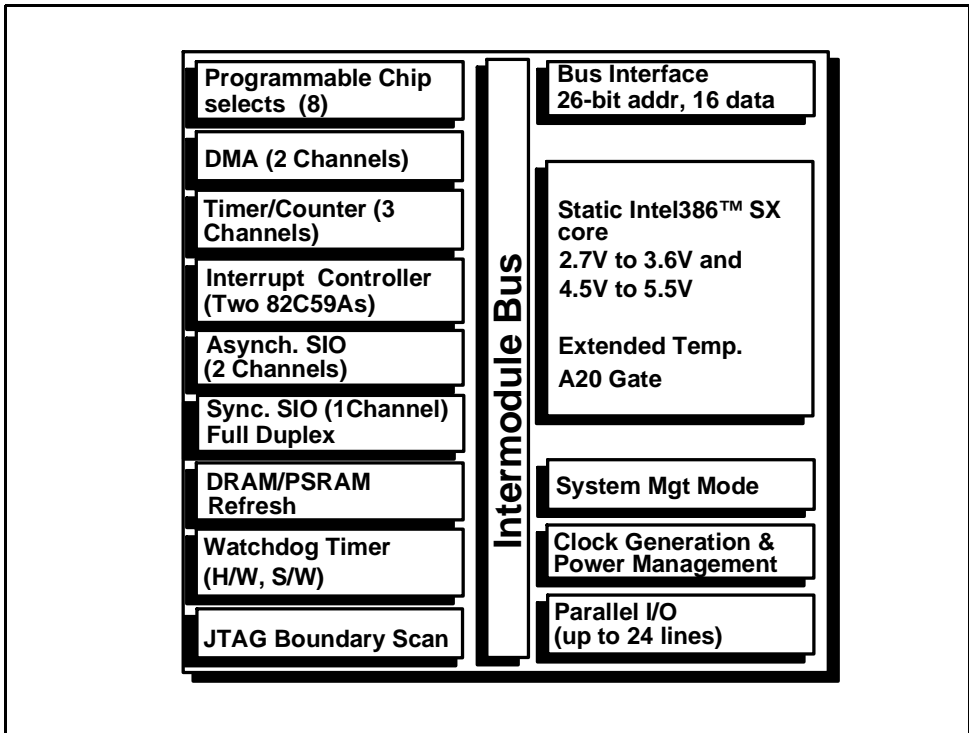


Figure 2. Intel386™ EX Microprocessor Block Diagram

6.1 Clock Generation and Power Management Unit

The clock generation circuit includes a divide-by-two counter. This is a programmable divider designed for generating a prescaled clock (PSCLK), and Reset circuitry. The CLK2 input provides timing for the chip. It is divided by two to generate a 50% duty cycle Phase1 (PH1) and Phase 2 (PH2) for the core and integrated peripherals. For power management, separate clocks are routed to the core (PH1C/PH2C), and the peripheral modules (PH1P/PH2P).

Two Power Management modes are provided within the Intel386 EX processor for flexible power-saving options. During Idle mode, the clocks to the CPU core are frozen in a known state (PH1C low and PH2C high), while the clocks to the peripherals continue to toggle. In Powerdown mode, the clocks to both core and peripherals are frozen in a known state (PH1C low and PH2C high). The Bus Interface Unit will not honor any DMA, DRAM refresh, or HOLD requests in Powerdown mode because the clocks to the entire device are frozen. Additional power management features are available through use of the RadiSys R380EX Embedded System Controller.

6.2 Chip Select Unit

The Chip Select Unit (CSU) decodes bus cycle address and status information and enables the appropriate chip-selects. The individual chip-selects become valid in the same bus state as the address and become inactive when either a new address is selected or the current bus cycle is complete.

The CSU is divided into eight separate chip-select regions, each of which can enable one of the eight chip-select pins. Each chip-select region can be mapped into memory or I/O space.

- A memory-mapped chip-select region can start at zero or on any $2^{(n+1)}$ Kbyte address location (where $n = 0 - 15$, depending upon the mask register).
- An I/O-mapped chip-select region can start at zero or on any $2^{(n+1)}$ byte address location (where $n = 0 - 15$, depending upon the mask register).

The size of the region is also dependent upon the mask used.

Additional I/O chip selects can be provided in this design by the RadiSys R380EX Embedded System Controller.

6.3 Interrupt Control Unit

The Intel386 EX processor's Interrupt Control Unit (ICU) contains two 8259A modules connected in a cascade configuration. The 8259A modules make up the heart of the ICU. These modules are similar to the industry-standard 8259A architecture.

The Interrupt Control Unit directly supports up to ten external (INT9:0) interrupt request signals, and up to eight internal (IR7:0) interrupt request signals. Pending interrupt requests are posted in the Interrupt Request Register, which contains one bit for each interrupt request signal. When an interrupt request is asserted, the corresponding Interrupt Request Register bit is set. The 8259A module can be programmed to recognize either an active-high level or a positive transition on the interrupt request lines. An internal Priority Resolver decides which pending interrupt request (if more than one exists) is the highest priority, based on the programmed operating mode. The Priority Resolver controls the single interrupt request line to the CPU. The Priority Resolver's default priority scheme places IR0 as the highest priority and IR7 as the lowest. The priority can be modified through software.

6.4 Timer/Counter Unit

The Timer/Counter unit on the Intel386 EX processor has the same basic functionality as the industry-standard 82C54 counter/timer. It provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. This maximum frequency must be considered when programming the input clocks for the counters. Six programmable timer modes allow the timers to be used as event counters, elapsed-time indicators, programmable one-shots, and in many other applications. All modes are software programmable.

6.5 Watchdog Timer Unit

The Watchdog Timer (WDT) unit consists of a 32-bit down-counter that decrements every PHIP cycle, allowing up to 4.3 billion count intervals. The WDTOUT pin is driven high for sixteen CLK2 cycles when the down-counter reaches zero (the WDT times out). The WDTOUT signal can be used to reset the chip, to request an interrupt, or to indicate to the user that a ready-hang situation has occurred. The down-counter can also be updated with a user-defined 32-bit reload value under certain conditions. Alternatively, the WDT unit can be used as a bus monitor or as a general-purpose timer.

6.6 Asynchronous Serial I/O Unit

The Intel386 EX processor's asynchronous serial I/O (SIO) unit is a Universal Asynchronous Receiver/Transmitter (UART). Functionally, it is equivalent to the National Semiconductor NS16450 and INS8250. The Intel386 EX processor contains two asynchronous serial channels.

The SIO unit converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the CPU to serial data. The CPU can read the status of the serial port at any time during its operation. The status information includes the type and condition of the transfer operations being performed and any errors (parity, framing, overrun, or break interrupt).

Each asynchronous serial channel includes full modem control support (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#) and is completely programmable. The programmable options include character length (5, 6, 7, or 8 bits), stop bits (1, 1.5, or 2), and parity (even, odd, forced, or none). In addition, it contains a programmable baud rate generator capable of DC to 512 Kbaud.

6.7 Synchronous Serial I/O Unit

The Synchronous Serial I/O (SSIO) unit provides for simultaneous, bi-directional communications. It consists of a transmit channel, a receive channel, and a dedicated baud rate generator. The transmit and receive channels can be operated independently (with different clocks) to provide non-lockstep, full-duplex communications; either channel can originate the clocking signal (Master Mode) or receive an externally generated clocking signal (Slave Mode).

The SSIO provides numerous features for ease and flexibility of operation. With a maximum clock input of 12.5 MHz to the baud rate generator (assuming 25Mhz device operation), the SSIO can deliver a baud rate of 6.25 Mb/s per second. Each channel is double buffered. The two channels share the baud rate generator and a multiply-by-two transmit and receive clock. The SSIO supports 16-bit serial communications with independently enabled transmit and receive functions and gated interrupt outputs to the interrupt controller.

6.8 Parallel I/O Unit

The Intel386 EX processor has three 8-bit, general-purpose I/O ports. All port pins are bi-directional, with CMOS-level input and outputs. All pins have both a standard operating mode and a peripheral mode (a multiplexed function), and all have similar sets of control registers located in I/O address space. Additional bi-directional I/O ports in this design can be provided by the RadiSys R380EX Embedded System Controller.

6.9 DMA and Bus Arbiter Unit

The Intel386 EX processor's DMA controller is a two-channel DMA; each channel operates independently. Within the operation of the individual channels, several different data transfer modes are available. These modes can be combined in various configurations to provide a very versatile DMA controller. Its feature set has enhancements beyond the 8237 DMA family; however, it can be configured such that it can be used in an 8237-like mode. Each channel can transfer data between any combination of memory and I/O with any combination (8 or 16 bits) of data path widths. An internal temporary register that can disassemble or assemble data to or from either an aligned or a nonaligned destination or source optimizes bus bandwidth.

The bus arbiter, a part of the DMA controller, works much like the priority resolving circuitry of a DMA. It receives service requests from the two DMA channels, the external bus master, and the DRAM Refresh controller. The bus arbiter requests bus ownership from the core and resolves priority issues among all active requests when bus mastership is granted.

Each DMA channel consists of three major components: the Requester, the Target, and the Byte Count. These components are identified by the contents of programmable registers that define the memory or I/O device being serviced by the DMA. The Requester is the device that requires and requests service from the DMA controller. Only the Requester is considered capable of initializing or terminating a DMA process. The Target is the device with which the Requester wishes to communicate. The DMA process considers the Target a slave that is incapable of controlling the process. The Byte Count dictates the amount of data that must be transferred.

In this design, the RadiSys R380EX Embedded System Controller supports fly-by DMA transactions between memory and I/O.

6.10 Refresh Control Unit

The Refresh Control Unit (RCU) simplifies dynamic memory controller design with its integrated address and clock counters. Integrating the RCU into the processor allows an external DRAM controller to use chip-selects, wait state logic, and status lines.

The Intel386 EX processor's RCU consists of four basic functions. First, it provides a programmable-interval timer that keeps track of time. Second, it provides the bus arbitration logic to gain control of the bus to run refresh cycles. Third, it contains the logic to generate row addresses to refresh DRAM rows individually. And fourth, it contains the logic to signal the start of a refresh cycle.

Additionally, it contains a 13-bit address counter that forms the refresh address, supporting DRAMs with up to 13 rows of memory cells (13 refresh address bits). This includes all practical DRAM sizes for the Intel386 EX processor's 64 Mbyte address space.

In this design, the internal DRAM refresh system in the R380EX Embedded System Controller is utilized rather than the Intel386 EX processor's.

6.11 JTAG Boundary Scan Unit

The JTAG Boundary Scan Unit provides access to the device pins and to a number of other testable areas on the device. It is fully compliant with the IEEE 1149.1 standard and thus interfaces with five JTAG-dedicated pins: TRST#, TCK, TMS, TDI, and TDO. It contains the Test Access Port (TAP) finite-state machine, a 4-bit instruction register, a 32-bit identification register, a single-bit bypass register, and an 8-bit test mode register. The JTAG unit also contains the necessary logic to generate clock and control signals for the chains that reside outside the JTAG unit itself: the SCANOUT and Boundary Scan chains.

6.12 Interval Timers

The 8254 Timer/Counter's three channels are configured with a 1.190MHz input clock derived from the 66MHz input clock. The Timer 0 output is internal connected to IRQ0 to provide a standard timer interrupt. The remaining two channels, Timer 1 and Timer 2 are available to specific applications.

Timer 1 is not needed as the refresh timer, since the Intel386 EX processor has a dedicated refresh unit, however, in the Embedded PC Reference Design, the R380EX's internal

refresh unit is used to perform a CAS before RAS refresh cycle.

6.13 Port 92

Port 92 controls the internal A20GATE signal and generates a CPU-only reset to the core. The RadiSys R380EX generates a RESETCPU when a SHUTDOWN cycle is detected.

6.14 Watchdog Timer

The Watch Dog Timer signal is routed to the RadiSys R380EX where, under software control, it can be used to generate a RESETCPU and a RESETDRV for the ISA bus.

6.15 SIO 0 & 1

The serial ports are mapped to I/O addresses 3F8h-3FFh (COM1) and 2F8h-2FFh (COM2) are connected to IRQ4 and IRQ3, respectively. COM1 and COM2 are a full RS232 ports. These ports are consistent with the PC's implementation.

When the floppy disk controller is used in DMA mode, the COM2 driver must be disabled because of the re-assignment of the COM2 RXD and TXD pin functions to the DRQ1 and DACK1 pin functions necessary for DMA.

7.0 I/O Devices

The Embedded PC Reference Design uses both internal and external I/O mapped peripherals. Some external devices require a chip select, while others perform the address decode themselves.

The standard internal peripherals include the Interrupt Controllers, Interval Timers, SIOs, and Port 92. Each are briefly described in the following subsections. Refer to the *Intel386™ EX Embedded Microprocessor User's Manual* (272485) for full descriptions.

7.1 I/O Map

As can be seen in Table 1, the Embedded PC Reference Design includes all of the standard peripheral devices needed to make a complete embedded PC. Some of these peripherals are embedded within the Intel386 EX processor itself while others are part of the RadiSys R380EX or other devices.

Table 1. Reference Design I/O Map

Chip Select	Device	Address Range (HEX)
Intel386 EX Processor Internal	PIC 0	0020-0021
Intel386 EX Processor Internal	Address Configuration Register	0022-0023
R380EX	R380 Internal Address Register	0024
R380EX	R380 Internal Data Register	0026
Intel386 EX Processor Internal	Timers 0-2	0040-0043
R380EX	Keyboard/Mouse Controller	0060,0064
R380EX	RTC & CMOS RAM	0070-0071
Intel386 EX Processor Internal	Port 92	0092
Intel386 EX Processor Internal	PIC 1	00A0-00A1
R380EX	IDE CS0	01F0-01F7
Intel386 EX Processor Internal	COM2	02F8-02FF
Super I/O	Parallel Port	378-37B
Super I/O	Floppy Disk Controller	3F0-3F7
GD6245	LCD VGA Controller	03B0-03DF, 46E8
PD6710	PCMCIA Controller.	03E0-03E1
R380EX	IDE CS1	03F6-03F7
Intel386 EX Processor Internal	COM1	03F8-03FF
Intel386 EX Processor Internal	Chip Configuration	F400-F85F
Intel386 EX Processor Internal	Chip Configuration	F875-F8FF

7.1.1 External I/O

This Embedded PC Reference Design includes interfaces to external peripherals. These include interfaces to the LCD VGA controller, floppy disk drive, an IDE hard disk, a buffered PCMCIA slot, and PC/104 and ISA Bus connectors. Provision is also included for connection of an external RTC, and/or an external keyboard/mouse controller.

7.1.2 Keyboard/mouse

The R380EX includes an internal keyboard/mouse controller. The Embedded PC Reference Design includes provisions for use of either the internal keyboard/mouse controller or an external keyboard/mouse controller like the Intel 82C42PE microcontroller.

The external Intel 82C42PE microcontroller provides a PS/2 style keyboard/mouse interface and resides on the ISA bus. The R380EX asserts the keyboard chip select whenever I/O address 60h or 64h is accessed regardless of whether the internal or external keyboard controller is selected. The R380EX internal keyboard/mouse controller is PC-compatible and also is configured for I/O space 60h and 64. In either case, the keyboard interrupt is connected to IRQ1 and the mouse interrupt to IRQ12/13 (IRQ12 is used in a PC).

7.1.3 RTC

The R380EX includes an internal real-time clock and 14 bytes of battery backed RAM. The Embedded PC Reference Design includes provisions for use of either the internal RTC and RAM, or an external RTC and RAM like the DS12887

An external Dallas Semiconductor DS12887 resides on the ISA bus and provides the real-time clock and the battery backed RAM function normally used in a PC environment. RTC_AS and RTC_DS are generated by the RadiSys R380EX in order to access the external RTC. Both the internal and external RTC are accessed at I/O 70-71h. The RTC interrupt is connected to IRQ8.

7.1.4 IDE

Two IDE interfaces are included in the Embedded PC Reference Design. An enhanced IDE interface is provided by the R380EX and a regular one by the FDC37C665 Super I/O chip.

The R380EX IDE interface is configured for I/O addresses 3F6-3F7h with the R380EX's CS0# as HST_CS1# and, I/O addresses 1F0-1F7h, with the R380EX's CS1# as HST_CS0#. The RadiSys R380EX is used to control data bus transceivers and uses (IOCS16#) to determine the access time and the Intel386 EX processor's bus sizing.

The FDC37C665's IDE interface is essentially identical to the R380EX's interface except that the R380EX has an enhanced IDE interface where the FDC37C665 is a regular IDE interface. Only one of the two interface should be enabled at a time.

The IDE interrupt is tied to IRQ14.

7.1.5 LCD VGA

The display section uses the Cirrus Logic CL-GD6245, single chip LCD VGA Controller that includes a RAMDAC and a frequency synthesizer. This supports VGA and SVGA functionality with screen resolutions from 640x480 in 256 colors up to 1024x768 in 16 colors. It also supports a variety of 640x480 LCDs, including: dual- and single-scan color or monochrome STN displays, 9-, 12-, and 18-bit color TFT, and multi-shade monochrome TFT displays. Three operation modes support VGA only, LCD only, and simultaneous VGA and LCD display. The design uses one 256K x 16 DRAM to provide a 512KB frame buffer.

The controller resides on the ISA bus. The memory and I/O space used by the VGA controller is a function of its configuration.

7.1.6 PCMCIA Controller

A Cirrus Logic CL-PD6710 is used to support one buffered PCMCIA card slot. Its control registers are mapped to I/O locations 3E0-3E1h and performs its own decode.

8.0 Hardware Interrupts

The interrupt mapping is close to that of a PC. Table 2 shows this mapping and where it deviates from a standard PC implementation. Note that the PC6710 PCMCIA controller is connected to several interrupts but the actual interrupt used is configured in software.

Table 2. Interrupt Mapping

PC INT #	IRQx	Vector (hex)	Name	PC Use
2	NMI	8	Shutdown	Parity Error/IOCHK
8	IRQ0	20	Timer 0	same
9	IRQ1	24	Keyboard	same
A	IRQ2	28	cascade vector	same
B	IRQ3	2C	PD6710, COM2	COM2
C	IRQ4	30	PD6710, COM1	COM1
D	IRQ5	34	PD6710, IRQ5,	LPT2
E	IRQ6	38	FDC	FDC
F	IRQ7	3C	PD6710, LPT1	LPT1
70	IRQ8	1C0	RTC	same
71	IRQ9	1C4	PD6710, IRQ9	VGA
72	IRQ10	1C8	PD6710, ISA	ISA
73	IRQ11	1CC	PD6710, ISA	ISA
74	IRQ12	1D0	PD6710, DMA	Mouse
75	IRQ13	1D4	Mouse	Num. Co-Proc.
76	IRQ14	1D8	IDE or PD6710, IRQ9	HDC
77	IRQ15	1DC	WDT	ISA

9.0 Additional Design Features

In addition to the features described above, the Embedded PC Reference Design includes circuitry for additional features which are often useful in embedded designs.

9.1 Intel Flash with Flash File System

The Embedded PC Reference Design includes circuitry to include an Intel 28F016 or 28F032 Flash device which could be used in a flash file system configuration. CS6# from the Intel386 EX processor is used as the chip select for this device.

9.2 3.3V Operation

Various portions of this design can be configured for 3.3V or 5V operation. This includes the Intel386 EX processor, RadiSys R380EX in particular. Other sections of the design should be carefully examined to ensure proper operation at reduced voltage.

9.3 POST Code Display and Logic Analyzer Connections

Two particularly useful aspect of the Embedded PC Reference Design during system debug are the included POST code displays and the logic analyzer connection points. Debugging both the hardware and software system of this board is simplified because of their inclusion

9.4 ISA Bus and PC/104 Bus

This design includes both ISA Bus and PC/104 bus interfaces which allow both regular “off the shelf” desk top PC cards as well as industrial embedded PC cards to be connected to the board for development and testing.

9.5 Ethernet

Because Ethernet is an important building block for embedded designs, an additional schematic page is included as an example of how to add Ethernet to this design.

9.6 System BIOS

In order to test the Embedded PC Reference Design, a Phoenix Technologies Ltd.* PicoBIOS* was modified to support the RadiSys R380EX. This BIOS is similar to a standard PC BIOS with support for the RTC, PS/2 style mouse/keyboard and the integrated VGA controller. The additional support required included configuring the Intel386 EX processor, the RadiSys R380EX, the Cirrus Logic GD6245 LCD VGA Controller and the Cirrus Logic PD6710 PCMCIA Controller. Flash ROM utilities were also added to the evaluation board.

9.7 IC Works W48C54A-59 Frequency Generator

The IC Works* W48C54A-59* mask option is particularly useful in Intel386 EX processor and R380EX-based embedded systems. This chip provides all of the proper frequencies needed in a system and includes two key features: fast startup time, and proper clock frequency for the serial channels. By using this part in conjunction with the R380EX, the R380EX's clock restart delay can be set for the 2mS delay, rather than the 8mS or 64mS delay required by other oscillators when restarting from being powered-down.

10.0 Summary

The Embedded PC Reference Design has been built, debugged and tested in order to provide a known working design as a starting point for Intel386 EX Processor and R380EX Embedded System Controller based PC-compatible designs.

This application note covers the features of the EXPLR2 Embedded PC Reference Design and highlights the most important features of the Intel386 EX and R380EX chips for use in building a DOS-compatible embedded system. The Intel386 EX Processor is a highly integrated embedded CPU which incorporates key peripheral components to form a cost effective, compact system for embedded PC applications. When coupled with the R380EX, this combination enables designers to create fully DOS compatible systems from long lived embedded components.

This application note also describes other key technologies which are incorporated in the Reference Design including Intel Boot Block Flash memory, PCMCIA and LCD VGA controllers from Cirrus Logic, and power management

features of the Intel386 EX processor and R380EX combination.

Using this proven design as a base for a custom PC-compatible system provides a head-start in product development which can result in faster time to market.

11.0 Highlights of Other System Components

11.1 The IC Works W48C54A-59 Frequency Generator

The IC Works W48C54A-59 is a custom W48C54A mask option designed for use with RadiSys embedded system controllers. This mask option features fast start-up frequency stabilization. Using this chip, the R380EX oscillator re-start delay can be set for the 2mS delay rather than the 8mS or 64mS delay required for most oscillators to stabilize.

This dual VCO clock synthesizer device accepts direct connection to a 14.318 MHz quartz crystal at the X1 and X2 pins and produces 24 MHz, 12 MHz and 1.843 MHz fixed clock outputs, as well as providing a selectable clock output (see Table 3, below). It can be operated with a 3.3V or 5V power supply.

Table 3. Output Frequency Selection

Select Address		Ratio	CLKOUT (MHz)
FS1	FS0		
0	0	42/12	50.113
0	1	56/12	66.817
1	0	31/12	40.568
1	1	28/12	33.409

For further information on W48C54A devices consult the *IC WORKS W48C54A/55A* data sheet.

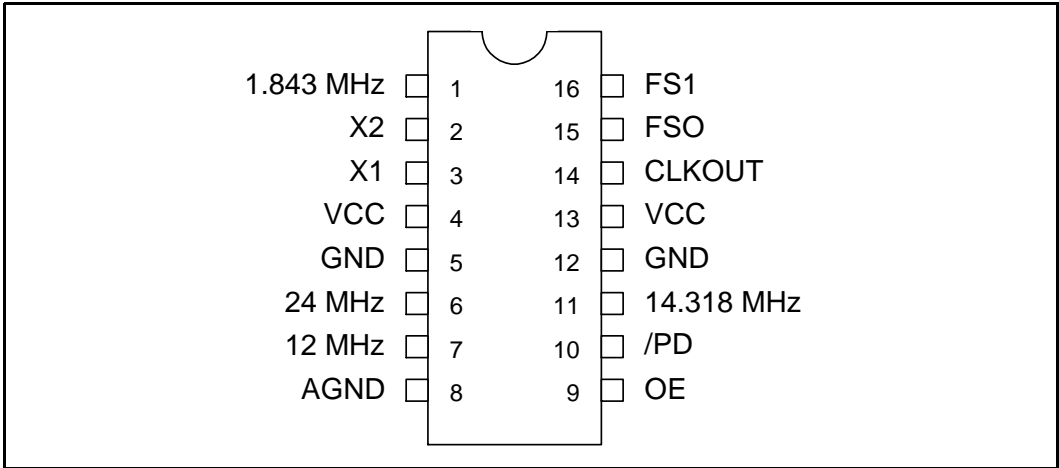


Figure 3. IC Works W48C54A-59 Pinout

11.2 Intel's SmartVoltage Boot Block Flash

11.2.1 Product Highlights

- 2-, 4- and 8-Mbit x8 or x8/x16 JEDEC-standard configuration
- Footprint upgradable from 2-Mbit through 8-Mbit
- SmartVoltage technology
 - Voltage flexibility
 - 3.3V low power read
 - Superior single 5V read/write performance
 - 2.7V read option
- Faster programming performance over 5V only
 - Lower throughput time
 - Lower manufacturing costs
- High performance read
 - 60nS at 5V
 - 110nS at 3.3V
 - 120nS at 2.7V
- Superior byte write performance for EEPROM emulation
- Absolute hardware write protection with $V_{pp}=0$
- Automated algorithm for user transparent erase/program

- Reset and deep-powerdown mode (0.2
- Widely-sourced packaging and architecture
- Optimized memory block architecture
- Ideal for ROM, EEPROM and Bulk Flash EPROM integration for embedded application

11.2.2 Product Description

Intel's advanced SmartVoltage™ 2-, 4- and 8-Mbit flash memories offer users optimal benefits in a mid-density flash. Using a cost-effective and highly advanced process technology, the SmartVoltage 2-, 4- and 8-Mbit products offer new capabilities in establishing a standard in flash memory. You can choose among read/write voltages, x8 or x8/x16 data bus, hardware reset, high performance read access, transparent automated erase/program algorithms and absolute write protection.

The SmartVoltage 2-, 4- and 8-Mbit memory architecture is ideal for integrating boot ROM, EEPROM-like parameter storage and bulk flash code storage - with optimized memory blocks for each need. Designers can incorporate this tuned architecture in a selection of footprint compatible densities, including 2-Mbit, 4-Mbit and 8-Mbit.

The industry today demands flash memory products that have advanced features, are cost effective, and deliver flexibility and ease of use. Intel delivers these capabilities in 40-pin and greater TSOP and PSOP packages. Plus, only

Intel offers voltage options for standard 5V read, down to 2.7V read for low-power current and future needs in one product offering at no price premium. In addition, Intel offers high-throughput efficiency in manufacturing with 12V programming, and simplicity of board design with 5V writes.

Intel's SmartVoltage 2-, 4-, and 8-Mbit products provide high integration for space-constrained embedded applications, low voltage for portable applications, and absolute block locking for easy system recovery in PC BIOS applications.

11.3 Cirrus Logic CL-GD6245: LCD VGA Controller

11.3.1 Product Highlights

- 176-pin (EIAJ standard) VQFP package
- Direct connection to 16/32-bit VESA* VL-Bus(TM)
- Supports dual-scan color STN LCD
- SimulSCAN* up to 640 x 480 x 256 colors with 0.5-Mbyte DRAM
- Supports single- and dual-scan monochrome STN LCD
- Supports mixed-voltage (3.3 and 5 V) operation
- Windows* performance-improvement features
- Supports 9-, 12-, 15-, and 18-bit color TFT LCD
- CRT resolutions up to 1024 x 768 with 16 colors or 800 x 600 with 256 colors
- 64 shades of gray or 256 colors at 640 x 480 on LCD
- Simultaneous CRT and LCD operation (SimulSCAN(TM)) in all configurations
- Low-power CMOS technology

11.3.2 Product Description

The CL-GD6245 is a high-performance single-chip LCD VGA controller optimized for subnotebook computers. The low-profile (1.3 mm high) 176-pin VQFP package is ideal

for double-sided board assembly to reduce form factor. Direct connection to 16/32-bit VESA VL-Bus further reduces component count for '486-based designs. SimulSCAN is available with dual-scan color STN displays up to 640 x 480 with 256 colors using only one 256K x 16 DRAM.

11.4 Cirrus Logic CL-PD6710: PC Card Host Adapters

11.4.1 Product Highlights

- Single-chip PC Card (PCMCIA) host adapters
- Compliant with PCMCIA 2.1 and JEIDA 4.1
- 82365SL-compatible register set, ExCA@-compatible
- Suspend mode for lowest power consumption
- Five programmable memory windows per socket
- Two programmable I/O windows per socket
- Programmable card access cycle timing
- Direct connection to ISA (PC AT) and PC Card sockets
- 8- or 16-bit CPU and PC Card interfaces
- ATA disk interface support
- Mixed-voltage (3.3 and 5 V) operation
- Single-socket 144-pin VQFP (CL-PD6710) for smallest form factor
- Dual-socket 208-pin PQFP (CL-PD6720 and CL-PD6722)

11.4.2 Product Description

The CL-PD6710 is a single-chip PC Card host adapter devices capable of controlling one PC Card socket. This device is fully compliant with PCMCIA 2.1 and JEIDA 4.1 and is optimized for use in notebook computers where reduced form factor and low power consumption are critical design objectives. With the CL-PD6710, a complete PC Card solution with card-power circuitry can occupy as little as 1.5 square inches (excluding the connector).

11.5 The SMC91C94 Ethernet Controller

11.5.1 Product Highlights

The SMC91C94* Ethernet Controller is from Standard Microsystems Corporation* (SMC). Features:

- ISA/PCMCIA Single-Chip Ethernet Controller
- 4608 Bytes of On-Chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Simultasking - Early Transmit and Early Receive Functions
- Hardware Memory Management Unit
- Optional Configuration via Serial EEPROM Interface (Jumperless)
- Single +5V Power Supply
- Low Power CMOS Design
- 100 Pin QFP and TQFP Packages

Bus Interface:

- Direct Interface to ISA and PCMCIA with No Wait States
- Flexible Bus Interface
- 16-Bit Data and Control Paths
- Fast Access Time (40 ns)
- Pipelined Data Path
- Handles Block Word Transfers for Any Alignment
- High Performance Chained (“Back-to-Back”) Transmit and Receive
- Pin Compatible with SMC91C92* in ISA Mode
- Flat Memory Structure for Low CPU Overhead
- Dynamic Memory Allocation Between Transmit and Receive
- Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- Supports Boot PROM for Diskless Applications

Network Interface:

- Integrates 10BASE-T Transceiver Functions:
 - Driver and Receiver
 - Link Integrity Test

- Receive Polarity Detection and Correction
- Integrates AUI Interface
- Implements 10 Mbps Manchester Encoding/Decoding and Clock Recovery
- Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- External and Internal Loopback Modes
- Four Direct Driven LEDs for Status/ Diagnostics

Software Drivers:

- Uses Certified SMC9000* Drivers

11.5.2 Product Description

New ethernet controller chip from Standard Microsystems Corporation (SMC) has PCMCIA interface, on-chip RAM, early transmit/early receive

The SMC91C94 is based on the same architecture and includes all the performance features of the SMC91C92 Ethernet controller, including 4608 bytes of on-chip RAM, with the addition of full PCMCIA and ISA bus compatibility and an optional Simultasking© capability. Simultasking enables information to be sent onto the network and to the CPU's system RAM before a complete packet is received by the controller. Performance improvements of up to 45% over NE2000-compatible controllers are possible.

The fact that the SMC91C94 has on-chip PCMCIA interface logic and embedded RAM in the same small package size as the SMC91C92 (100-pin QFP or TQFP) is a particular advantage in PCMCIA designs where real estate is a critical issue.

In addition to having features in common with the SMC91C92, the SMC91C94 is pin and register-set compatible with the earlier device, giving designers an easy migration path requiring no changes in hardware layout or software drivers. To take full advantage of the improved performance potential, SMC is supplying an enhanced version of the SMC9000 software driver suite which will turn on the Simultasking feature. The SMC91C94, which has all the functionality needed to implement a high-performance 10BASE-T (twisted pair) node, has an AUI port for interfacing to transceivers for 10BASE-5 (thick coax), 10BASE-2 (thin coax) and 10BASE-F (fiber). The device is capable of direct interface, no-wait-state ISA bus operation and occupies 16 I/O locations but no memory space. Jumperless configuration via an

EEPROM serial interface is available and the SMC91C94 supports boot-up from PROM for diskless applications.

11.6 The SMC FDC37C665GT—Advanced High-Performance Multi-Mode Parallel Port Super I/O Floppy Disk Controller

11.6.1 Product Highlights

- Floppy Disk Available on Parallel Port Pins
- 2.88MB Super I/O Floppy Disk Controller
 - Licensed CMOS 765B Floppy Disk Controller
 - Software and Register Compatible to the 82077AA Using SMC's Proprietary Floppy Disk Controller Core
 - Supports Vertical Recording Format
 - 100% IBM Compatibility
 - Detects All Overrun/Underrun Conditions
 - 48 mA Drivers and Schmitt Trigger Inputs
 - DMA Enable Logic
 - Data Rate and Drive Control Registers
 - Swap Drives A and B
 - Non-Burst Mode DMA Option
 - FDC Primary/Secondary Address Selection
 - 16 Byte Data FIFO
 - Low Power CMOS 0.8u Design
- Hardware/Socket Compatible with FDC37C651 and FDC37C661 (Standard and Enhanced Parallel Port Modes)
- Enhanced Digital Data Separator
 - Low Cost Implementation - 24 MHz Crystal
 - No Filter Components Required
 - Ease of Test and Use, Lower System Cost, and Reduced Board Area
 - 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
- Supports Floppy Disk and Tape Drives
- Programmable Precompensation Modes
- Multi-Mode Parallel Port
 - Standard Mode
 - IBM PC/XT, PC/AT, PS/2 Compatible Bidirectional Parallel Port
 - Enhanced Mode
 - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 Compliant
 - High Speed Mode
 - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) Compliant
 - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
 - Provides Backdrive Current Protection
 - 24 mA Output Drivers
 - Two Parallel Port Interrupt Pins
- Serial Ports
 - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
 - MIDI Compatible
 - Programmable Baud Rate Generator
 - Modem Control Circuitry
- IDE Interface
 - On-Chip Decode and Select Logic Compatible with IBM PC/XT and PC/AT Embedded Hard Disk Drives
 - IDE Primary/Secondary Address Selection
- Supports Four Floppy Drives Directly (Standard and Enhanced Modes)
- General Purpose 11 Bit Address Decoder
- 100 Pin QFP Package

12.0 Contact Information

12.1 Intel Corporation

For Intel Customer Support in US and Canada, call 800-628-8686. Documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation Literature Sales
 P.O. Box 7641
 Mt. Prospect IL 60056-7641
 1-800-548-4725

Web Site: <http://www.intel.com>

Table 4. Related Intel Documents

Document Title	Order #
<i>Intel386™ EX Embedded Microprocessor User's Manual</i>	272485
<i>Intel386™ EX Embedded Microprocessor datasheet</i>	272420
<i>Intel386™ SX Microprocessor Programmer's Reference Manual</i>	240331
<i>Intel386™ SX Microprocessor Hardware Reference Manual</i>	240332
<i>Intel Development Tools handbook</i>	272520

12.2 RadiSys Corporation

For RadiSys Corporation product information please contact:

RadiSys Corporation
 15025 S.W. Koll Parkway
 Beaverton, OR 97006-6056
 Toll Free: 800-950-0044
 Tel: 503-646-1800
 Fax: 503-646-1850

Web Site: <http://www.radisys.com>

12.3 IC Works

For IC Works product information please contact:

IC Works, Inc.
 3725 North First Street
 San Jose, CA 95134-1700
 Tel: 408-922-0202
 Fax: 408-922-0833

12.4 Cirrus Logic

For Cirrus Logic product information please contact:

Cirrus Logic
 3100 West Warren Avenue
 Fremont, CA 94538
 Tel: 510-623-8300
 Fax: 510-252-6020

Web Site: <http://www.cirrus.com>

12.5 SMC

For SMC product information please contact:

Standard Microsystems Corporation
 SMC - Headquarters
 Hauppauge, NY
 Phones: 800-SMC-4-YOU
 516-435-6000
 Fax: 516-273-1803

Web Site: <http://www.smc.com>

