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APPLICATION NOTE

EXPLR1 Embedded PC Evaluation Platform Application Note

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FIGURES

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1.0 INTRODUCTION

The EXPLR1 Embedded PC Evaluation Platform, developed as a working design, enables shorter design cycles by providing a proven platform as a starting point. The EXPLR1 board was designed by RadiSys* for Intel and highlights the features of the embedded Intel386™ EX Processor and Intel Boot Block Flash Memory, and the RadiSys R300EX Memory/Bus Controller. The EXPLR1 Reference Design Kit can be used "as is" or as a building block to enhance a specific solution.

The Intel386 EX processor is a single-chip "system" which employs a static Intel386 Cx processor core and a host of integrated peripherals, including DMA and interrupt controllers, serial and parallel ports, chip selects, timers/counters, JTAG, and power/system management features. Its 26-bit addressing provides a large 64 Mbyte memory address space. EXPLR1 incorporates additional technologies for use as building blocks for a myriad of applications. Since the EXPLR1 design utilizes the highly integrated Intel386 EX processor, it does not require a standard PC chip set. The RadiSys R300EX Memory/Bus Controller is used for DRAM control and for the generation of more complex, fully timing qualified chip enables and expansion signals.

This design includes the features required for most DOS* and Windows* based embedded PC applications. It is self-contained with expansion capabilities via a single PCMCIA slot. The design generates a general purpose Synchronous Expansion Bus (SEB), attached to the CPU. Command strobes (IOR#, IOW#, MEMW#, MEMR#, BALE) are generated while status inputs (IOCHRDY, IOCS16#, MEMCS16#) are used in a way similar to the ISA bus. The design uses the SEB to interface to the LCD/SVGA graphics controller (Cirrus Logic GD6245), PCMCIA controller (Cirrus Logic PD6710), the IDE disk interface, the RTC (DS12887) and the keyboard/mouse controller (Intel 82C42PE).

Section 14.0, RELATED INFORMATION (pg. 14-24) contains a list of documents containing detailed information about the Intel386 EX processor and EXPLR1.

2.0 EXPLR1 PRODUCT DESCRIPTION

The EXPLR1 Embedded PC Evaluation Platform is DOS compatible and uses a standard PC-like BIOS. It features several products and technologies:

- Embedded Intel386 EX Processor
- Intel 4 Mbyte Boot Block Flash Memory
- RadiSys R300EX Memory/Bus Controller
- PCMCIA Slot

The EXPLR1 platform's functional features include:

- Pipelined, zero wait state, page mode operation
- 1, 4, or 16 Mbytes using standard DRAM SIMM, 2, or 8 Mbytes using a single-RAS DRAM SIMM
- One x32 SIMM socket
- LCD/SVGA Local Bus Graphics Controller (512KB DRAM frame buffer)
- Support for color and monochrome LCDs
- RTC with Extended Battery Backed RAM
- PS/2 Style Keyboard and Mouse Interface
- IDE Hard Disk Drive Interface
- PCMCIA 2.0 (single slot)
- Two Asynchronous Serial Ports (COM1 and COM2)
- Synchronous Expansion Bus and Digital I/O signals on headers

The features of the Intel386 EX processor are used extensively to minimize the requirement for a standard chip set and external logic. The interrupt controller, chip select unit, wait state generator, SIOs, parallel I/O ports and dynamic bus sizing are all used.

NOTE:

Although this is a complete functional unit, the design is modular, allowing for addition and modification of features to meet the specific requirements of a target application.

3.0 FUNCTIONAL BLOCK DIAGRAM

Figure 1 shows the EXPLR1 Platform block diagram.

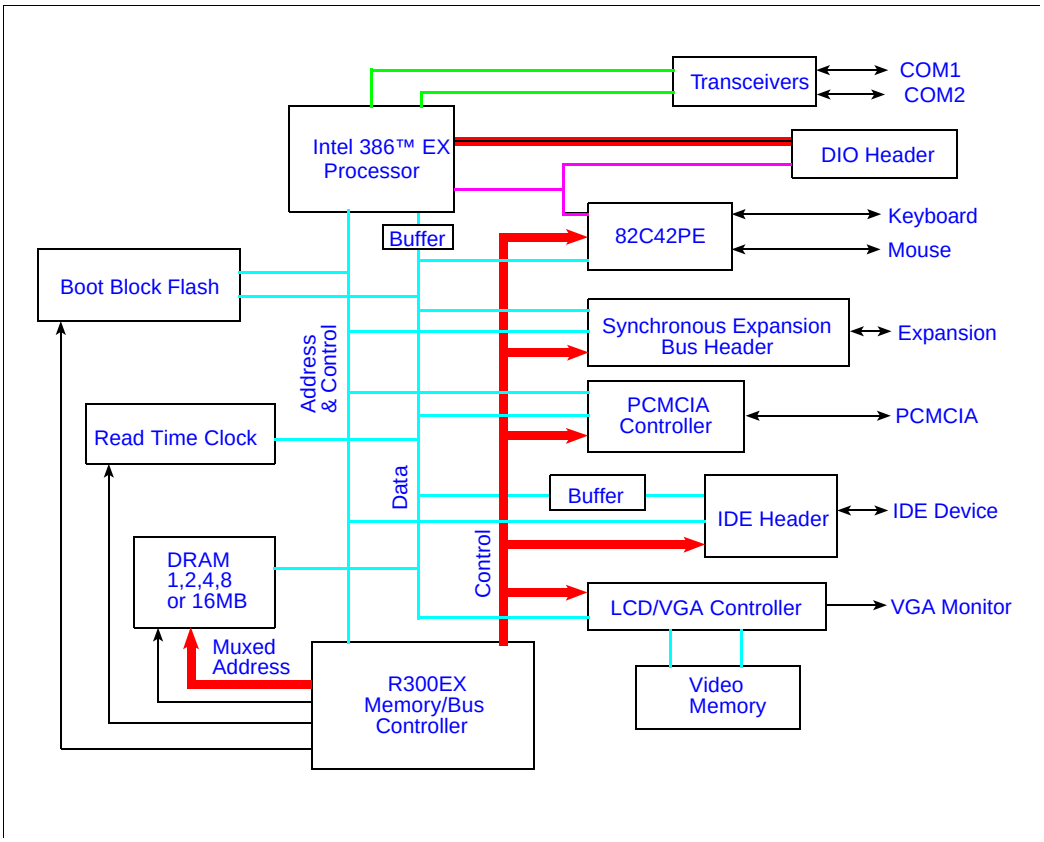


Figure 1. EXPLR1 Embedded PC Evaluation Platform Functional Block Diagram

4.0 FUNCTIONAL DESCRIPTION OF THE INTEL386 EX MICROPROCESSOR

The Intel386 EX processor (Figure 2) is a fully static, 32-bit processor optimized for embedded applications. It features low power and low voltage capabilities, integration of many commonly used DOS-type peripherals, and a 32-bit programming architecture compatible with the large software base of Intel386 processors. The following sections provide an overview of the integrated peripherals.

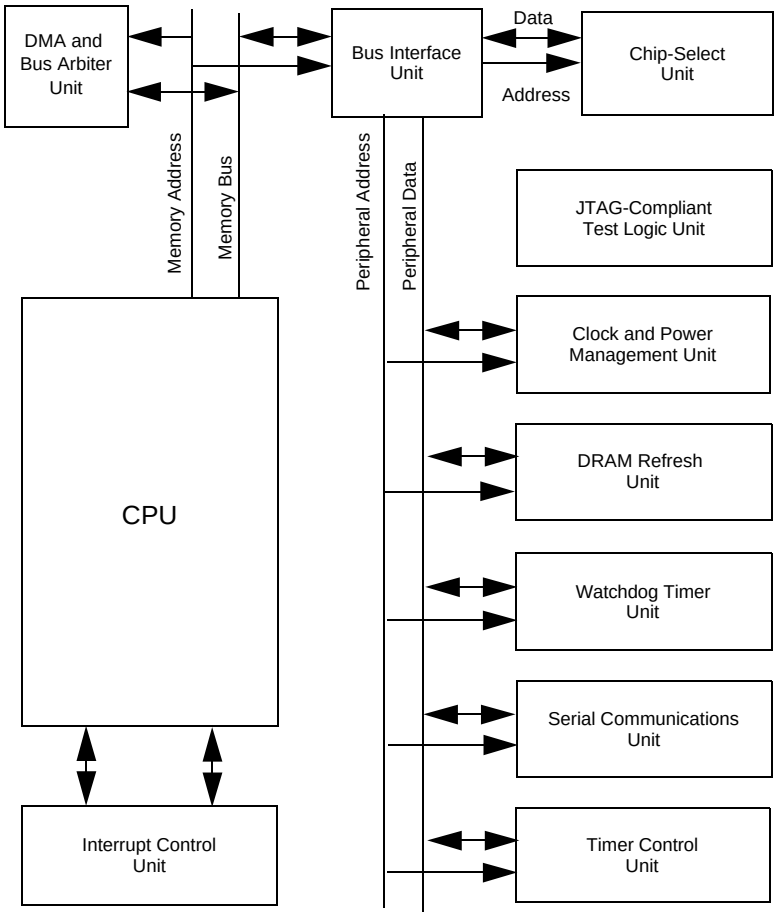


Figure 2. Intel386™ EX Microprocessor Block Diagram

4.1 Clock Generation and Power Management Unit

The clock generation circuit includes a divide-by-two counter. This is a programmable divider designed for generating a prescaled clock (PSCLK), and Reset circuitry. The CLK2 input provides timing for the chip. It is divided by two to generate a 50% duty cycle Phase1 (PH1) and Phase 2 (PH2) for the core and integrated peripherals. For power management, separate clocks are routed to the core (PH1C/PH2C), and the peripheral modules (PH1P/PH2P).

Two Power Management modes are provided for flexible power-saving options. During Idle mode, the clocks to the CPU core are frozen in a known state (PH1C low and PH2C high), while the clocks to the peripherals continue to toggle. In Powerdown mode, the clocks to both core and peripherals are frozen in a known state (PH1C low and PH2C high). The Bus Interface Unit will not honor any DMA, DRAM refresh, or HOLD requests in Powerdown mode, because the clocks to the entire device are frozen.

4.2 Chip Select Unit

The Chip Select Unit (CSU) decodes bus cycle address and status information and enables the appropriate chip-selects. The individual chip-selects become valid in the same bus state as the address and become inactive when either a new address is selected or the current bus cycle is complete.

The CSU is divided into eight separate chip-select regions, each of which can enable one of the eight chip-select pins. Each chip-select region can be mapped into memory or I/O space.

- A memory-mapped chip-select region can start on zero or on any $2^{(n+1)}$ Kbyte address location (where n = 0–15, depending upon the mask register).
- An I/O-mapped chip-select region can start on zero or on any $2^{(n+1)}$ byte address location (where n = 0–15, depending upon the mask register).

The size of the region is also dependent upon the mask used.

4.3 Interrupt Control Unit

The Intel386 EX processor's Interrupt Control Unit (ICU) contains two 8259A modules connected in a cascade mode. The 8259A modules make up the heart of the ICU. These modules are similar to the industry-standard 8259A architecture.

The Interrupt Control Unit directly supports up to eight external (INT7:0) interrupt request signals, and up to eight internal (IR7:0) interrupt request signals. Pending interrupt requests are posted in the Interrupt Request Register, which contains one bit for each interrupt request signal. When an interrupt request is asserted, the corresponding Interrupt Request Register bit is set. The 8259A module can be programmed to recognize either an active-high level or a positive transition on the interrupt request lines. An internal Priority Resolver decides which pending interrupt request (if more than one exists) is the highest priority, based on the programmed operating mode. The Priority Resolver controls the single interrupt request line to the CPU. The Priority Resolver's default priority scheme places IR0 as the highest priority and IR7 as the lowest. The priority can be modified through software.

Besides the eight interrupt request inputs available to the Intel386 EX microprocessor, additional interrupts can be supported by cascaded external 8259A modules. Up to four external 8259A units can be cascaded to the master through connections to the INT3:0 pins. In this configuration, the interrupt acknowledge (INTA#) signal can be decoded externally using the ADS#, D/C#, R/W#, and M/IO# signals.

4.4 Timer/Counter Unit

The Timer/Counter unit on the Intel386 EX processor has the same basic functionality as the industry-standard 82C54 counter/timer. It provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. This maximum frequency must be considered when programming the input clocks for the counters. Six programmable timer modes allow the timers to be used as event counters, as elapsed-time indicators, as programmable one-shots, as well as in many other applications. All modes are software programmable.

4.5 Watchdog Timer Unit

The Watchdog Timer (WDT) unit consists of a 32-bit down-counter that decrements every PH1P cycle, allowing up to 4.3 billion count intervals. The WDTOUT pin is driven high for sixteen CLK2 cycles when the down-counter reaches zero (the WDT times out). The WDTOUT signal can be used to reset the chip, to request an interrupt, or to indicate to the user that a ready-hang situation has occurred. The down-counter can also be updated with a user-defined 32-bit reload value under certain conditions. Alternatively, the WDT unit can be used as a bus monitor or as a general-purpose timer.

4.6 Asynchronous Serial I/O Unit

The Intel386 EX processor's asynchronous serial I/O (SIO) unit is a Universal Asynchronous Receiver/Transmitter (UART). Functionally, it is equivalent to the National Semiconductor NS16450 and INS8250. The Intel386 EX processor contains two asynchronous serial channels.

The SIO unit converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the CPU to serial data. The CPU can read the status of the serial port at any time during its operation. The status information includes the type and condition of the transfer operations being performed and any errors (parity, framing, overrun, or break interrupt).

Each asynchronous serial channel includes full modem control support (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#) and is completely programmable. The programmable options include character length (5, 6, 7, or 8 bits), stop bits (1, 1.5, or 2), and parity (even, odd, forced, or none). In addition, it contains a programmable baud rate generator capable of DC to 512 Kbaud.

4.7 Synchronous Serial I/O Unit

The Synchronous Serial I/O (SSIO) unit provides for simultaneous, bidirectional communications. It consists of a transmit channel, a receive channel, and a dedicated baud rate generator. The transmit and receive channels can be operated independently (with different clocks) to provide non-lockstep, full-duplex communications; either channel can originate the clocking signal (Master Mode) or receive an externally generated clocking signal (Slave Mode).

The SSIO provides numerous features for ease and flexibility of operation. With a maximum clock input of 12.5 MHz to the baud rate generator (assuming 25 Mhz device operation), the SSIO can deliver a baud rate of 6.25 Mbits per second. Each channel is double buffered. The two channels share the baud rate generator and a multiply-by-two transmit and receive clock. The SSIO supports 16-bit serial communications with independently enabled transmit and receive functions and gated interrupt outputs to the interrupt controller.

4.8 Parallel I/O Unit

The Intel386 EX processor has three 8-bit, general-purpose I/O ports. All port pins are bidirectional, with CMOS-level input and outputs. All pins have both a standard operating mode and a peripheral mode (a multiplexed function), and all have similar sets of control registers located in I/O address space. Ports 1 and 2 provide 8 mA of drive capability, while port 3 provides 16 mA.

5.0 DMA AND BUS ARBITER UNIT

The Intel386 EX processor’s DMA controller is a two-channel DMA; each channel operates independently. Within the operation of the individual channels, several different data transfer modes are available. These modes can be combined in various configurations to provide a very versatile DMA controller. Its feature set has enhancements beyond the 8237 DMA family; however, it can be configured such that it can be used in an 8237-like mode. Each channel can transfer data between any combination of memory and I/O with any combination (8 or 16 bits) of data path widths. An internal temporary register that can disassemble or assemble data to or from either an aligned or a nonaligned destination or source optimizes bus bandwidth.

The bus arbiter, a part of the DMA controller, works much like the priority resolving circuitry of a DMA. It receives service requests from the two DMA channels, the external bus master, and the DRAM Refresh controller. The bus arbiter requests bus ownership from the core and resolves priority issues among all active requests when bus mastership is granted.

Each DMA channel consists of three major components: the Requestor, the Target, and the Byte Count. These components are identified by the contents of programmable registers that define the memory or I/O device being serviced by the DMA. The Requestor is the device that requires and requests service from the DMA controller. Only the Requestor is considered capable of initializing or terminating a DMA process. The Target is the device with which the Requestor wishes to communicate. The DMA process considers the Target a slave that is incapable of controlling the process. The Byte Count dictates the amount of data that must be transferred.

5.1 Refresh Control Unit

The Refresh Control Unit (RCU) simplifies dynamic memory controller design with its integrated address and clock counters. Integrating the RCU into the processor allows an external DRAM controller to use chip-selects, wait state logic, and status lines.

The Intel386 EX processor’s RCU consists of four basic functions. First, it provides a programmable-interval timer that keeps track of time. Second, it provides the bus arbitra-

tion logic to gain control of the bus to run refresh cycles. Third, it contains the logic to generate row addresses to refresh DRAM rows individually. And fourth, it contains the logic to signal the start of a refresh cycle.

Additionally, it contains a 13-bit address counter that forms the refresh address, supporting DRAMs with up to 13 rows of memory cells (13 refresh address bits). This includes all practical DRAM sizes for the Intel386 EX processor's 64 Mbyte address space.

5.2 JTAG Boundary Scan Unit

The JTAG Boundary Scan Unit provides access to the device pins and to a number of other testable areas on the device. It is fully compliant with the IEEE 1149.1 standard and thus interfaces with five JTAG-dedicated pins: TRST#, TCK, TMS, TDI, and TDO. It contains the Test Access Port (TAP) finite-state machine, a 4-bit instruction register, a 32-bit identification register, a single-bit bypass register, and an 8-bit test mode register. The JTAG unit also contains the necessary logic to generate clock and control signals for the chains reside outside the JTAG unit itself: the SCANOUT and Boundary Scan chains.

6.0 MEMORY

Depending on the Intel386 EX processor's chip select configuration, memory accesses are directed to Flash, DRAM or the SEB. System memory is implemented using a single 4 Mbit Boot Block Flash Memory device and a single x32 SIMM socket which supports 1, 4 or 16 Mbyte of DRAM connected as two 16-bit banks with jumpers to select the options. The design supports 2 Mbyte and 8 Mbyte DRAM SIMMS, both of which are configured as a single 16-bit bank, and utilizes a single RAS signal. The chip selects are used as follows:

- GCS5# defines the DRAM linear space from address 0 to the DRAM size.
- UCS# defines the Flash space in the upper 512KB of the 64 Mbyte address range. (3F80000h-3FFFFFFh)
- GCS6# provide access to the lower half (up to 256KB) of the Flash in real memory just below 1 Mbyte. (00C0000h-00FFFFFh)
- Accesses above GCS5# and in the 640K to just below 1M range (00A0000h-00FFFFFh) where GCS6# is not generated are directed to the SEB (from 00A0000H to 00BFFFFh).

SEB memory accesses are in support of the PCMCIA and LCD/VGA controllers. The PCMCIA controller "windows" can be configured anywhere in real or extended memory and the VGA screen RAM can be configured to reside in DOS memory (normally 00A0000h-00BFFFFh) or as a linear frame buffer in the extended memory area above the DRAM.

6.1 Memory Chip Selects

Table 1 describes the chip select utilization It should be noted that the DRAM chip select overlaps the GCS6# and the SEB area in the lower 1 Mbyte of the memory map. The RadiSys R300EX controlling the DRAM inhibits DRAM accesses for 00A0000H-00FFFFFH and enables the SEB to be accessed in this region when GCS6# is not active. When GCS6# is active, it generates two wait state Flash accesses.

Table 1. Chip Select Utilization

Chip Select	Device	Address Range (HEX)	Wait States	Data Width	Memory Speed (ns)
GCS5#	1 Mbyte DRAM 2 Mbyte DRAM 4 Mbyte DRAM 8 Mbyte DRAM 16 Mbyte DRAM	0000000-00FFFFF 0000000-01FFFFF 0000000-03FFFFF 0000000-07FFFFF 0000000-0FFFFFF	0,1,2	16	70
UCS#	512 Kbyte FLASH	3F80000-3FFFFFF	2	16	80
GCS6#	128 Kbyte FLASH 256 Kbyte FLASH	00E0000-00FFFFF 00C0000-00FFFFF	2	16	80
none	SEB	00A0000-00DFFFF 00A0000-00BFFFF	8/15[1]	16/8[2]	-

NOTE:
1. Default cycles are 15 wait states for 8-bit and 8 wait states for 16-bit.
2. The CPLD forces 8 bit if external logic does not assert MEMCS16#.

6.2 Memory Map

Table 2. System Memory Map

	UCS#	3FFFFFF 3FE0000	Boot Block, Parm. Block
		3FDFFFF 3FC0000	avail.
		3FBFFFF 3FA0000	BIOS VGA BIOS
		3F9FFFF 3F90000	ROM DOS
		3F8FFFF 3F80000	avail.
		(see note)	SEB
		0FFFFFF	SEB
GCS5#		(max DRAM) 0100000	DRAM
	GCS6#	00FFFFF 00E0000	BIOS, VGA BIOS
	GCS6# (opt)	00DFFFF 00C0000	ROM DOS or SEB
	(fixed)	00BFFFF 00A0000	SEB
		009FFFF 0000000	DRAM

NOTE:

1. All memory accesses to areas above GCS5# (DRAM) and below UCS# are directed to the SEB. This provides access to the VGA and PCMCIA in extended memory when configured with 16 Mbytes of DRAM.

7.0 I/O DEVICES

The EXPLR1 design uses both internal and external I/O mapped peripherals. Some external devices require a chip select; others perform the address decode themselves.

7.1 I/O Map

Table 3 shows the system I/O map.

Table 3. System I/O Map

Chip Select	Device	Address Range (HEX)	Wait States	Data Width
internal	PIC 0	0020-0021	-	-
internal	Address Configuration Register	0022-0023	-	-
internal	Timers 0-2	0040-0043	-	-
GCS1#	Keyboard/Mouse Control	0060,0064	15d[1]	8
GCS2#	RTC & External CMOS	0070-0071	15d[1]	8
internal	Port 92	0092	-	-
internal	PIC 1	00A0-00A1	-	-
GCS4#	IDE CS0	01F0-01F7	8/15d[1]	8/16[2]
internal	COM2	02F8-02FF	-	-
GD6245	LCD/VGA CTRL	03B0-03DF, 46E8	-	8/16[2]
PD6710	PCMCIA Controller	03E0-03E1	15d[1]	8/16[2]
GCS3#	IDE CS1	03F6-03F7	15d[1]	8
internal	COM1	03F8-03FF	-	-
internal	Chip Configuration	F400-F85F	-	-
internal	Digital I/O	F860-F865	-	-
internal	Chip Configuration	F875-F8FF	-	-

NOTES:

1. Default cycles are 15 wait states for 8-bit and 8 wait states for 16-bit.
2. The CPLD forces 8 bit if external logic does not assert IOCS16#.

7.2 Intel386 EX Processor Internal I/O

The standard internal peripherals include the Interrupt Controllers, Interval Timers, SIOs, and Port 92. Each are briefly described in the following subsections. Refer to the *Intel386™ EX Embedded Microprocessor User's Manual* (272485) for full descriptions.

7.2.1 Interval Timers

The 8254 Timer/Counter's three channels are configured with a 1.190 MHz input clock derived from the 50 MHz input clock. The Timer 0 output is internally connected to IRQ0 to provide a standard 55 µs timer interrupt. The remaining two channels, Timer 1 and Timer 2, are available to specific applications and configured to generate IRQ10 and IRQ11, respectively.

NOTE:

Timer 1 is not needed as the refresh timer, since a dedicated unit in the Intel386 EX processor is available for this function.

7.2.2 Refresh Unit

The Refresh Unit is configured to perform a "refresh" bus cycle (memory data read with neither byte enable active) every 15.6 µs. The refresh base address is set so the DRAM chip select (CGS5#) is generated and the refresh row address is presented on A11-1 of the address bus. The RadiSys R300EX recognizes the refresh cycle and performs a CAS before RAS refresh cycle, which utilizes the DRAM's internal refresh counter.

7.2.3 Port 92

Port 92 controls the internal A20GATE signal and generates a CPU-only reset to the core. The RadiSys R300EX generates an NMI interrupt when a SHUTDOWN cycle is detected, allowing the BIOS NMI handler to issue a CPU-only reset.

7.2.4 Watch Dog Timer

The Watch Dog Timer can generate an IRQ15.

7.2.5 SIO 0 & 1

The serial ports are mapped to I/O addresses 3F8h-3FFh (COM1) and 2F8h-2FFh (COM2) are connected to IRQ4 and IRQ3, respectively. COM1 is a "three-wire" interface while COM2 is a full RS232 port. The ports are consistent with the PC's implementation. Table 4 shows the divider values and error percentage for some selected baud rates.

Table 4. Divider Values and Error Percentages

Desired Baud Rate	1.8432 MHz Clock	
	Divisor Value for 16x Clock	Percent Error
300	384	0
1200	96	0
2400	48	0
9600	12	0
19200	6	0
57600	2	0
115200	1	0

7.2.6 Digital I/O Port

Port1 on the Intel386 EX processor is used for Digital I/O. The Port1 signals along with the PWRGD, CLK2, IRQ5, IRQ12, INT2, and INT3 signals are routed to the DIO connector. Power is supplied on the connector by the +12, -12, and +5V pins. Using the DIO and external interrupts pre-empts using the keyboard and mouse interrupts.

7.3 External I/O

This design includes a set of interfaces to external peripherals. They include interfaces to LCD/VGA controller, an IDE hard disk, an RTC, a buffered PCMCIA slot, and Intel 82C42PE keyboard/mouse microcontroller.

7.3.1 LCD/VGA

The display section uses the Cirrus Logic, single chip, CL-GD6245 LCD/VGA Controller that includes a RAMDAC and a frequency synthesizer. This supports VGA and SVGA functionality with screen resolutions from 640x480 in 256 colors up to 1024x768 in 16. It also supports a variety of 640x480 LCDs, including: dual- and single-scan color or monochrome STN displays, 9-, 12-, and 18-bit color TFT, and multi-shade monochrome TFT displays. Three operation modes support VGA only, LCD only, and simultaneous VGA and LCD display. The design uses one 256K x 16 DRAM to provide a 512KB frame buffer.

The controller resides on the SEB and is configured in ISA mode. The memory and I/O space used by the VGA controller is a function of its configuration.

7.3.2 Keyboard/mouse

An Intel 82C42PE microcontroller provides a PS/2 style keyboard/mouse interface. Although it physically resides on the local address and data buses, it requires ISA-like I/O read and write strobes. GCS1# is configured for I/O space 60H and 64h and does not use the CPU’s wait state generation, therefore accesses are run as the default 8-bit, 15 wait state, SEB I/O cycles. The keyboard interrupt is connected to IRQ1 and the mouse interrupt to IRQ12.

7.3.3 RTC

A Dallas Semiconductor DS12887 provides the real-time clock and the battery backed RAM function normally used in a PC environment. RTC_AS and RTC_DS are generated by the RadiSys R300EX from GCS2#. The RTC resides on the local data buses and is accessed by SEB cycles to I/O 70-71h. The RTC interrupt is connected to IRQ8.

7.3.4 IDE

An IDE interface is implemented using 2 chip selects from the Intel386 EX processor. GCS3# is configured for I/O addresses 3F6-3F7h and used to for HST_CS1#, while GCS4#, I/O addresses 1F0-1F7h, is used for HST_CS0#. The RadiSys R300EX controls a data bus transceiver and uses (IOCS16#) to determine the access time and the Intel386 EX processor's bus sizing. These cycles are run at the SEB standard 8 or 15 wait states.

The IDE interrupt is tied to IRQ14.

7.3.5 PCMCIA Controller

A Cirrus Logic CL-PD6710 supports one buffered PCMCIA card slot. Its control registers are mapped to I/O locations 3E0-3E1h and performs its own decode.

Three of the interrupt outputs of the CL-PD6710 are available. IRQ5, 9 and 14 outputs are tied directly to the Intel386 EX processor's IRQ5, 9 and 14 inputs. IRQ14 is shared with the IDE interface and allows a PCMCIA ATA disk to be used instead of the IDE disk interface.

8.0 Hardware Interrupts

The interrupt mapping is close to that of a PC. Table 5 shows this mapping and where it deviates from a standard PC implementation.

Table 5. Interrupt Mapping

PC INT #	IRQx	Vector (hex)	Name	PC Use
2	NMI	8	Shutdown	Parity Error/IOCHK
8	IRQ0	20	Timer 0	same
9	IRQ1	24	Keyboard	same
A	IRQ2	28	cascade vector	same
B	IRQ3	2C	COM2	same
C	IRQ4	30	COM1	same
D	IRQ5	34	PD6710, IRQ5, DIO-IRQ5	LPT2
E	IRQ6	38	DIO-INT2	FDC
F	IRQ7	3C	DIO-INT3	same
70	IRQ8	1C0	RTC	same
71	IRQ9	1C4	PD6710, IRQ9	VGA
72	IRQ10	1C8	Timer 1	ISA
73	IRQ11	1CC	Timer 2	ISA
74	IRQ12	1D0	Mouse, PD6710	Mouse
75	IRQ13	1D4	N/A	NPX
76	IRQ14	1D8	IDE or PD6710, IRQ14	HDC
77	IRQ15	1DC	WDT	ISA

9.0 RadiSys R300EX Overview

A RadiSys R300EX provides the support required by the Intel386 EX processor and the peripheral devices. RadiSys R300EX is a modular design and provides a set of functions that are likely to be required in many common Intel386 EX processor designs.

9.1 Reset Synchronization

The RESET signal that goes to the CPU is synchronized with CLK2 to allow the internal state machines to be in sync with the CPU.

9.2 Ready Generation

This logic returns RDY# to terminate any bus cycle that is not claimed by the Intel386 EX processor (LBA# is inactive). This includes “Halt/Shutdown” cycles, SEB, DRAM and Flash (below 1 Mbyte) accesses.

- Halt/shutdown and 16-bit SEB cycles are 8 wait states.
- 8-bit SEB cycles are 15 wait states
- SEB accesses can be extended with the IOCHRDY signal.
- DRAM access vary from 0 to 2 wait states depending on the access type (page hit, miss,...).
- Flash accesses are 2 wait states.

The generation of RDY# for all unclaimed accesses allows a simple interface to most ISA peripherals and eliminates the “hang” condition possible when software “polls” various addresses to determine the existence of a resource.

The RadiSys R300EX drives RDY# any time LBA# is inactive. The RDY# signal is forced high for the cycle immediately after it is sampled low by the CPU. The only time that RDY# is tri-stated is when the LBA# signal is active.

9.3 Data Bus Transceiver Control

A disable signal for a data bus transceiver between the CPU and peripheral devices is generated to eliminate the possibility of a conflict on the data bus when the CPU transitions from a read to a write cycle. The transceiver also provides TTL to CMOS level translation for the Intel386 EX processor. The transceiver is disabled for all T1, T1P and Ti cycles that follow a T2 or T2P cycle.

9.4 NMI Setting/Clearing

NMI is generated when a CPU “Shutdown” cycle is detected. The BIOS uses this to issue a CPU-only reset via Port 92. The RadiSys R300EX includes the logic to reset the NMI by detecting an access to the Reset Vector (UCS#).

9.5 DRAM Control

The DRAM controller was designed to support page-mode non-interleaved access to the main memory. It provides access times from 0 to 2 wait states depending on the address sequence from the CPU. The DRAM interface was designed to support 256Kx32,1Mx32 or 4Mx32 symmetric SIMM (equal number of rows and columns) configured as 2 banks, 16-bits wide (2 RAS, 4 CAS and 1 WE input). It also supports 512Kx32, and 2Mx32 symmetric SIMMs configured as a single bank, 16 bits wide (1 RAS, 4 CAS, and 1 WE input).

The DRAM controller in the RadiSys R300EX includes the address multiplexors, thereby further reducing the number of components required for a design. It also includes the CAS before RAS refresh generation circuitry.

9.6 Flash/EPROM Control

The interface to the Flash memory is made up of three signals: FLSHA18, FLSHCS#, and FLSHWE#. The FLASHA18 signal is used as the most significant address bit of the Flash memory device, in place of A18 directly from the CPU. When UCS# is asserted (i.e. at the top of the full address space), FLSHA18 is the normal version of A18. When GCS6# is asserted (i.e. at the top of the 1M address space), FLSHA18 is the inverted version of A18. This enables the same physical Flash memory device to easily be mapped into two locations in the address map. In this way, the boot code can show up at the top of the physical address space, while the BIOS can be found at the top of the 1M address space as expected, and still only require one physical device.

FLASHCS# is generated any cycle where either UCS# or GCS6# is detected and FLSHWE# is generated for write cycles where either UCS# or GCS6# is active. All write access to flash must be word-wide on even byte boundaries. The Vpp programming voltage for the flash is controlled by a jumper.

9.7 SEB Interface

The RadiSys R300EX generates BALE, MEMR#, MEMW#, IOR#, IOW# and responds to MEMSC16#, IOCS16# and IOCHRDY as required by the external peripheral devices.

9.8 Theory of Operation

This discussion is limited to the description of the RadiSys R300EX and its interface to the other components. For detailed descriptions of the other individual devices, please refer to the appropriate vendor's documentation.

9.9 RadiSys R300EX Pin Definition

Table 6 shows the pin definitions.

Table 6. RadiSys R300EX Pin Definitions (Sheet 1 of 2)

Pin	RadiSys R300EX Inputs
CLK2	2x input clock, same as input to the Intel386 EX processor
ADS#	Address Status
W/R#	Write/Read
M/IO#	Memory/IO
D/C#	Data/command
BHE#	High byte enable
BLE#	Low byte enable
A[23:1]	CPU address bus used for DRAM address and misc. decodes
UCS#	Upper chip select (Flash at the top of the address space)
GCS6#	General chip select 6 (Flash below 1 Mbyte)
GCS5#	General chip select 5 (DRAM 1, 2, 4, 8, or 16 Mbyte)
GCS4#	General chip select 4 (IDE)
GCS3#	General chip select 5 (IDE)
GCS2#	General chip select 2 (Keyboard/mouse control) 60-61h and 64-65h
GCS1#	General chip select 1 (RTC)
LBA#	Intel386 EX processor Local Bus Access
PWRGD	Power good used to generate a RESET
SEB Inputs	
IOCHRDY	Used to extend SEB cycles
IOCS16#	Indicates a 16 bit SEB I/O device is being accessed
MEMCS16#	Indicates a 16 bit SEB memory device is being accessed
Outputs to the CPU	
RESET	RESET - Synchronized with CLK2, used to phase the state machines
RDY#	READY I/O
NA#	Next Address - Used to request pipelining for all DRAM accesses
BS8#	Bus Size Eight - Used to indicate an external 8-bit device is being accessed
NMI	Non Maskable Interrupt - Generated for CPU shutdown cycles
Outputs to DRAM	
MA[0:10]	Multiplexed DRAM address
RAS#	Row Address Strobe to the DRAM
CASAH#	Column Address Strobe to the DRAM bank A, high byte
CASAL#	Column Address Strobe to the DRAM bank A, low byte
CASBH#	Column Address Strobe to the DRAM bank B, high byte
CASBL#	Column Address Strobe to the DRAM bank B, low byte

Table 6. RadiSys R300EX Pin Definitions (Sheet 2 of 2)

Pin	RadiSys R300EX Inputs
WE#	Write enable to both DRAM banks
ONE_4MEG	Memory size selection jumper input
Outputs to Flash	
FLSHCS#	Flash chip enable
FLSHWE#	Flash write enable
FLSHA18	Most significant address bit to the Flash
SEB and Miscellaneous Outputs	
IOR#	SEB I/O read strobe
IOW#	SEB I/O write strobe
MEMR#	SEB memory read strobe
MEMW#	SEB memory write strobe
BALE	Address latch signal
RTC_AS	Address strobe to the RTC (IOW to 70h)
RTC_DS	Data strobe to the RTC (IOR or IOW to 71h)
IDE_ENH#	Enable to the IDE high byte data transceiver
IDE_ENL#	Enable to the IDE low byte data transceiver
KBD_CS#	Keyboard control CS#
DATA_DE	Disable for data bus transceivers

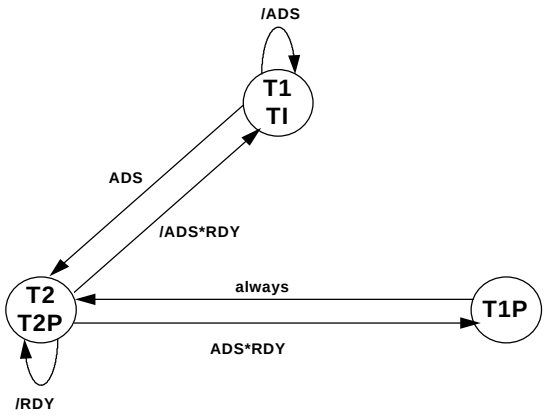
9.10 State Machines

Three state machines make up the core of the CPLD:

- The **Bus Tracker** uses ADS# and RDY# to follow the Intel386 EX processor bus through its various T-states.
- The **SEB** state machine generates various cycles to the external peripherals.
- The **DRAM** state machine keeps track of DRAM access states and generates the DRAM control signals and RDY# for DRAM accesses.

9.11 Bus Tracker Description

Figure 3 shows the bus tracker. All transitions of the state machine are synchronized with the CPU's internal 1x clock. This state machine starts the SEB state machine, generates the Flash chip select, and detects CPU "shutdown" cycles, in order to generate an NMI.



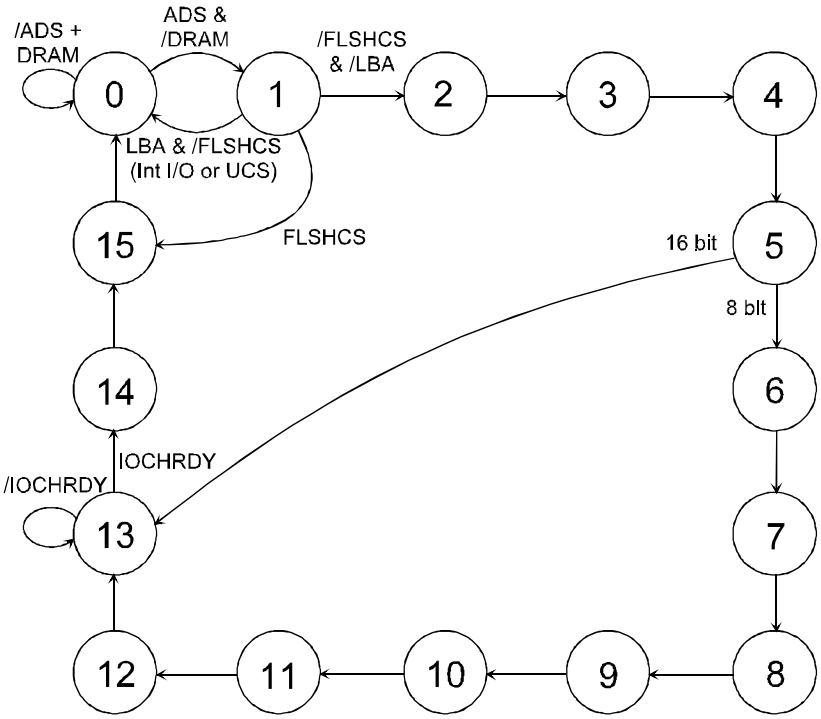
NOTE:

1. The system resets to the T1Ti state waiting for the first access indicated by assertion of ADS.
2. It remains in this state until RDY is asserted.
3. It transitions to T1 if ADS is inactive (non-pipeline) or to T1P is ADS is active (pipeline).

Figure 3. Bus Tracker

9.12 SEB Description

Figure 4 shows the SEB state machine.



NOTE:

1. FLSHCS = GCS6# + UCS#
2. A transition from state #0 to state #1 occurs at the end of any T1 or T1P that is not directed to DRAM.
3. LBA# is checked at the end of state #1 to identify internal Intel386 EX processor I/O accesses and non-flash accesses (the CPU generates the RDY) and returns the state machine to state #0 to await the next bus cycle. Accesses to Flash with GCS6# or UCS# sends the state machine to state #15 providing 2 Wait States. All other cycles are directed to the SEB.
4. BALE is asserted at the beginning of state #1 and will be deasserted at the end of state #1 if the next state is either state #0 or state #15. If the next state is state #2, then BALE will be deasserted in the middle of that state.
5. In state #5, IOSC16# or MEMCS16# is sampled to determine whether the access is to an 8 or 16 bit device to adjust the wait states.
6. At state #13, the clock synchronized version of IOCHRDY is sampled to allow the accessed device to extend the cycle.
7. RDY# is set active at the end of state #15 for one T-state. RDY# changes state 1/4 T-State, or one CLK2 phase, into the T-State, rather than at the beginning or middle of the T-State.

Figure 4. SEB State Machine

The dynamic bus sizing capability of the Intel386 EX processor, via the BS8# signal, provides the 16 bit to 8 bit conversion cycles when an 8 bit device is accessed with a "word" bus cycle.

BALE is set active at the beginning of state #1 and is de-asserted at the end of state #1 (LBA# active) or in the middle of state #2 (LBA# inactive). The appropriate SEB command strobe (MEMR#, MEMW#, IOR# or IOW#) is set active at the beginning of state #3. The read strobes are held active until the end of state #0 while the write strobes are de-asserted at the end of state #15 to insure the required data and address hold time. Ready is asserted at the transition from state #15 to state #0, and is deasserted one T-state (two CLK2's) later.

The SEB design implements a functional subset of the ISA bus. SMEMR# and SMEMW# strobes are not generated, nor is 0WS# used to shorten accesses. See the SEB timing analysis section below for other variants.

9.13 DRAM Controller Description

The page-mode DRAM controller makes use of the Intel386 EX processor's address pipelining to support zero wait state read and one wait state write cycles. The address used for bank selection is determined by the ONE_4MEG jumper input. For 1 or 4 Mbyte, A19 determines which DRAM bank is selected. For 2, 8, or 16 Mbyte, A23 selects the bank.

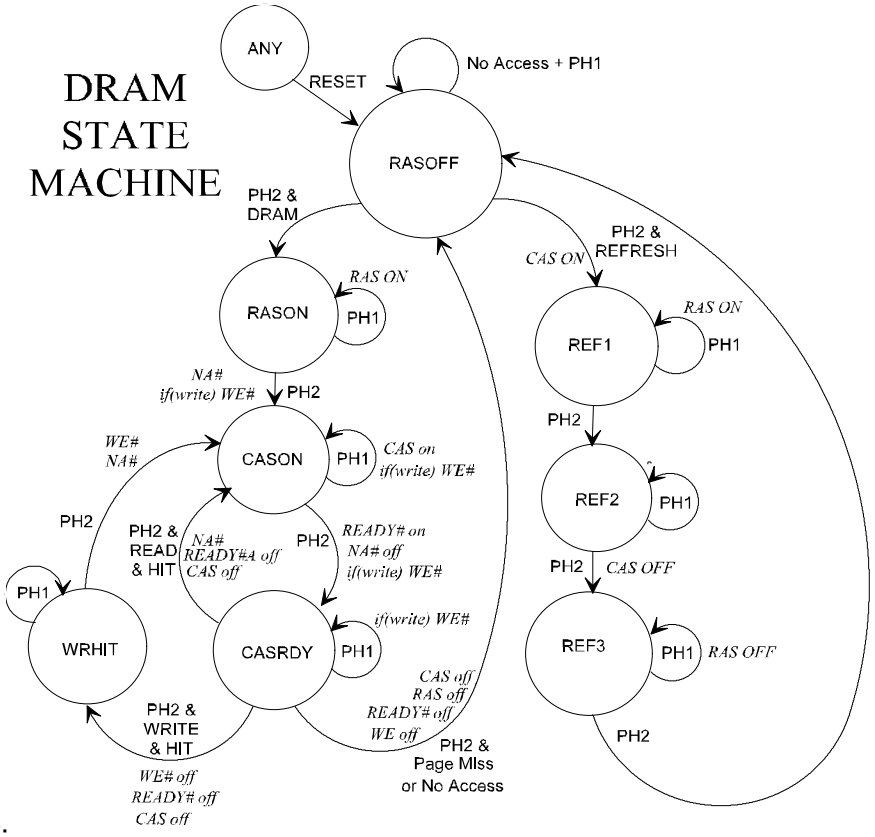
The page hit register saves the CPU address bits A[23:10]] whenever RAS is asserted. At the beginning of any DRAM access, (in T1 or T2P), a page hit is determined by comparing the new CPU address with the values stored in the page hit register. If the upper address bits match those stored in the register, and at least one byte enable is active, then a page hit is recognized.

The RadiSys R300EX generates four types of DRAM cycles with varying performance depending on the address sequences and whether the cycle is pipelined or not. These relationships are shown in Table 7.

Table 7. DRAM Performance

Cycle Type	WS Non-pipeline	WS Pipeline	Comments
RAS# already off	2	-	RAS off after refresh or non DRAM access
Page miss	-	2	RAS# precharge required
Read page hit	-	0	CASxx# only access
Write page hit	-	1	CASxx# only access. Wait state required to guarantee write access time.
Refresh	3	N/A	Refresh both banks

Figure 5 details the DRAM controller state machine.



NOTE:

1. Signals in *italics* with “on” and “off” indicate when the named output signal is asserted or de-asserted. The signal stays in its current state unless explicitly changed as noted by “on” or “off”.
2. BHE# and BLE# signals are tested to determine if a DRAM cycle is a refresh cycle, or a read/write cycle.

Figure 5. DRAM Controller State Machine

All DRAM control signals are generated by this state machine and the current cycle type.

RAS# is asserted in the middle of state RASON for a regular cycle, or the middle of REF1 for a refresh cycle. It is deasserted at the end of state CASRDY when transitioning back to state RASOFF, or in the middle of REF3.

Four CAS signals are generated, one for each byte of each bank. The appropriate CAS (CASAH#, CASAL#, CASBH#, CASBL#) signals are asserted in the middle of state CASON. The CASxx# signal is deasserted upon exiting state CASRDY, or state REF2.

To support pipelining of the Intel386 EX processor, the NA# signal is generated for all accesses that are directed to DRAM. This signal is generated from GCS5# and address lines A23-17. Table 8 shows the row/column multiplexing scheme.

Table 8. Row/Column Multiplexing Scheme

	ONE_4MEG = High (for 1 Mbyte or 4 Mbyte)		ONE_4MEG = Low (for 2Mbyte, 4 Mbyte, or 16 M byte)	
	Row	Column	Row	Column
MA10	A22	A21	A22	A21
MA9	A21	A20	A20	A19
MA8	A18	A9	A18	A9
MA7	A17	A8	A17	A8
MA6	A16	A7	A16	A7
MA5	A15	A6	A15	A6
MA4	A14	A5	A14	A5
MA3	A13	A4	A13	A4
MA2	A12	A3	A12	A3
MA1	A11	A2	A11	A2
MA0	A10	A1	A10	A1

Note that 1 Mbyte, 4 Mbyte and 16 Mbyte DRAM SIMMs are organized as 2 banks, 16 bits wide, while 2 Mbyte and 8 Mbyte DRAM SIMMs often have only one 16-bit wide bank. For 1 Mbyte or 4 Mbyte configurations, the ONE_4MEG signal must be high so that A19 can select the bank (CASAx or, CASBx). For 2 Mbyte, 8 Mbyte or 16 Mbyte configurations, the ONE_4MEG signal must be low so that A23 can select the bank.

9.14 Flash/EPROM Control

UCS# or GCS6# forms FLASHCS# which is generated from the beginning of the first T2 until the end of the last T2 cycle. FLSHWE# is generated for flash write cycles and extends from the middle of the first T2 to the middle of the last T2. This is to provide adequate setup and hold times for writes to the Flash device.

9.15 System BIOS

The System BIOS is similar to a standard PC BIOS with support for the RTC, PS/2 style mouse/keyboard and the integrated VGA controller. Additional support is required as follows:

- Configuring the Intel386 EX processor, GD6245 and the PD6710
- NMI handling to perform a CPU-only reset in case of a Shutdown
- Flash ROM utilities (jumper on the keyboard controller P14 pin selects normal boot or flash utility)

9.16 Intel386 EX Processor Configuration

Table 9 shows the values of the Intel386 EX processor-specific configuration registers.

Table 9. Intel386 EX Processor Configuration Register Values (Sheet 1 of 3)

Address (hex)	Register	High Byte (hex)	Low Byte (hex)	Description
0022	I/O Remap	-	04	SIO0-1 & DMA into Expanded I/O
F400	CS0 Low Address	00	00	disabled
F402	CS0 High Address	00	00	
F404	CS0 Low Mask	00	00	
F406	CS0 High Mask	00	00	
F408	CS1 Low Address	80	80	60-61, 64-5, I/O8
F40A	CS1 High Address	00	01	
F40C	CS1 Low Mask	14	01	
F40E	CS1 High Mask	00	00	
F410	CS2 Low Address	C0	80	0070-0071,I/O8
F412	CS2 High Address	00	01	
F414	CS2 Low Mask	04	01	
F416	CS2 High Mask	00	00	
F418	CS3 Low Address	D8	80	03F6-03F7,I/O
F41A	CS3 High Address	00	0F	
F41C	CS3 Low Mask	00	01	
F41E	CS3 High Mask	00	00	
F420	CS4 Low Address	C2	80	01F0-01F7,I/O
F422	CS4 High Address	00	07	
F424	CS4 Low Mask	1C	01	
F426	CS4 High Mask	00	00	
F428	CS5 Low Address	03	80	0000000-0XFFFFF,MEM
F42A	CS5 High Address	00	00	
F42C	CS5 Low Mask	F8	01	
F42E	CS5 High Mask	00	0F	
F430	CS6 Low Address	03	02	00E0000-00FFFFF,MEM,2WS
F432	CS6 High Address	00	0E	
F434	CS6 Low Mask	FC	01	
F436	CS6 High Mask	00	01	
F438	UCS Low Address	03	02	3FE0000-3FFFFFF,MEM,2WS
F43A	UCS High Address	03	F8	
F43C	UCS Low Mask	F8	01	

Table 9. Intel386 EX Processor Configuration Register Values (Sheet 2 of 3)

Address (hex)	Register	High Byte (hex)	Low Byte (hex)	Description
F43E	UCS High Mask	00	07	
F480	SSIO T. Buffer	00	00	disabled
F482	SSIO R. Buffer	00	00	
F484	SSIO Baud	-	00	
F486	SSIO CON1	-	C0	
F488	SSIO CON2	-	00	
F48A	SSIO CTRL	-	00	
F4A0	REF Base Address	00	00	Base Address = 0
F4A2	REF CIR	01	86	~15.6 µs @ 25 MHz
F4A4	REF Control	80	00	enabled
F4A6	REF Address	0F	FF	A11-1
F4C0	WDT Reload High	01	00	~670mS @ 25MHz
F4C2	WDT Reload Low	00	00	"
F4C4	WDT Counter High	read only	read only	
F4C6	WDT Counter High	read only	read only	
F4C8	WDT Clr	read only	read only	LOCKOUT Seq. Reg.
F4CA	WDT Status	-	read only	
F4F8	SIO 0	-	-	remapped to COM1 (3F8-F)
F4FA	SIO 0	-	-	"
F4FC	SIO 0	-	-	"
F4FE	SIO 0	-	-	"
F800	CLK Control	-	00	nu
F802	PSCLK Scaler	00	13	1.190MHz @ 25MHz
F820	Pin Configuration 0	-	00	Port 1x is LPT Data
F822	Pin Configuration 1	-	7E	Port 2[7],Txd,Rxd & GCS4-1,2[0]
F824	Pin Cfg 2	-	0C	Port 3[7-4],INT1-0,3[1-0]
F826	Pin Cfg 3	-	1F	GCS6,NPX,GCS5 & SIO1
F830	DMA Cfg	-	88	DMA's disabled

Table 9. Intel386 EX Processor Configuration Register Values (Sheet 3 of 3)

Address (hex)	Register	High Byte (hex)	Low Byte (hex)	Description
F832	INT Cfg	-	0F	CAS disabled,INT7-4
F834	TMR Cfg	-	00	PSCLKs
F836	SIO Cfg	-	47	COM1(2pin),SERCLK=12.5 MHz
F860	P1 Pin	-	read only	
F862	P1 LTC	-	XX	LPT data out
F864	P1 Dir	-	00	P1[7-0] = out
F866	nu	-	-	
F868	P2 Pin	-	read only	
F86A	P2 LTC	-	00	LPTa, INIT#=0
F86C	P2 Dir	-	7F	P2[7] = out
F86E	nu	-	-	
F870	P3 Pin	-	read only	
F872	P3 LTC	-	03	LPTb,ADFX#,STB#=1
F874	P3 Dir	-	FC	P3[7-4]=in, [1-0]=out
F8F8	SIO 1	-	-	remapped to COM2 (2F8-F)
F8FA	SIO 1	-	-	"
F8FC	SIO 1	-	-	"
F8FE	SIO 1	-	-	"

9.17 NMI Handler

The BIOS should generate a CPU-only reset via Port 92 when an NMI interrupt is detected. This enables user-generated shutdown cycles to cause a reset (PC compatibility).

9.18 Flash Support

The flash memory's boot block section contains code which enables:

- Downloading to a host PC — all parameter or main block contents
- Uploading from a host PC — a binary image which can be programmed into the flash

The flash boot block area should contain code which initializes the board then checks the jumper on P14 of the 82C42PE:

- When P14 jumper is present (bit = 0), the code should vector to a flash programming utility
- When P14 jumper is not present, the code performs normal PC-style POST and boot routines

The flash programming utility should provide the capability to attach the POS Terminal's two COM ports to the two COM ports of a host PC which is running a companion application.

- One COM port handles ASCII terminal-like communication to the host PC's screen and keyboard
- One COM port provides the data path to upload/download to flash

10.0 VGA BIOS

The VGA controller uses the standard VGA BIOS and drivers provided by Cirrus Logic.

11.0 CONNECTORS/JUMPERS

Table 10 shows the connectors/jumpers.

Table 10. Connectors/Jumpers (Sheet 1 of 2)

Jumper / Connector	Function
JP2	COM2 - full RS232
JP3	COM1 - 3 wire (Rxd,Txd, Gnd)
JP4	PCMCIA speaker out
JP5 1-2 2-3	Boot Block Programming Enable programming Disable programming
JP6 off on	DRAM Size 1, 4 Mbytes 2, 8, 16 Mbytes
JP7	Panel Select
JP8	Speaker
JP9	POST loop test
JP10	BIOS Boot Options
JP11	IDE Connector
J2	PCMCIA Connector
J3	PS/2 Mouse

Table 10. Connectors/Jumpers (Sheet 2 of 2)

Jumper / Connector	Function
J4	VGA Connector
J5	PS/2 Keyboard
H1	DIO Connector
H2	SEB Connector
CN1	Flat Panel Connector

12.0 Schematics and PLD Equations

The EXPLR1 kit includes schematics and PLD equations in hardcopy and on diskette. Schematics are in OrCAD* format. Refer to the *EXPLR1 Embedded PC Evaluation Platform Board Manual*, in the Related Information section for additional product information availability.

13.0 Summary

The EXPLR1 has been built, debugged, and tested as a working design. This application note and the *EXPLR1 Embedded PC Evaluation Platform Board Manual* describes the design's hardware and software implementation details. This document addresses memory control, and contains several DRAM controller state machines. The DOS-compatible EXPLR1 design, when used with a PC and off-the-shelf tools, provides users with an affordable, quick and easy-to-use platform for developing application software.

The Intel386 EX processor is a highly integrated embedded CPU which incorporates key peripheral components to form a cost effective, compact system for embedded PC applications. This document describes other key technologies, including the Intel Boot Block Flash Memory, RadiSys R300EX Memory/Bus Controller, PCMCIA slot, and power management. POS terminal and other embedded PC architectures and markets are well served by embedded Intel Architecture processors which provide low-cost development environments, fast time to market, proven support infrastructure, and long lifecycles.

14.0 RELATED INFORMATION

For Intel Customer Support in US and Canada, call 800-628-8686. Documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect IL 60056-7641
1-800-879-4683

Table 11. Related Intel Documentation

Document Title	Order #
Intel386™ EX Embedded Microprocessor User's Manual	272485
Intel386™ EX Embedded Microprocessor datasheet	272420
Intel386™ SX Microprocessor Programmer's Reference Manual	240331
Intel386™ SX Microprocessor Hardware Reference Manual	240332
Intel *Development Tools* handbook	272520
EXPLR1 Embedded PC Evaluation Platform Board Manual	272775