TECHNICAL PAPER

Interfacing the Byte-Wide SmartVoltage FlashFile™ Memory Family to the Intel960® Microprocessor Family

October 1996

Order Number: 297804-001

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FIGURES

TABLES

REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

This technical paper describes the designs for interfacing Intel's byte-wide SmartVoltage FlashFile™ memory family to different processors in the Intel960® processor family. The techniques discussed in the following sections focus on interfacing the 28F008SC to the i960 processor family; however, these can be applied to other members of the byte-wide SmartVoltage FlashFile memory family as well. For the designs described below, any control logic as well as processor bus cycles have been simulated, but they have **not** been lab tested.

The 4-, 8-, and 16-Mbit byte-wide SmartVoltage FlashFile memories provide high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. For secure code storage applications where code is either directly executed out of flash or downloaded to RAM, these memories offer three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. Code and data storage applications are facilitated well by their enhanced suspend capabilities. The SmartVoltage technology allows a choice in V_{CC} and V_{PP} combinations to meet system performance and power expectations. Furthermore, their power management aids in power-sensitive applications.

The read and write operations of the these devices are controlled by three distinct signals—CE#, OE#, and WE#. The power-down and reset operations are controlled by one signal—RP#. These pins are described in Table 1.

Please refer to the Intel World Wide Web site, BBS, or your Intel or local distribution sales office to obtain the schematics, timing analysis files, and logic files for the interfaces documented in this paper.

The timing specifications used in these designs were taken from the datasheets listed in Appendix A. The Appendix contains the names and order numbers of the datasheets used. The byte-wide FlashFile memory datasheets used were revision -001. The revision numbers for the microprocessor datasheets used are as follows: *80960JA/JF Embedded 32-Bit Microprocessor Datasheet* (revision -004), *80L960JA/JF 3.3V Embedded 32-Bit Microprocessor Datasheet* (revision -002), *80960RP Intelligent I/O Microprocessor Datasheet* (revision -001), *80960HA/HD/HT 32-Bit High-Performance Superscalar Processor Datasheet* (revision -004).

Please contact your Intel or local distribution sales office for up-to-date specifications before finalizing any design.

2.0 i960® MICROPROCESSOR FAMILY INTERFACE

2.1 i960® JF Microprocessor Interface at 33 MHz

The i960® JF processor is a 32-bit RISC embedded processor with a 32-bit multiplexed address/data bus.

Table 1. Byte-Wide SmartVoltage FlashFile™ Memory Pin Descriptions

Sym	Type	Name and Function
CE#	I	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
OE#	I	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	I	**WRITE ENABLE:** Controls writes to the Command User Interface (CUI) and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	I	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode.

Table 2. i960® JF Processor Pin Descriptions

Sym	Type	Name and Function
AD31:0	I/O	**ADDRESS/DATA BUS:** Multiplexed address and data bus.
ALE	O	**ADDRESS LATCH ENABLE:** Indicates the transfer of a physical address.
ADS#	O	**ADDRESS STROBE:** Indicates a valid address and the start of a new bus access.
BE3:0#	O	**BYTE ENABLES:** Selects which of up to four data bytes on the bus participates in the current bus access.
W/R#	O	**WRITE/READ:** Specifies whether the operation is a write(1) or a read(0).
RDYRCV#	I	**READY/RECOVER:** Indicates that data on AD lines can be sampled or removed; controls the insertion of wait-states.
CLKIN	I	**CLOCK INPUT:** Provides the processor's fundamental time base.

2.1.1 PROCESSOR INTERFACE SIGNALS

System logic uses the signals described in Table 2 in interfacing the 28F008SC to the i960 JF processor.

2.1.2 INTERFACE CONSIDERATIONS

The following discussion considers the interfacing of a 5V V_{CC} i960 JF processor operating at 33 MHz to 28F008SC-85s.

This design (shown in Figure 1) uses four 28F008SC-85s to match the 32-bit data bus of the i960 JF processor, providing 4 Mbytes of flash memory. Four octal latches, enabled by the ALE signal, de-multiplex the address from the AD bus. The latched address bits AD_{21}–AD_2 select locations within the 28F008SC-85s' memory space.

CLK Option

A 33 MHz clock signal drives the i960 JF processor CLKIN input and the PLD.

Reset

An active-low reset signal, RESET#, drives the RESET# inputs of the i960 JF processor and PLD as well as the RP# input of the 28F008SC-85s.

Control Signal Generation

Combinational logic using the upper ten bits of the latched address and the byte enable pins generates the CE# control signals for the 28F008SC-85s as well as the CS# input for the state machine. The upper ten bits are used to determine if the bus cycle is directed to the flash's memory space. This logic is a ten-input OR gate, and the address range depicted in the schematic is 00000000h–003FFFFFh. If the memory range desired for the flash memory is 80000000h–803FFFFFh, the AD_{31} input to the OR gate is inverted. The processor's ADS# and W/R# also serve as inputs to the state machine. The state machine generates the OE# and WE# signals for the 28F008SC-85s. The state machine also generates the RDYRCV# signal to the i960 JF processor to control wait-state generation. When powered-up, the state machine will transition to state S0 within one clock cycle since the address decode logic will be driving the CS# signal high, and the state machine equations are written in such a way that if this signal is sampled high in the middle of a read or write cycle, the state machine immediately returns to state S0.

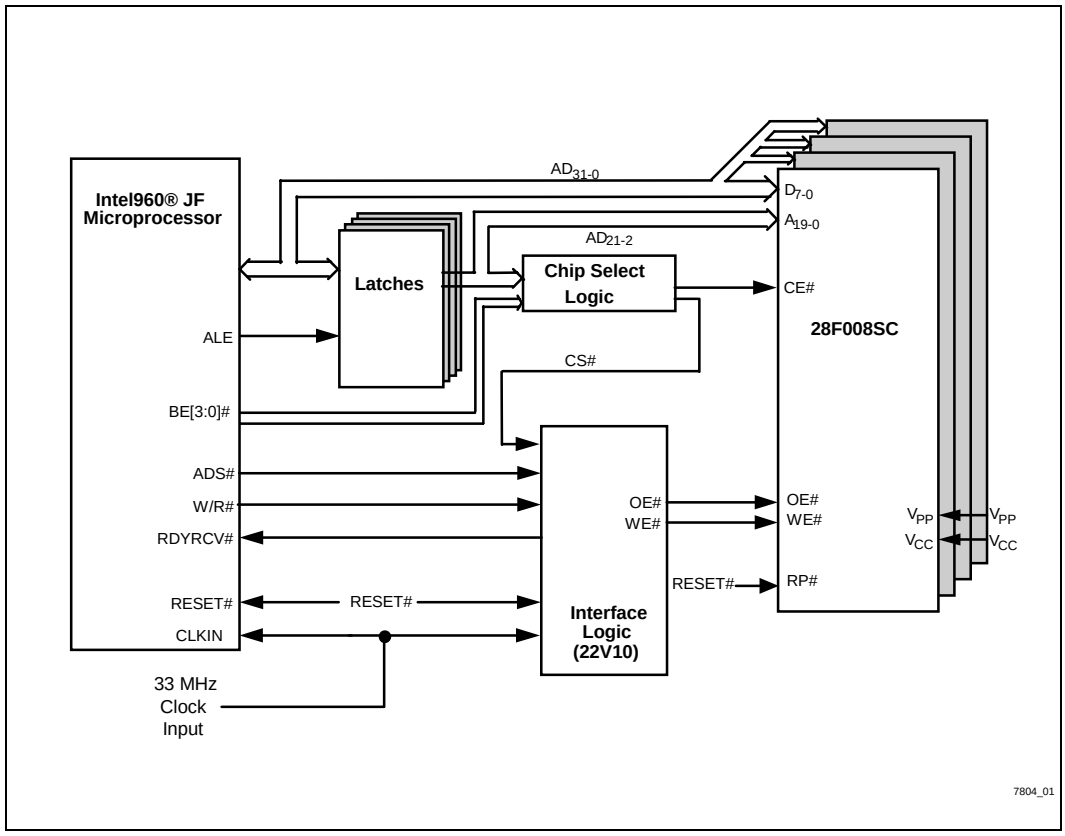

Figure 1. 28F008SC Interface to the i960® JF Processor

2.1.3 READ CYCLE DESCRIPTION

Refer to the state diagram (Figure 2) and read cycle timing diagram (Figure 3) for the following discussion of the read cycle.

When the i960 JF processor initiates a read cycle by asserting ADS#, the state machine enters an anticipation state. At the end of cycle T2, if CS# is asserted with W/R# = "0," the state machine asserts OE# to enable the 28F008SC-85 data output buffers. The OE# signal remains asserted and the RDYRCV# signal is asserted after the T3 cycle to inform the i960 JF processor that valid data is on the bus. At the end of the T4 cycle, the processor reads the data presented, and the state machine deasserts both OE# and RDYRCV#. The state machine then returns to its idle state to wait for the next bus cycle.

2.1.4 WRITE CYCLE DESCRIPTION

Refer to the state diagram (Figure 2) and write cycle timing diagram (Figure 4) for the following discussion of the write cycle.

When the i960 JF processor initiates a write cycle by asserting ADS#, the state machine enters an anticipation state. After cycle T2, if CS# is asserted with W/R# = "1," the state machine asserts WE#. The WE# signal remains asserted and the RDYRCV# signal is asserted at the end of the T3 cycle to inform the i960 JF processor that the flash is ready to accept the data. After cycle T4, the 28F008SC-85s latch the address and data to write when the state machine deasserts WE#. RDYRCV# is also deasserted as the state machine returns to its idle state to wait for the next bus cycle.

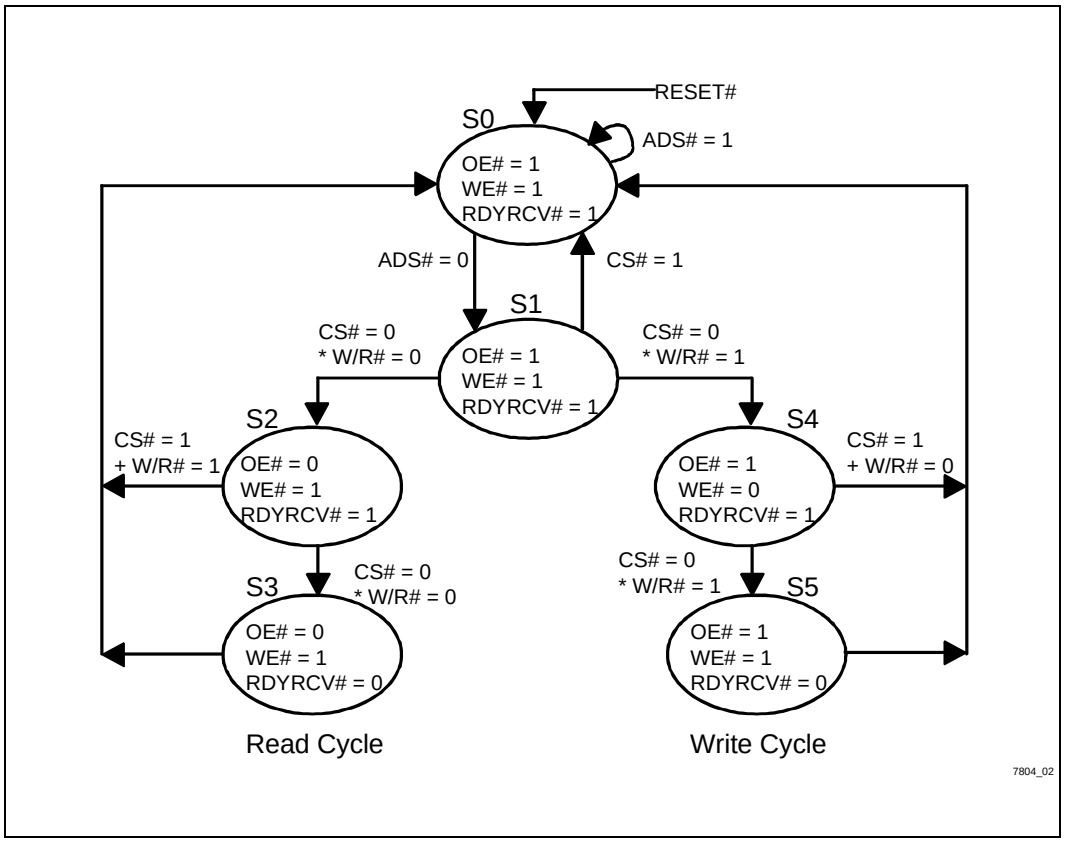

Figure 2. State Diagram for i960® JF CPU Interface

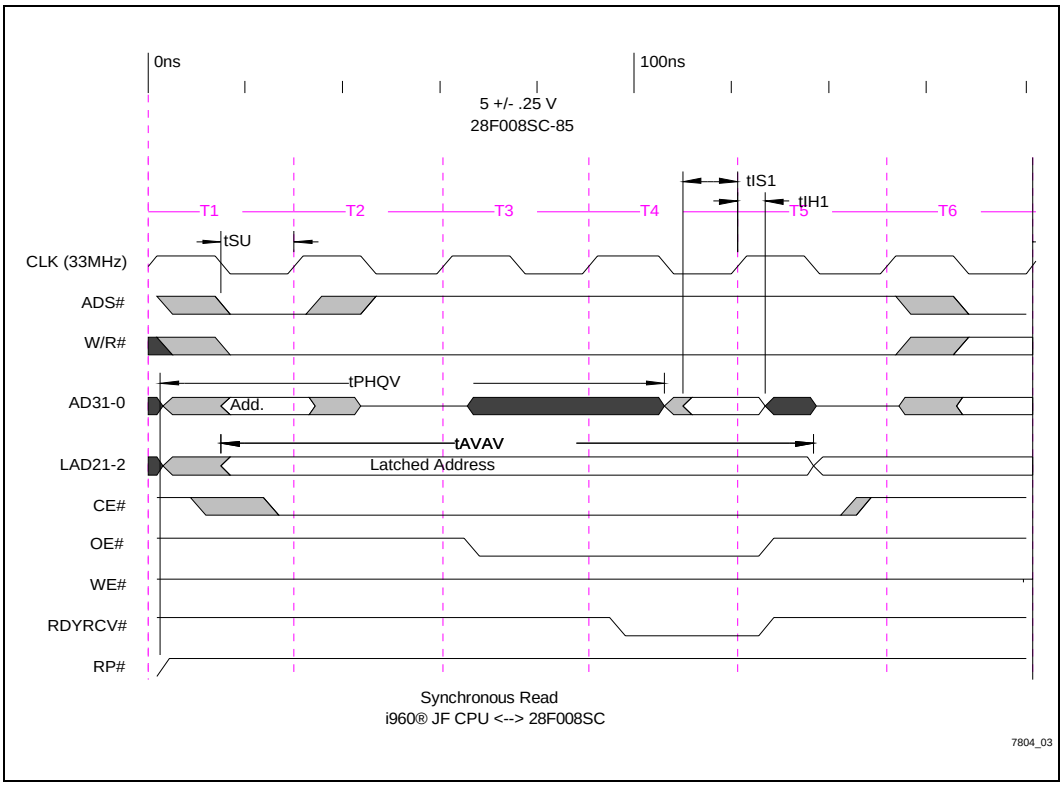

Figure 3. Read Cycle for i960® JF CPU Interface

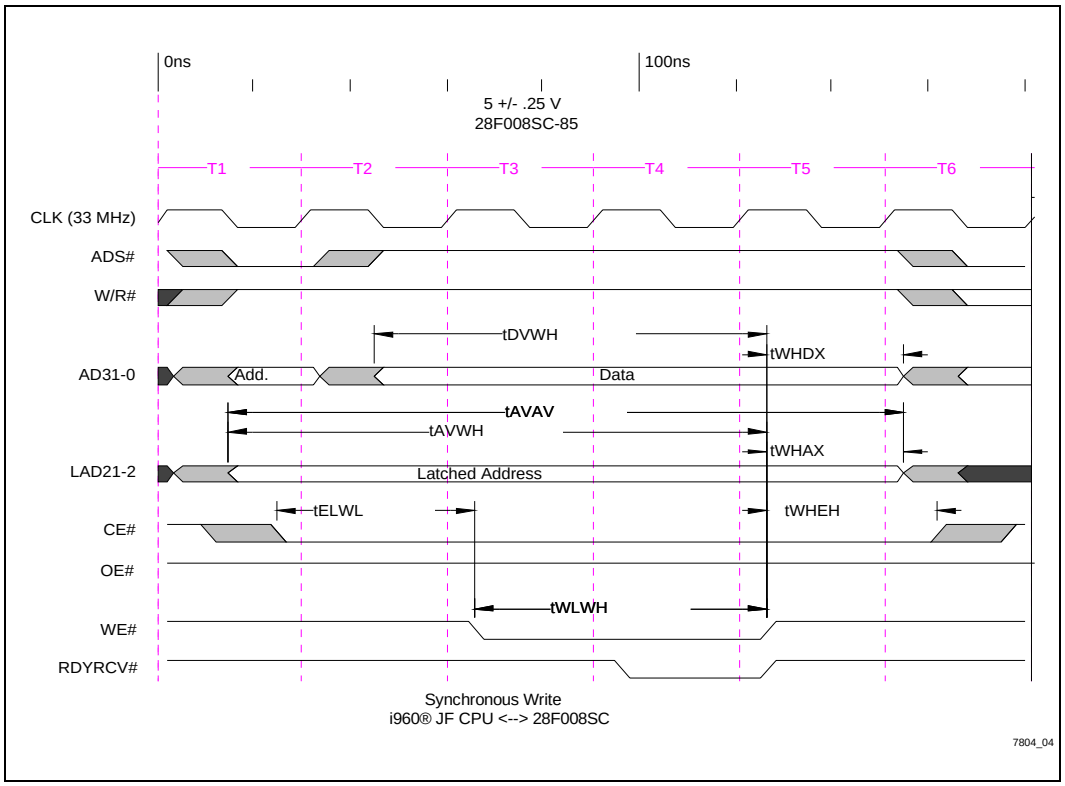

Figure 4. Write Cycle for i960® JF CPU Interface

2.1.5 ALTERNATE INTERFACE CONFIGURATIONS

The following section describes the changes which must be made to the state machine described previously to interface at different i960 JF CPU frequencies as well as different 28F008SC speeds.

3.3V V_{CC} Operation: When operating at 16 MHz, state S4 in the write cycle is omitted when both 28F008SC-120s and -150s are used. When running at 25 MHz, one wait-state is inserted between states S2 and S3 in the read cycle for 28F008SC-150s.

5V V_{CC} Operation: For operation at 16 MHz, state S4 is omitted from the write cycle for all 28F008SC speeds. State S2 of the read cycle is omitted when interfacing to 28F008SC-85s and -90s at 16 MHz. For 33 MHz operation, a wait-state is inserted between states S2 and S3 in the read cycle when using 28F008SC-120s.

Table 3 and Table 4 summarize these changes. A “NC” entry in the table signifies that “No Change” is necessary to the state diagram described above to work in this configuration. A “WS Sx→Sy” entry means a wait-state must be inserted between states Sx and Sy of the state machine. If a state can be omitted from the state machine, a “Skip Sx” is the table entry.

2.1.6 INTERFACING THE i960® JF MICROPROCESSOR TO OTHER FLASH COMPONENTS

For the 28F008SC designs described earlier, Smart 3 (28F008S3) flash memory is interchangeable with the 28F008SC at 3.3V V_{CC} operation, and Smart 5 (28F008S5) flash memory is interchangeable with the 28F008SC at 5V V_{CC} operation.

This section describes the changes necessary when interfacing with byte-wide 4- and 16-Mbit SmartVoltage (28F004SC/28F016SC), Smart 3 (28F004S3/28F016S3) or Smart 5 (28F004S5/28F016S5) flash memory.

Interfacing with 4-Mbit Components

When a 4-Mbit component is used, the AD_{21} pin becomes another input to the OR gate, requiring an 11-input OR gate in the interface design.

For 3.3V V_{CC} Operation: 28F004SC/S3-120s and -150s can replace 28F008SC/S3-120s and -150s, respectively, with no changes.

For 5V V_{CC} Operation: 28F004SC/S5-85s, -90s, and -120s can replace 28F008SC/S5-85s, -90s, and -120s, respectively, with no changes.

Table 3. 3V V_{CC} Interface Configurations

i960® JF CPU	28F008SC	
	-120 ns	-150 ns
16 MHz	**R:** NC **W:** Skip S4	**R:** NC **W:** Skip S4
25 MHz	**R:** NC **W:** NC	**R:** 1 WS S2→S3 **W:** NC

Table 4. 5V V_{CC} Interface Configurations

i960® JF CPU	28F008SC		
	-85 ns	-90 ns	-120 ns
16 MHz	**R:** Skip S2 **W:** Skip S4	**R:** Skip S2 **W:** Skip S4	**R:** NC **W:** Skip S4
25 MHz	**R:** NC **W:** NC	**R:** NC **W:** NC	**R:** NC **W:** NC
33 MHz	-----	**R:** NC **W:** NC	**R:** 1 WS S2→S3 **W:** NC

Interfacing with 16-Mbit Components

When a 16-Mbit component is used, the AD_{22} pin becomes an input to the flash device, requiring a 9-input OR gate in the interface design.

For 3V V_{CC} Operation: 28F016SC/S3-120s and -150s can replace 28F008SC3/S3-120s and -150s, respectively, with no changes.

For 5V V_{CC} Operation: 28F016SC/S5-95s and -100s can replace 28F008SC/S5-85s and -90s, respectively, with one modification. In the 33 MHz interface, a wait-state is necessary between states S2 and S3 of the read cycle.

28F016SC/S5-120s can replace 28F008SC/S5-120s with no changes.

2.2 i960® RP Microprocessor Interface at 33 MHz

The i960® RP processor is a 5V V_{CC} only, 32-bit RISC embedded processor with a 32-bit multiplexed address/data bus. The i960 RP processor combines many features with the i960 JF processor creating an intelligent I/O processor.

2.2.1 PROCESSOR INTERFACE SIGNALS

System logic uses the signals described in Table 5 in interfacing the 28F008SC to the i960 RP processor.

2.2.2 INTERFACE CONSIDERATIONS

The following discussion considers the interfacing of the 5V V_{CC} i960 RP processor operating at 33 MHz to 28F008SC-85s.

This design (shown in Figure 5) uses four 28F008SC-85s to match the 32-bit data bus of the i960 RP processor, providing 4 Mbytes of flash memory. Four octal latches, enabled by the ALE signal, de-multiplex the address from the AD bus. The latched address bits AD_{21}–AD_2 select locations within the 28F008SC-85s' memory space.

CLK Option

A 33 MHz clock signal drives the i960 RP processor S_CLK input.

Reset

An active-low reset signal, RESET#, drives the P_RST# input of the i960 RP processor and the RP# input of the 28F008SC-85s.

Control Signal Generation

Combinational logic using the upper ten bits of the latched address and the byte enable signals generates the CE# control signals for the 28F008SC-85s. The upper ten bits are used to determine if the bus cycle is directed to the flash's memory space. This logic is a ten-input OR gate, and the address range depicted in the schematic is 00000000h–003FFFFFh. If the memory range desired for the flash memory is 80000000h–803FFFFFh, the AD_{31} input to the OR gate is inverted. The processor's DT/R# signal OR'd with the processor's DEN# signal, after a 10 ns delay, controls the OE# input of the 28F008SC-85. The DEN# signal must be delayed 10 ns to avoid the bus contention possible as the processor drives the address and the flash's data pins transition to a low impedance state. The WE# input of the 28F008SC-85 is controlled by the inverted DT/R# signal OR'd with the delayed DEN# signal. The wait-states necessary for the bus transfers are controlled by the on-board wait-state generator.

Table 5. i960® RP Processor Pin Descriptions

Sym	Type	Name and Function
AD31:0	I/O	**ADDRESS/DATA BUS:** Multiplexed address and data bus.
ALE	O	**ADDRESS LATCH ENABLE:** Indicates the transfer of a physical address.
ADS#	O	**ADDRESS STROBE:** Indicates a valid address and the start of a new bus access.
BE3:0#	O	**BYTE ENABLES:** Select which of up to four data bytes on the bus participate in the current bus access.
DEN#	O	**DATA ENABLE:** Indicates data transfer cycles during a bus access.
DT/R#	O	**DATA TRANSMIT/RECEIVE:** Indicates the direction of data transfer to (0) and from (1) the address/data bus.
W/R#	O	**WRITE/READ:** Specifies whether the operation is a write (1) or a read (0).
RDYRCV#	I	**READY/RECOVER:** Indicates that data on AD lines can be sampled or removed; controls the insertion of wait-states.
S_CLK	I	**SECONDARY PCI BUS CLOCK:** Provides the processor's fundamental timing in synchronous model; all input/output timings are relative to S_CLK.

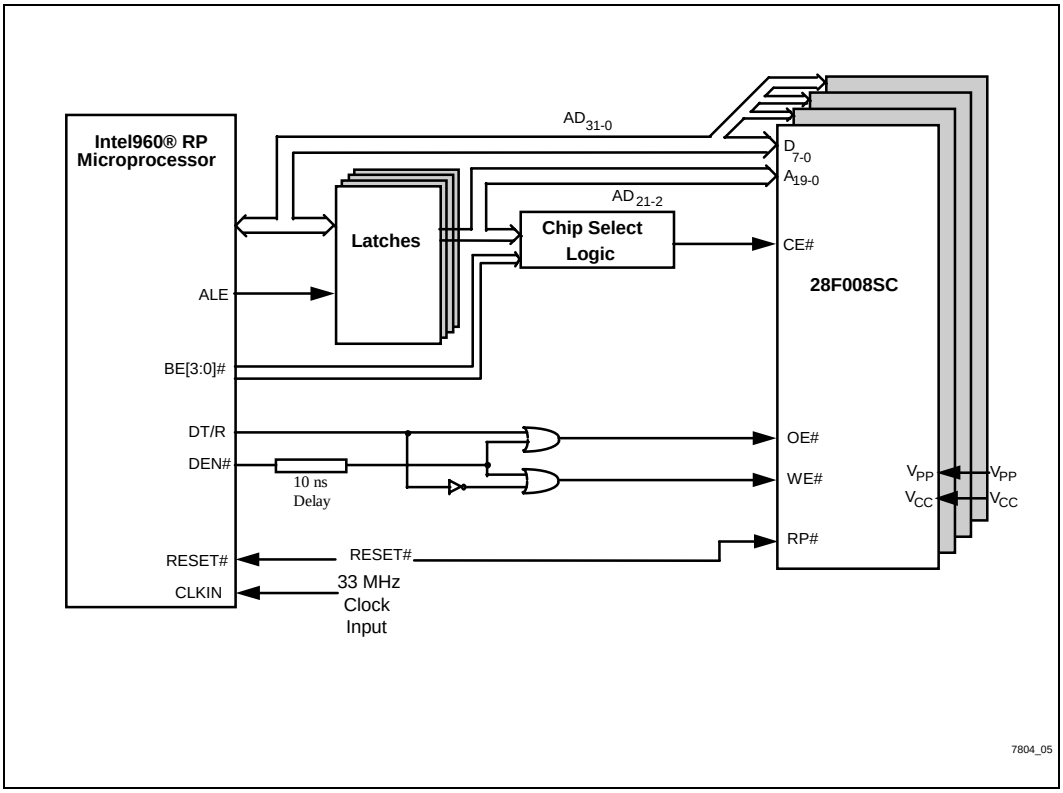

Figure 5. 28F008SC Interface to the i960® RP CPU

2.2.3 READ CYCLE DESCRIPTION

Refer to the read cycle timing diagram (Figure 6) for the following discussion of the read cycle.

After the i960 RP processor initiates a read cycle by asserting ADS# (end of T1 cycle), the processor's DEN# signal is asserted a time t_{OV2} later. The DEN# signal is delayed an additional 10 ns. The DT/R# signal is also valid, logic 0, at this time, and this signal OR'd with the delayed DEN# signal force OE# low. After two programmed wait-states, the processor reads the data presented at the end of the T4 cycle, and the DEN# signal is deasserted a time t_{OV2} later. After the delay, the deassertion of DEN# forces OE# high.

2.2.4 WRITE CYCLE DESCRIPTION

Refer to the write cycle timing diagram (Figure 7) for the following discussion of the write cycle.

After the i960 RP processor initiates a write cycle by asserting ADS# (end of T1 cycle), the processor's DEN# signal is asserted a time t_{OV2} later. The DEN# is further delayed 10 ns. The DT/R# signal is also valid, logic "1," at this time, and the negation of this signal OR'd with the delayed DEN# forces WE# low. After one programmed wait-state, the processor deasserts the DEN# signal. After the delay, the deassertion of DEN# forces WE# high. WE# going high causes the 28F008SC-85s to latch the address and the data to be written.

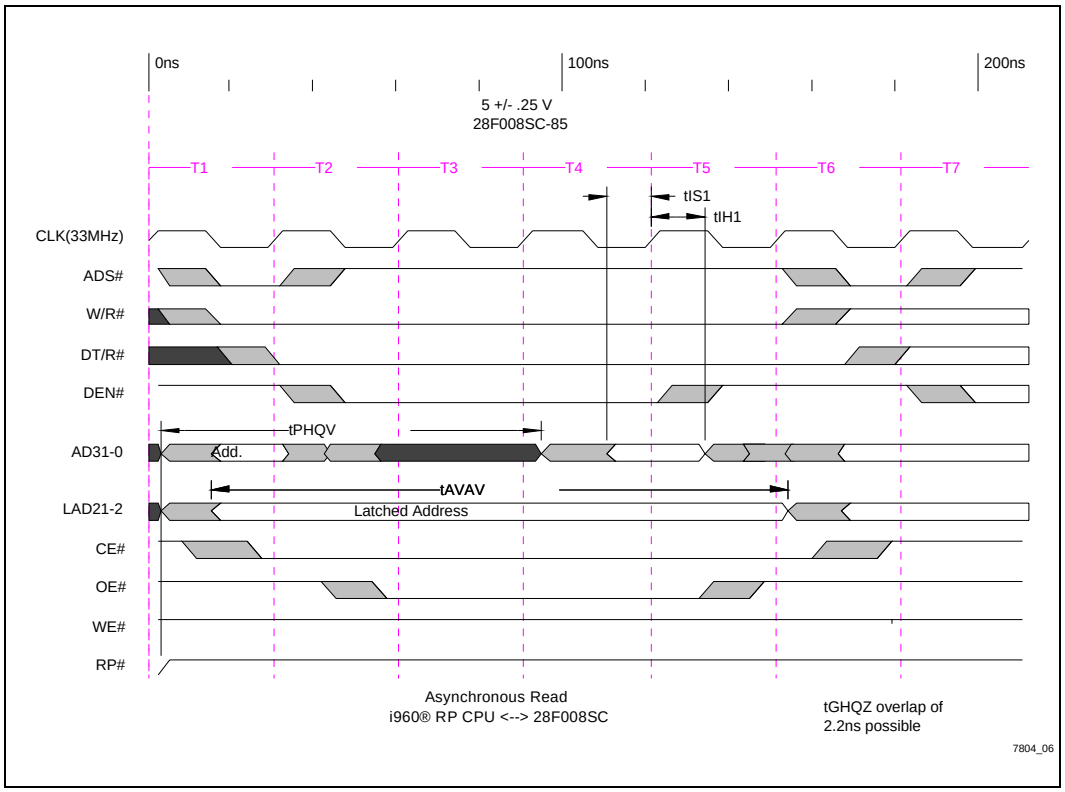

Figure 6. Read Cycle for i960® RP CPU Interface

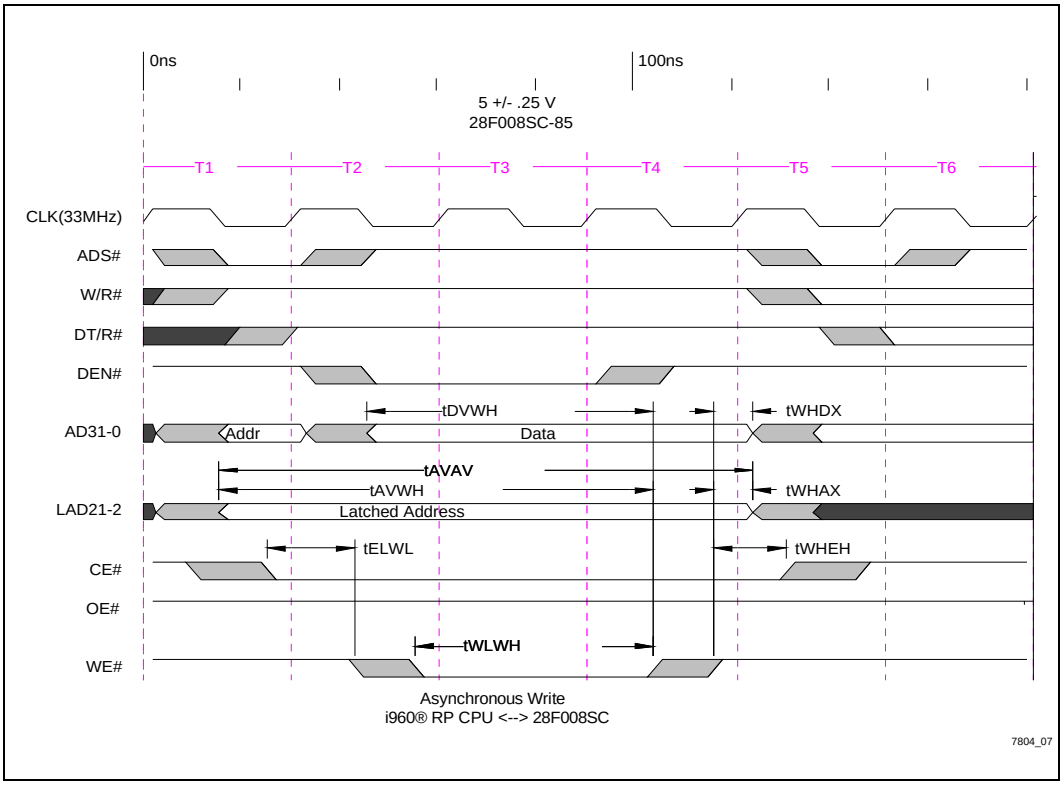

Figure 7. Write Cycle for i960® RP CPU Interface

2.2.5 ALTERNATE INTERFACE CONFIGURATIONS

The following section describes the changes which must be made to the design described earlier to interface at different 5V V_{CC} i960 RP CPU frequencies as well as different 28F008SC speeds.

When operating at 16 MHz, 28F008SC-85s, -90s, and -120s need one wait-state for the read cycle and zero wait-states for the write cycle. At 25 MHz, 28F008SC-85s require one wait-state for both read and write cycles, and -90s and -120s use the same number of wait-states as the 33 MHz design described previously. At 33 MHz, 28F008SC-90s and -120s require three wait-states for the read cycle, and 28F008SC-90s require one wait-state for the write cycle while 28F008SC-120s require two wait-states for the write cycle.

Table 6 summarizes these changes. A “NC” entry in the table signifies that “No Change” is necessary for the interface to work in this configuration. If the number of programmed wait-states is different from the interface described above, the number of wait-states **which must be programmed** is given in the table.

Table 6. 5V V_{CC} Interface Configurations

i960® RP CPU	28F008SC		
	-85 ns	-90 ns	-120 ns
16 MHz	**R:** 1 WS **W:** 0 WS	**R:** 1 WS **W:** 0 WS	**R:** 1 WS **W:** 0 WS
25 MHz	**R:** 1 WS **W:** 1 WS	**R:** NC **W:** NC	**R:** NC **W:** NC
33 MHz	**----**	**R:** 3 WS **W:** 1 WS	**R:** 3 WS **W:** 2 WS

2.2.6 INTERFACING THE i960® RP MICROPROCESSOR TO OTHER FLASH COMPONENTS

For the 28F008SC designs described earlier, Smart 5 (28F008S5) flash memory is interchangeable with the 28F008SC at 5V V_{CC} operation.

This section describes the changes necessary when interfacing with byte-wide 4- and 16-Mbit SmartVoltage (28F004SC/28F016SC) or Smart 5 (28F004S5/28F016S5) flash memory.

Interfacing with 4-Mbit Components

When a 4-Mbit component is used, the AD_{21} pin becomes another input to the OR gate, requiring an 11-input OR gate in the interface design.

28F004SC/S5-85s, -90s, and -120s can replace 28F008SC/S5-85s, -90s, and -120s, respectively, with no changes.

Interfacing with 16-Mbit Components

When a 16-Mbit component is used, the AD_{22} pin becomes an input to the flash device, requiring a 9-input OR gate in the interface design.

28F016SC/S5-95s can replace 28F008SC/S5-85s with the following change—an additional wait-state is needed for the read cycle at both 25 and 33 MHz. 28F016SC/S5-100s and 28F016SC/S5-120s can replace 28F008SC/S5-90s and -120s, respectively, with no changes.

2.3 i960® Hx Microprocessor Interface at 33 MHz

The i960® Hx series processors are 32-bit RISC microprocessors with separate 32-bit address and data buses. The i960 Hx series are 3.3V V_{CC} processors which have a 5V tolerance, enabling these processors to interface to both 3.3V and 5V flash devices if the 5V supply is ±5 %.

2.3.1 PROCESSOR INTERFACE SIGNALS

System logic uses the signals described in Table 7 in interfacing the 28F008SC to the i960 Hx processor.

2.3.2 INTERFACE CONSIDERATIONS

The following discussion considers the interfacing of the i960 Hx processor operating at 33 MHz (5V V_{CC}) to 28F008SC-85s.

This design (shown in Figure 8) uses four 28F008SC-85s to match the 32-bit data bus of the i960 Hx processor, providing 4 Mbytes of flash memory. The address bits A_{21}–A_2 along with BE3:0# select locations within the 28F008SC-85s' memory space.

CLK Option

A 33 MHz clock signal drives the i960 Hx processor CLKIN input.

Reset

An active-low reset signal, RESET#, drives the RESET# inputs of the i960 Hx processor and the RP# input of the 28F008SC-85s.

Control Signal Generation

Combinational logic using the upper ten bits of the latched address and the byte enable signals generates the CE# control signals for the 28F008SC-85s. The upper ten bits are used to determine if the bus cycle is directed to the flash's memory space. This logic is a ten-input OR gate, and the address range depicted in the schematic is 00000000h–003FFFFFh. If the memory range desired for the flash memory is 80000000h–803FFFFFh, the A_{31} input to the OR gate is inverted. The processor's DT/R# signal OR'd with the processor's DEN# signal controls the OE# input of the 28F008SC-85. The WE# input of the 28F008SC-85 is controlled by the inverted DT/R# signal OR'd with the DEN# signal. The wait-states necessary for the bus transfers are controlled by the on-board wait-state generator.

Table 7. i960® Hx Processor Pin Descriptions

Sym	Type	Name and Function
A31:2	O	**ADDRESS BUS:** Carries the upper 30 bits of the physical address.
D31:0	I/O	**DATA BUS:** Data bus.
ADS#	O	**ADDRESS STROBE:** Indicates a valid address and the start of a new bus access.
BE3:0#	O	**BYTE ENABLES:** Select which of up to four data bytes addressed by A31:2 are active during a bus access.
DEN#	O	**DATA ENABLE:** Indicates data transfer cycles during a bus access.
DT/R#	O	**DATA TRANSMIT/RECEIVE:** Indicates the direction of data transfer to (0) and from (1) the address/data bus.
W/R#	O	**WRITE/READ:** Specifies whether the operation is a write (1) or a read (0).
READY#	I	**READY:** Indicates that data on data bus can be sampled or removed; controls the insertion of wait-states.
CLKIN	I	**CLOCK INPUT:** Provides the time base for the i960 Hx processor.

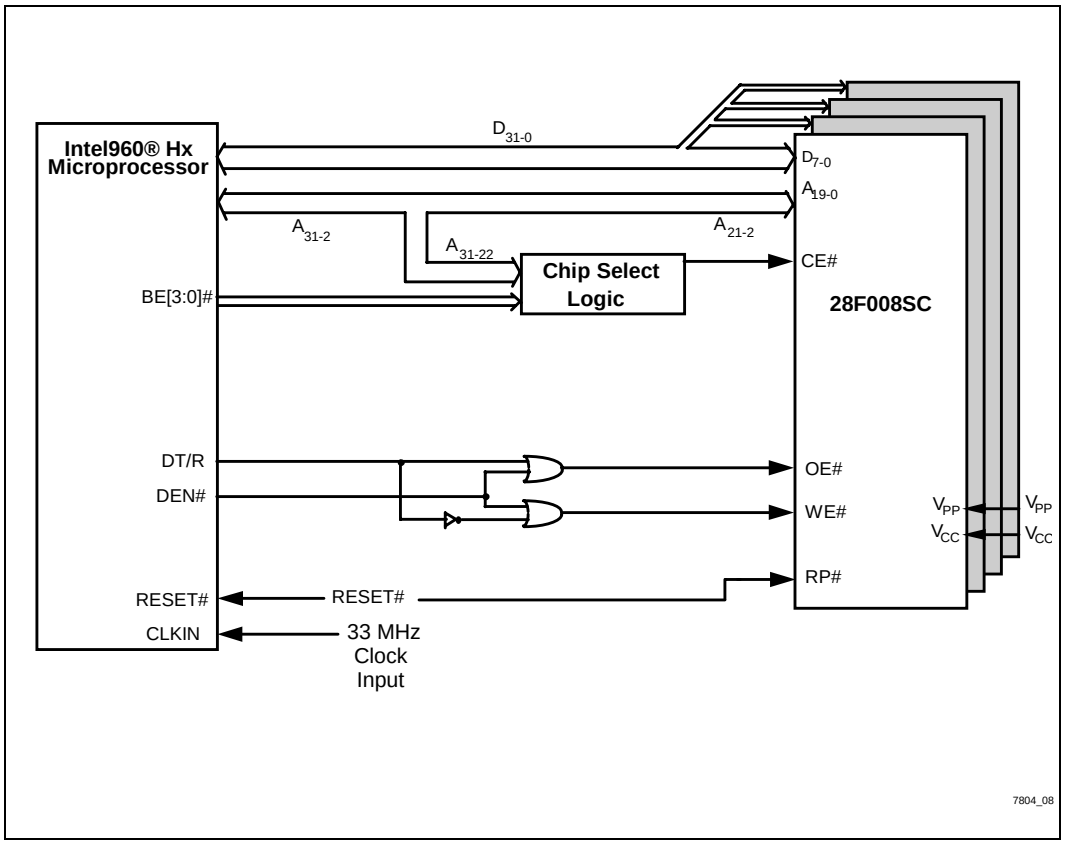

Figure 8. 28F008SC Interface to the i960® Hx CPU

2.3.3 READ CYCLE DESCRIPTION

Refer to the read cycle timing diagram (Figure 9) for the following discussion of the read cycle.

After the i960 Hx processor initiates a read cycle by asserting ADS# (after T1 cycle), the processor's DEN# signal is asserted a time t_{OV2} later. The DT/R# signal is also valid, logic "0," at this time, and these two signals OR'd together force OE# low. After two programmed wait-states, the processor reads the data presented at the end of the T4 cycle, and the DEN# signal is deasserted a time t_{OV2} later, forcing OE# high.

2.3.4 WRITE CYCLE DESCRIPTION

Refer to the write cycle timing diagram (Figure 10) for the following discussion of the write cycle.

After the i960 Hx processor initiates a write cycle by asserting ADS# (end of T1 cycle), the processor's DEN# signal is asserted a time t_{OV2} later. The DT/R# signal is also valid, logic "1," at this time, and these two signals OR'd together force WE# low. After one programmed wait-state, the processor deasserts the DEN# signal at the end of the T3 cycle, forcing WE# high. WE# going high causes the 28F008SC to latch the address and data to be written.

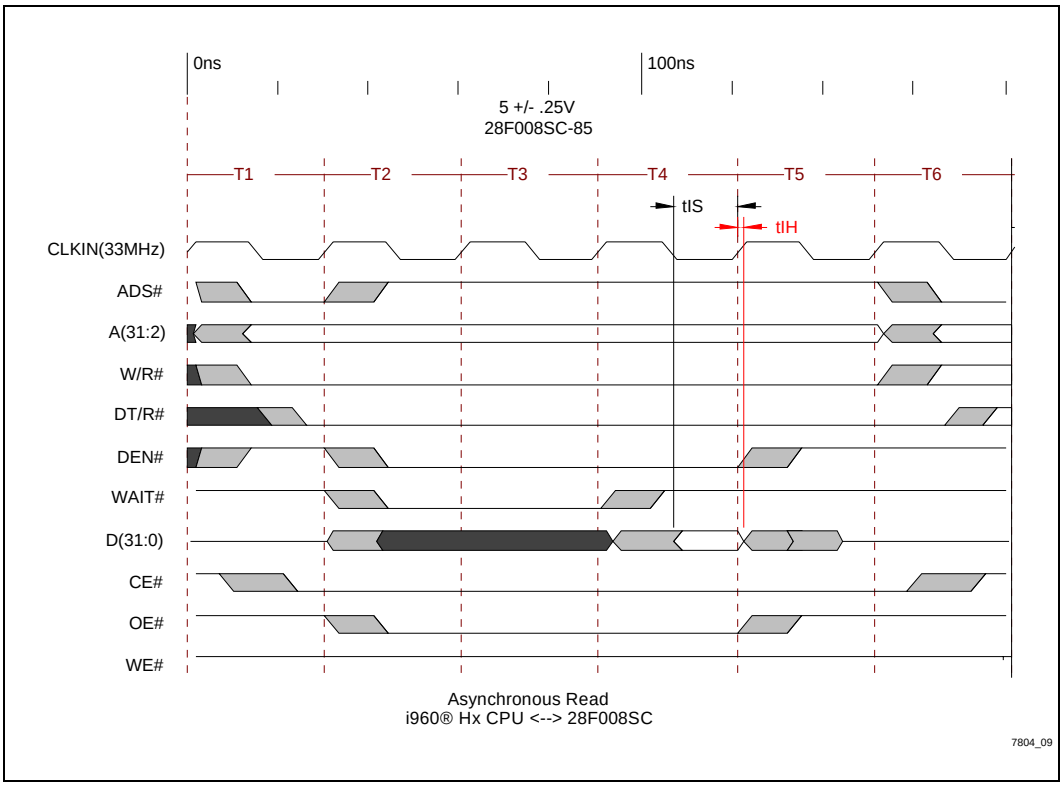

Figure 9. Read Cycle for i960® Hx CPU Interface

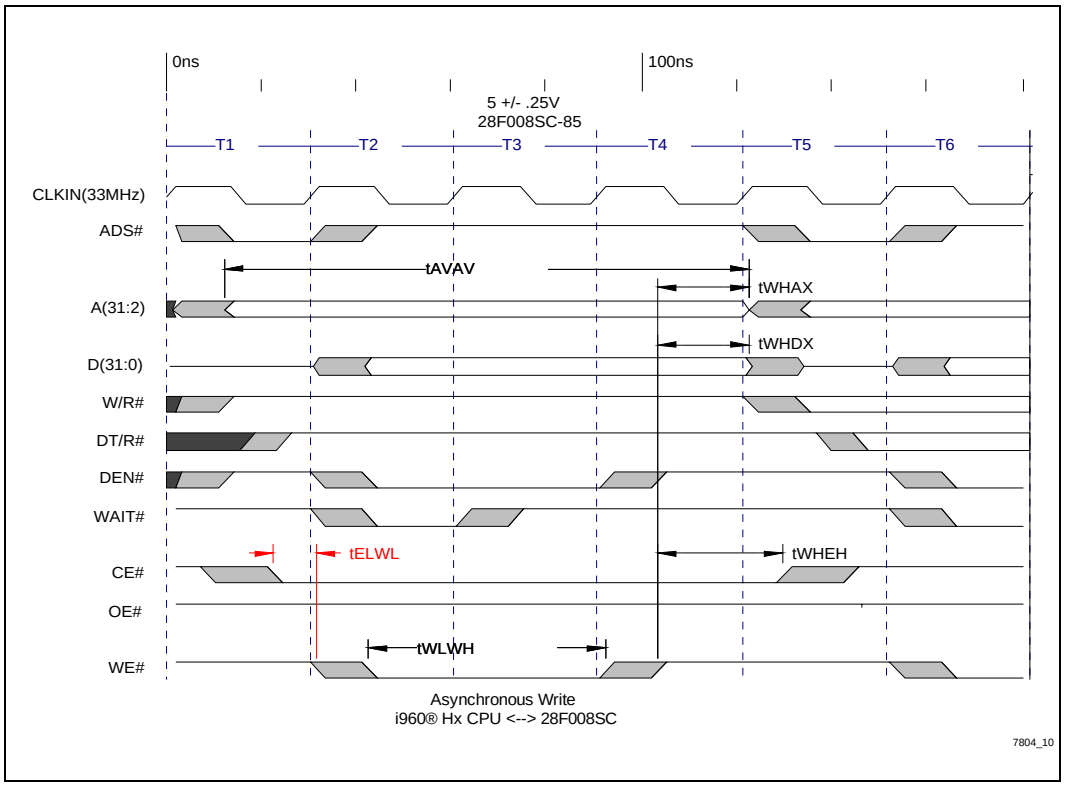

Figure 10. Write Cycle for i960® Hx CPU Interface

2.3.5 ALTERNATE INTERFACE CONFIGURATIONS

The following section describes the changes which must be made to the design described earlier to interface at different i960 Hx CPU frequencies as well as different 28F008SC speeds.

3.3V V_{CC} Operation: When operating at 25 MHz, 28F008SC-120s need two wait-states and -150s need three wait-states for the read cycle. For the write cycle, one wait-state is needed for both -120s and -150s. At 33 MHz and interfacing to 28F008SC-120s, three wait-states and two wait-states are necessary for the read and write cycles, respectively. For the read and write cycles of 28F008SC-150s, four and three wait-states, respectively, must be programmed into the wait-state generator.

5V V_{CC} Operation: For operation at 25 MHz, one wait-state is needed for both the read and write cycles when 28F008SC-85s or -90s are used. If 28F008SC-120s are used at 25 MHz, two wait-states are required for the read cycle while one is needed for the write cycle. At 33 MHz, 28F008SC-90s use the same number of wait-states as the design described previously. If 28F008SC-120s are used, three wait-states are required for the read cycle and two waits for the write cycle.

Table 8 and Table 9 summarize these changes. A “NC” entry in the table signifies that “No Change” is necessary for the interface to work in this configuration. If the number of programmed wait-states is different from the interface described above, the number of wait-states **which must be programmed** is given in the table.

Table 8. 3V V_{CC} Interface Configurations

i960® Hx CPU	28F008SC	
	-120 ns	-150 ns
25 MHz	**R:** 2 WS **W:** 1 WS	**R:** 3 WS **W:** 1 WS
33 MHz	**R:** 3 WS **W:** 2 WS	**R:** 4 WS **W:** 3 WS

Table 9. 5V V_{CC} Interface Configurations

i960® Hx CPU	28F008SC		
	-85 ns	-90 ns	-120 ns
25 MHz	**R:** 1 WS **W:** 1 WS	**R:** 1 WS **W:** 1 WS	**R:** NC **W:** NC
33 MHz	----	**R:** NC **W:** NC	**R:** 3 WS **W:** 2 WS

2.3.6 INTERFACING THE i960® HX PROCESSOR TO OTHER FLASH COMPONENTS

For the 28F008SC designs described earlier, Smart 3 (28F008S3) flash memory is interchangeable with the 28F008SC at 3.3V V_{CC} operation, and Smart 5 (28F008S5) flash memory is interchangeable with the 28F008SC at 5V V_{CC} operation.

This section describes the changes necessary when interfacing with byte-wide 4- and 16-Mbit SmartVoltage (28F004SC/28F016SC), Smart 3 (28F004S3/28F016S3) or Smart 5 (28F004S5/28F016S5) flash memory.

Interfacing with 4-Mbit Components

When a 4-Mbit component is used, the A_{21} pin becomes another input to the OR gate, requiring an 11-input OR gate in the interface design.

For 3.3V V_{CC} Operation: 28F004SC/S3-120s and -150s can replace 28F008SC/S3-120s and -150s, respectively, with no changes.

For 5V V_{CC} Operation: 28F004SC/S5-85s, -90s, and -120s can replace 28F008SC/S5-85s, -90s, and -120s, respectively, with no changes.

Interfacing with 16-Mbit Components

When a 16-Mbit component is used, the A_{22} pin becomes an input to the flash chip, requiring a 9-input OR gate in the interface design.

For 3.3V V_{CC} Operation: 28F016SC/S3-120s and -150s can replace28F008SC/S3-120s and -150s, respectively, with no changes.

For 5V V_{CC} Operation: 28F016SC/S5-95s can replace 28F008SC/S5-85s with one modification. In the 25 MHz interface, an additional wait-state is necessary for the read cycle.

28F016SC/S5-100s can replace 28F008SC/S5-90s if an additional wait-state is added to both the 25 and 33 MHz read cycles.

28F016SC/S5-120s can replace 28F008SC/S5-120s with no changes.

APPENDIX A
ADDITIONAL INFORMATION

Related Intel Documentation(1,2)

Order Number	Document
290600	*Byte-Wide SmartVoltage FlashFile™ Memory Family Datasheet*
290597	*Byte-Wide Smart 5 FlashFile™ Memory Family Datasheet*
290598	*Byte-Wide Smart 3 FlashFile™ Memory Family Datasheet*
272504	*80960JA/JF Embedded 32-Bit Microprocessor Datasheet*
272744	*80L960JA/JF 3.3V Embedded 32-Bit Microprocessor Datasheet*
272737	*80960RP Intelligent I/O Microprocessor Datasheet*
272495	*80960HA/HD/HT 32-Bit High-Performance Superscalar Processor Datasheet*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.