



80960SA/SB

SPECIFICATION UPDATE

Release Date: July, 1996

Order Number: 272850-001

The 80960SA/SB may contain design defects or errors known as errata. Characterized errata that may cause the 80960SA/SB's behavior to deviate from published specifications are documented in this specification update.



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The 80960SA/SB may contain design defects or errors known as errata. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

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Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Intel currently manufactures only the C stepping of the 80960SA and only the B stepping of the 80960SB. The 80960SB B stepping has one erratum, and the 80960SA C stepping has no errata.

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 80960SA/SB Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Electrical specifications for these products are found in the following documents:

Title	Order
<i>80960SA Embedded 32-Bit Microprocessor with 16-bit Burst Data Bus datasheet</i>	272206-002
<i>80960SB Embedded 32-Bit Microprocessor with 16-bit Burst Data Bus datasheet</i>	272207-001

Functional descriptions for these products are found in the following documents:

Title	Order
<i>i960® SA/SB Microprocessor Reference Manual</i>	270929-003

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, and documentation changes which apply to the 80960SA/SB product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.
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Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are being evaluated.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.
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Errata

No.	Steppings				Page	Status	ERRATA
	A	A-1	B	C-1			
9600001	X				7	Fixed	Byte Enables Switch Prematurely with Wait States
9600002	X				9	Fixed	Data Bus Invalid after First Wait State
9600003	X	X			9	Fixed	INTA# Pulses Incorrect
9600004	X	X			10	Fixed	Byte Enables BE1:0# Inactive Until READY# Assertion
9600005	X	X	X		10	Fixed	FAIL# Pin Malfunction
9600006			X		10	Fixed	Breakpoint Register Initialization
9600007			X		11	Fixed	Extra Idle State During Interrupt Acknowledge Cycle

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.



IDENTIFICATION INFORMATION

Markings

As of January 1994, all N80960SA, S80960SA, and N80960SB devices will be marked with stepping numbers. Status column indicates affected products with asterisk (*).

80960SA/SB steppings are identified by specification numbers from the following list:

Part #	Specification #	Stepping	Package	Status
N80960SA	C1	C-1	PLCC	*Current
S80960SA	C1	C-1	QFP-EIAJ	*Current
N80960SB	B	B	PLCC	*Current
N80960SA	Q 8244	C-1	PLCC	Current
S80960SA	Q 8261	C-1	QFP-EIAJ	Current
TN80960SA	Q 8341	C-1	PLCC	Current
N80960SA	C1 S W225	C-1	PLCC (T & R)	*Current
N80960SA	C1 S W226	C-1	PLCC (T & R)	*Current
N80960SA	C1 S W227	C-1	PLCC (T & R)	*Current
N80960SB	Q 8319	A	PLCC	Obsolete
S80960SB	Q 8320	A	QFP-EIAJ	Obsolete
C80960SB	Q 8322	A	CLCC	Obsolete
C80960SB	Q 8358	A-1	CLCC	Obsolete
N80960SB	Q 8374	A-1	PLCC	Obsolete
S80960SB	Q 8375	A-1	QFP-EIAJ	Obsolete
N80960SB	Q 8378	A-1	PLCC	Obsolete
N80960SB	Q 8465	A	PLCC	Obsolete
S80960SB	Q 8466	A	QFP-EIAJ	Obsolete
N80960SB	S V899	A-1	PLCC	Obsolete
S80960SB	S V900	A-1	QFP-EIAJ	Obsolete
N80960SA	S V943	A-1	PLCC	Obsolete
N80960SA	S V944	A-1	PLCC	Obsolete
N80960SB	S V945	A-1	PLCC	Obsolete
S80960SA	S V966	A-1	QFP-EIAJ	Obsolete
S80960SB	S V967	A-1	QFP-EIAJ	Obsolete
N80960SA	S V998	B	PLCC	Obsolete
N80960SA	S V999	B	PLCC	Obsolete
N80960SB	S W001	B	PLCC	Obsolete
N80960SB	S W002	B	PLCC	Obsolete
S80960SA	S W003	B	QFP-EIAJ	Obsolete
S80960SB	S W004	B	QFP-EIAJ	Obsolete
N80960SA	S W159	B	PLCC (T & R)	Obsolete
N80960SA	S W140	B	PLCC (T & R)	Obsolete
N80960SB	B S W025	B	PLCC (T & R)	*Current
N80960SB	B S W232	B	PLCC (T & R)	*Current

ERRATA**9600001. *Byte Enables Switch Prematurely with Wait States***

PROBLEM: During many accesses with wait states, the BE1:0# signals incorrectly switch after the first Tw state. The affected accesses include:

- All byte accesses with wait states.
- All quad-word, triple-word, long-word, word or short-word accesses with single-byte misalignment and wait states.

If the bus cycle is a burst access, the problem occurs on each data transfer within the burst. This problem will not occur if READY# always goes active early enough to signal zero wait states.

IMPLICATION: User systems and software may exhibit erroneous behavior.

WORKAROUND: Do not use the READY# input; tie it to a LOW logic state. If wait states are necessary, gate the input clock using external logic.

Figure 1 illustrates example workaround logic. A programmable logic device (PLD) driven by a 4X clock oscillator provides a 2X clock for the 80960SA/SB and other system clocks. READY# is an input to the PLD which stops the 2X clock whenever it is asserted. When READY# is deasserted, the PLD resynchronizes the 2X clock to the system clocks. Figure 2 is a state diagram of the workaround.

The 80960SA/SB has dynamic registers, so do not stop its input clock for more than about one microsecond. This restriction limits the number of wait states to about nine for a 10 MHz 80960SA/SB.

The workaround also reduces the overall performance of the microprocessor since it cannot execute instructions while its clock is stopped.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600002. *Data Bus Invalid after First Wait State*

PROBLEM: During certain write cycles with wait states, the data are valid only during the first Tw state. The affected accesses include:

- All byte writes with wait states.
- All short-word writes with wait states.
- All quad-word, triple-word, long-word or word writes with single-byte or short-word misalignment and wait states.

If the bus cycle is a burst access, the problem occurs on each data transfer within the burst.

WORKAROUND: This erratum is related to #1 and the workaround is identical. Do not use READY# to insert wait states.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600003. *INTA# Pulses Incorrect***PROBLEM:**

- A. During interrupt acknowledge sequences, INTA# does not transition high between the two bus accesses which comprise the cycle. An 8259A interrupt controller will fail because it will see just one long INTA# pulse, not two distinct pulses.
- B. A sequence of approximately twelve spurious INTA# pulses can occur during the processor self-test.

WORKAROUND:

- A. Generate a new INTA# signal by OR'ing DEN# with the 80960SA/SB INTA# output. The new signal will meet 8259A input requirements except that an additional wait state may be necessary.
- B. Ignore INTA# during self-test. A hardware fix is usually not necessary.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600004. *Byte Enables BE1:0# Inactive Until READY# Assertion*

PROBLEM: If the READY# input is active at the end of the address cycle, the byte enables operate correctly. If READY# is inactive at the end of the address cycle, the byte enables stay inactive through successive data cycles until READY# is activated. This problem only affects systems implemented as normally-not-ready.

WORKAROUND: The best workaround is implementation of a normally-ready system, i.e., READY# is asserted except when wait states are desired. For a normally-not-ready system, AND the AS# signal with the ready logic and connect the resulting output to the processor's READY# input.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600005. *FAIL# Pin Malfunction*

PROBLEM: During initialization, the BLAST#/FAIL# pin does not signal the outcome of the memory checksum test unless the internal self-test was selected during reset.

The combination of asserted BLAST#/FAIL# and deasserted BE1:0# indicates an initialization failure on the 80960SA/SB. When leaving reset, the 80960SX checks the states of the INT0#, INT1, INT3# and LOCK# pins to select initialization activity. After the processor passes or skips the internal self-test, the BLAST#/FAIL# pin goes active twice while the processor performs two quad word reads starting at 00000000H. If a zero checksum of the eight words is incorrect, the processor should again activate FAIL#, indicating an initialization failure. However, if the internal self-test was disabled, a failure is not indicated, regardless of the checksum. In all cases, an incorrect checksum shuts down the processor.

WORKAROUND: Pull INT0#, INT3# and LOCK# up to a HIGH state during reset to select the internal self-test.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600006. *Breakpoint Register Initialization*

PROBLEM: The 80960SX has two breakpoint registers; these can be written using the Set Breakpoint Register IAC only, and they cannot be read. Bits 2-31 of the register contain the address on which to break, and bit 1 enables or disables the breakpoint. These registers are not set to a specific value during initialization, and may be enabled upon powerup. This could cause sporadic breakpoints to occur if tracing is enabled in the process controls and breakpoint trace mode is enabled in the trace controls.

IMPLICATION: This errata does not affect the normal function of the breakpoint.

WORKAROUND: Disable the breakpoints using the Set Breakpoint Register IAC to set bit 1 of both registers to 1. In addition if breakpoints are not being used, do not set the breakpoint trace mode bit in the trace controls.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

960007. *Extra Idle State During Interrupt Acknowledge Cycle*

PROBLEM: There are 6 Ti states between the two INTA pulses of an Interrupt Acknowledge Cycle, rather than the 5 Ti states that are documented. In addition the W/R# pin will pulse high for one cycle during the first Ti state.

WORKAROUND: The Interrupt Request/Acknowledge Transaction still functions properly, with an additional cycle of latency.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

None for this revision of this specification update.