Intelligent I/O Architecture

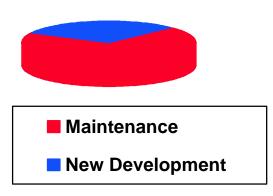
I₂**O**

PCI Spring Developers' Conference and Expo

Mark L. Brown Intel Corporation (602) 554-3864



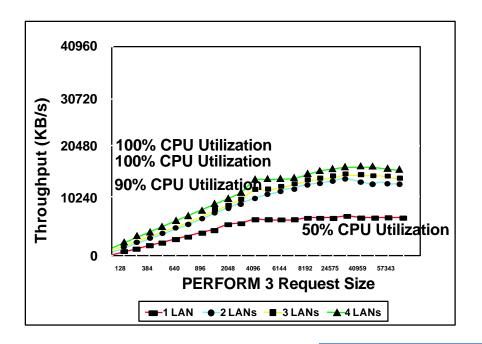
- I/O Scalability is Limited
 - Performance
 - Connectivity
- Introduction of New I/O Technology
 - Slow to market
 - Development funds limited due to maintenance costs



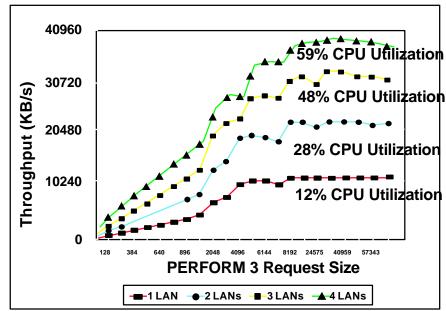


Intelligent I/O Performance Analysis for Fast Ethernet

Server performance with four PRO/100 adapters



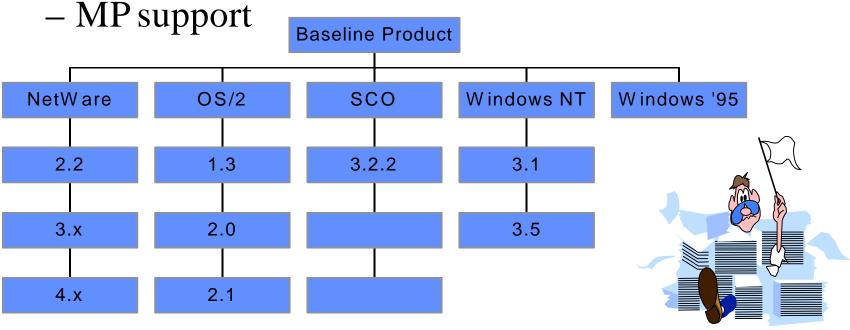
Server performance with four intelligent PRO/100 Server Adapters



Source: Intel Benchmarks



- Device Driver Dilemma
 - Proliferation of network operating systems





- Create standard OS interface to system I/O
- Enable intelligent I/O devices
- Interoperability between I/O devices
- Enable Peer-to-Peer I/O Communication
- Enable rapid deployment of I/O technology
- Co-exist with legacy drivers

Create an industry standard I/O architecture.



- Consistent driver model across multiple operating environments
 - Device firmware is OS & system independent
 - Enable a single binary image for a target execution environment
- Reduced device driver development costs
- Focus on introduction of new technology
- Reduced cost of intelligent I/O



OS specific code defined by OS vendor

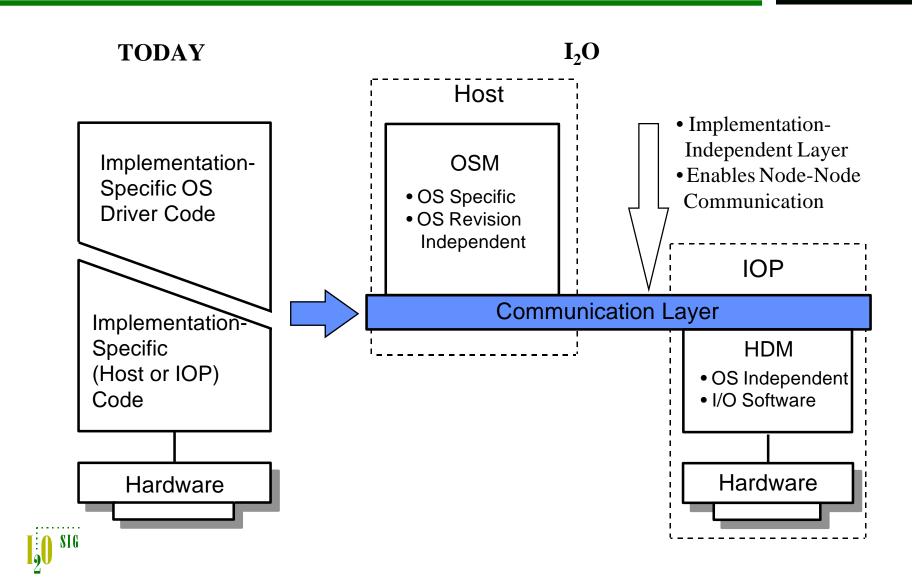
I/O Class specific code

I/O device specific code defined by H/W implementation

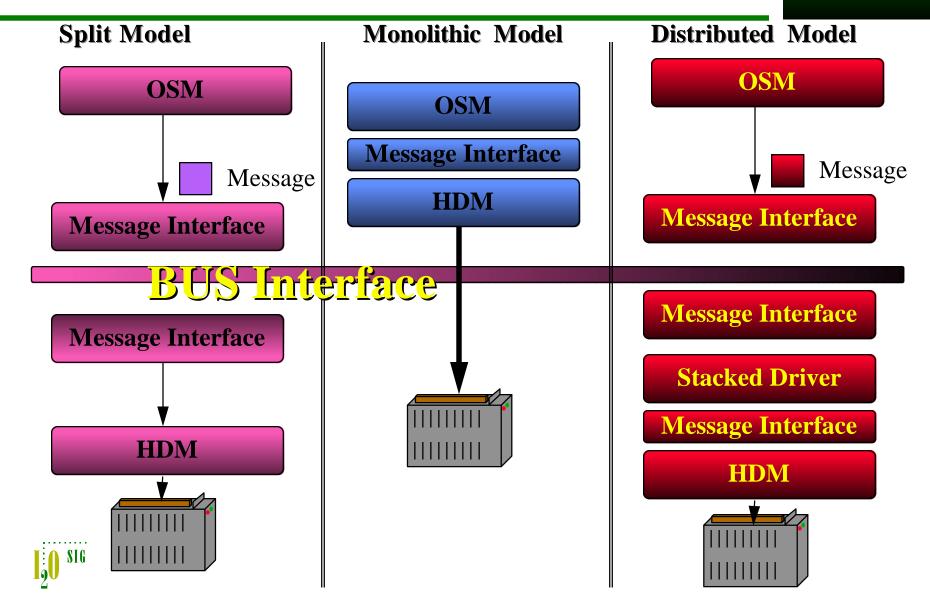
Hardware



I₂O Split Driver Model

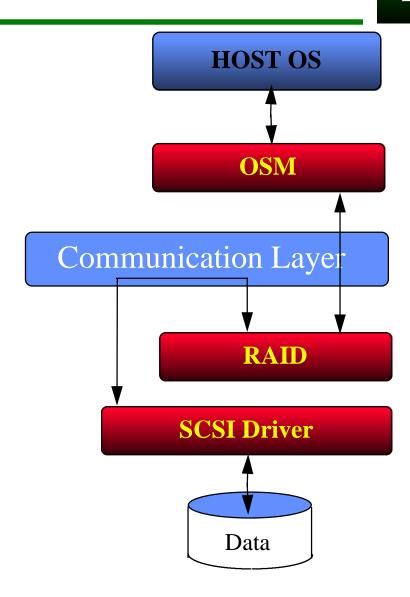


Conceptual Overview



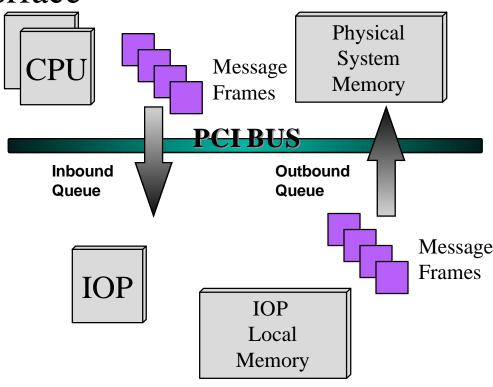
Layered architecture promotes stackable drivers

Value-add at multiple levels



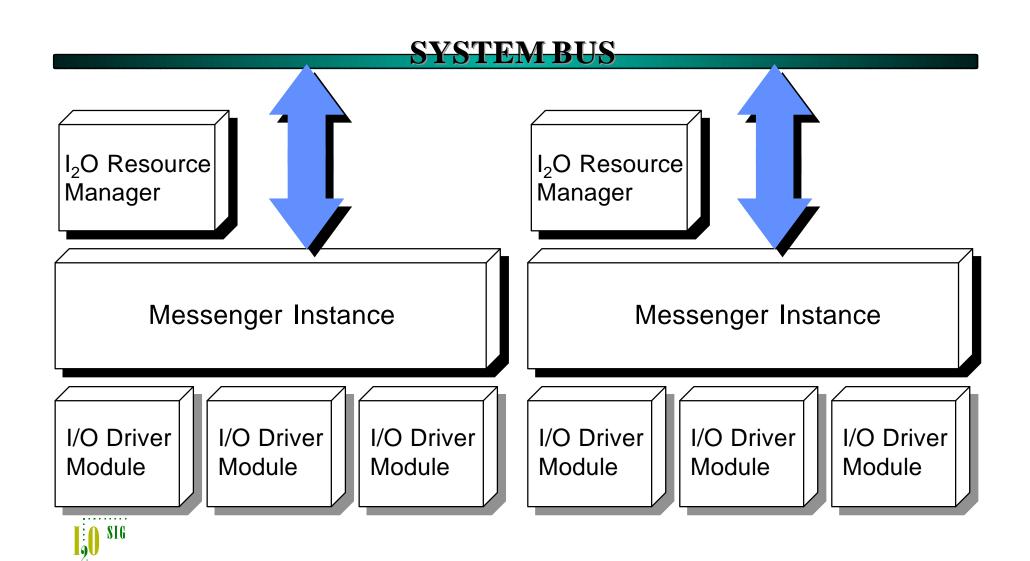


- Allows OS to batch I/O requests
 - Eliminates CPU stall during I/O transactions
 - Increases system TPS
- Consistent hardware interface
 - Simplified software model for I₂O driver
 - OS support becomes pervasive
 - Narrows requirements for compliance

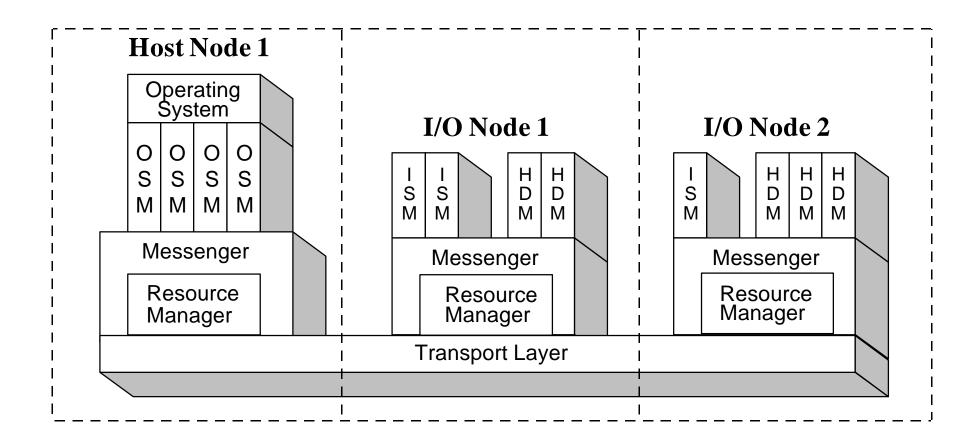




Communication Service Model

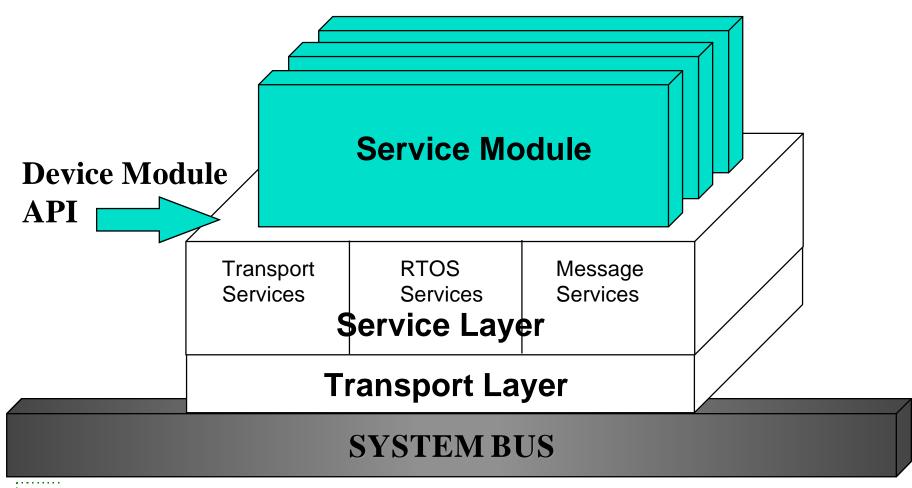


I₂O Software Architecture



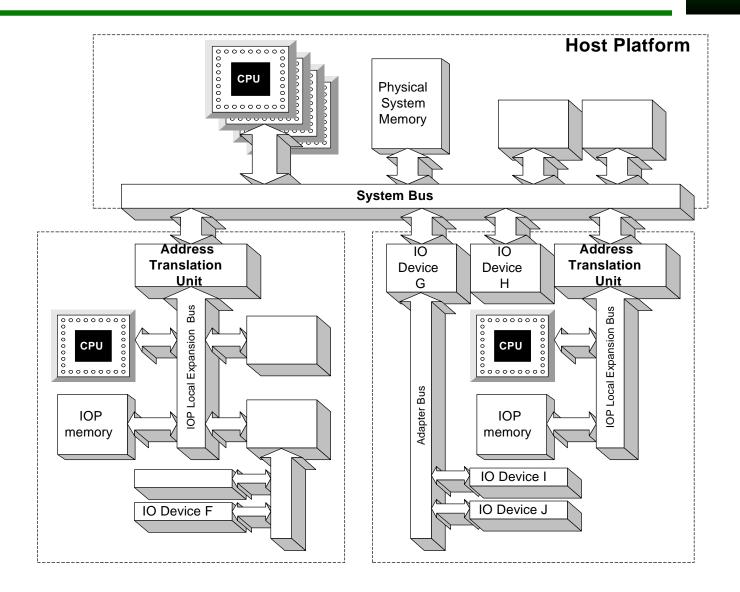


I₂O Message Service Model





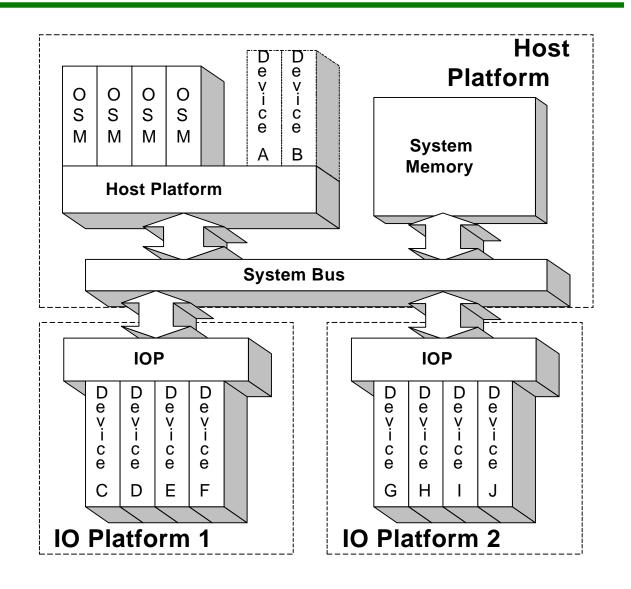
I₂O System Model - Physical View I₂O



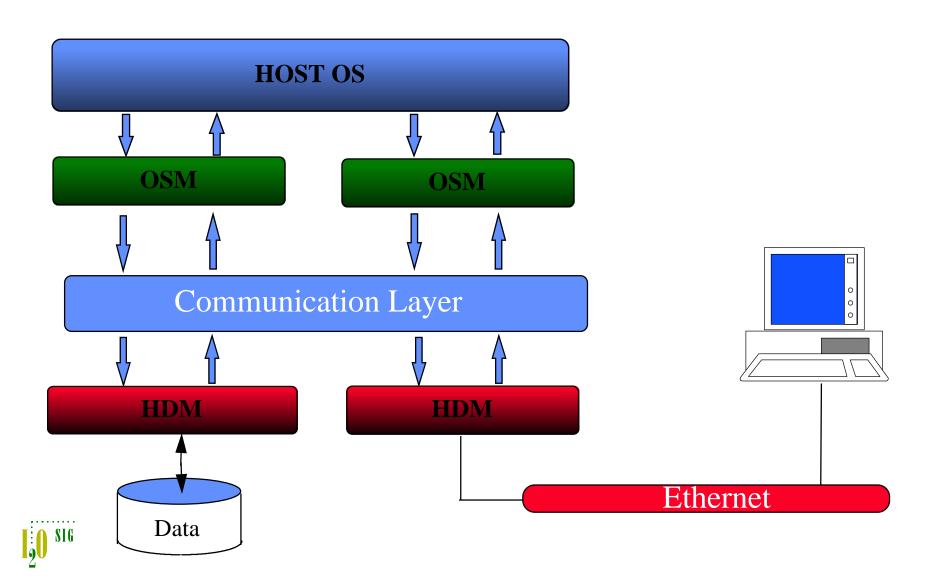


I₂O System Model - Logical View I₂O









I₂O Message Frame

I₂O

Two primary parts: fixed size header & variable-size payload.

Two basic categories: request messages & reply messages.

Message Header

Message Payload



Utility Messages

- common across all I/O classes
- provide basic level of functionality for negotiation & configuration

Base Messages

typically describe I/O requests or services requests

Private Messages

 allow for extensions to the base set of messages within an I/O class



- Executive Class Used to communicate between Messenger Instances
- Block Storage Abstraction of block storage device: hard disk drive, CD ROM, etc.
- LAN Abstraction of LAN port: ethernet, token ring, etc.
- SCSI Peripheral Abstraction of SCSI device
- SCSI Adapter exposes an interface to the host bus adapter



- Take Advantage of Industry Expertise
 - NOS Vendors
 - I/O Adapter Vendors
 - System Integration Vendors
- Develop the Specification
 - Create an Open Architecture
 - Validate with a Proof-of-Concept Platform
- Form a Special Interest Group





I₂O SIG Membership

 I_2O

Steering Committee

<u>Members</u>

Compaq

HP

Intel

Microsoft

NetFrame

Novell

Symbios Logic

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Contributing Members

Accelerate Technologies SMC

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AMI Tandem

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SCO Wind River Systems
Xpoint Technologies

I₂O SIG Information

(415) 750-8352 (*Phone*)

(415)751-4829 (Fax)

http://www.I2OSIG.org



Associate Members

Acer America

Annabooks

Cyclone Microsystems

Fore Systems

ICP Vortex

Siemens Nixdorf

- Multiple Levels of I₂O SIG Participation
 - Steering Committee (includes 3 elected members)
 - Contributing Member(1 company/1 vote)
 - Associate Member (no vote)
- Establish Working Committees *
 - Participation limited to Contributing Members
 - Multiple participation allowed
- Specify Compliance Requirements *



- Clustering/Fault Tolerance
- Peer-to-Peer
- Server Management
- Fibre Channel
- Certification
- ATM/WAN
- 64 Bit
- Storage/RAID
- Marketing/Public Relations
- IRTOS



- I₂O Architecture is a solution to I/O standardization and performance bottlenecks
- I₂O Architecture is not dependent on a single microprocessor or bus architecture
- I₂O Architecture defined by proven leaders from all segments of the server and I/O industry
- Membership of the I₂O SIG is growing to address new technologies

