HARNESS THE POWER OF PCI FOR NETWORK INNOVATION

Harness the Power of PCI for Network Innovation

The PCI (Peripheral Component Interconnect) bus offers many advantages to hubs, routers and other embedded systems that require a high-speed, low latency backplane. With data rates of one Gigabit per second and above, PCI gives hub and router designers the bandwidth previously provided only by proprietary architectures.

With PCI as a backplane, hubs and routers gain all the benefits of using a high-volume, PC-standard architecture: wide availability of low-cost network interface silicon, a proven standard architecture, and compatibility with other manufacturers' hardware.

PLX Technology, a member of the PCI Special Interest Group (SIG), now offers the PCI 9060 chip, which generates and controls the PCI bus in embedded systems such as hubs or routers. Combined with Intel's i960® 32-bit RISC processor family, the PCI 9060 provides a variety of price/performance options for equipment ranging from workgroup hubs to enterprise network products.

Network Equipment Architecture

Switching hubs, bridges and routers must transfer large amounts of data between segments. High data transfer rates and low latencies are critical requirements that, until now, only proprietary buses could provide. Standard personal computer buses such as ISA (AT), Micro Channel and EISA could not meet these requirements.

PCI and Network Equipment

PCI was designed specifically to improve bandwidth and latency in computer systems. Although PCI has been adopted initially by the manufacturers of personal computer, engineering workstation and mini-computer systems, the data transfer and latency benefits are attractive to a wide range of embedded applications, including hubs and routers. Current versions of the PCI bus support data transfer rates starting at 132 Megabytes (1056 Megabits) per second, upgradeable to 528 Megabytes (4224 Megabits) per second. In embedded systems, latencies are fully under the control of the system designer and can be a fraction of a microsecond compared to tens or hundreds of microseconds for previous standard PC buses. Furthermore, the infinite burst capability of PCI is well suited to I/O traffic.

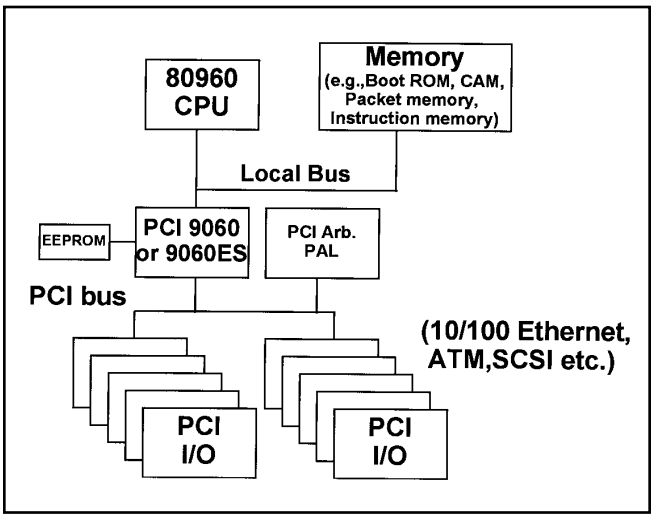
PCI Component Cost and Availability

Most suppliers of network interface controller chips (NICs), including Ethernet, 100 Megabit Ethernet and ATM (Asynchronous Transfer Mode), now offer, or intend to offer, a PCI interface for their components. Already there is wide availability of low-cost, high-performance PCI NIC chips.

PCI 9060 Connects PCI to the Leading Networking Processor

Until now, the main challenge of implementing a PCI bus in an embedded system has been the lack of PCI controller silicon. There is a wide selection of silicon for Intel486™ and Pentium™ processor-based systems, but none for the unique requirements of RISC processor-based embedded systems.

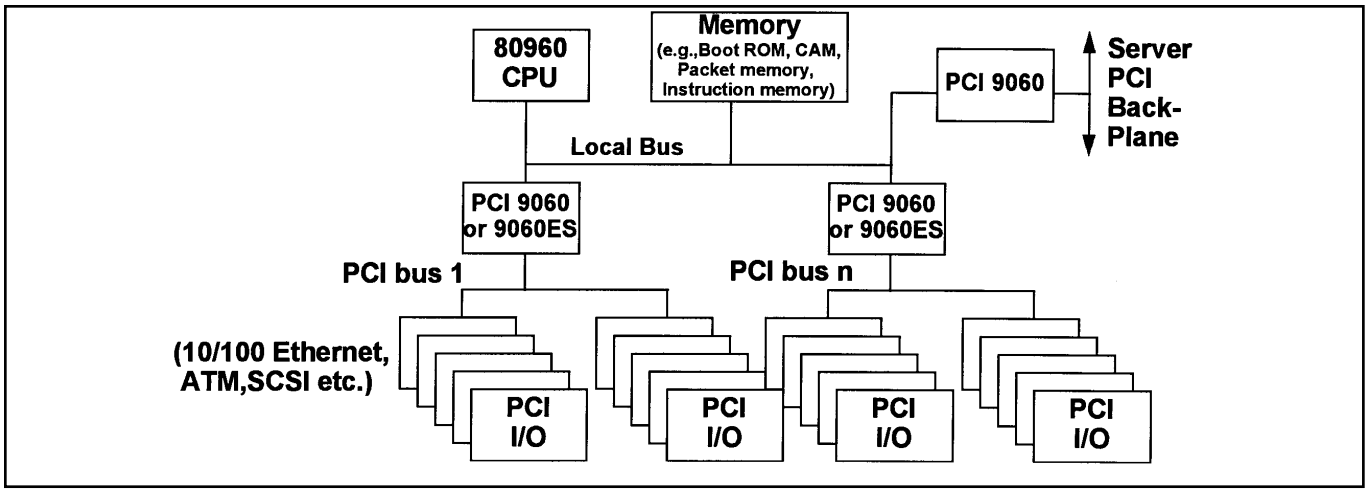
The PCI 9060, designed as an interface to Intel's i960 32-bit embedded processor architecture, contains the logic required to generate and control a PCI bus in an embedded system. Intel and PLX jointly defined the PCI 9060 to ensure the optimum feature set and compatibility with the expanding line of Intel i960 processors. The attached diagram illustrates a typical network equipment architecture.



Low cost switching hub design

– Glueless connection to i960 processor, including i960 Jx and Sx processors

– Glueless connection to high-performance PCI network controllers @ 33 MHz



High Performance Hub Design

– Glueless connection to superscalar i960 CF processor and future versions
– Supports multiple PCI buses
– Option to connect to server's PCI backplane

The PCI 9060 generates the PCI bus under control of the i960 processor. During initialization, the 9060 configures all the devices on the PCI bus from information in the boot FLASH or ROM. Configuration information includes the base address of the various NICs on the PCI bus, value of latency timers, and other critical data.

The 9060 supports four data transfer modes between the PCI bus and the local bus, where the i960 processor and packet memory reside. First the PCI NICs, acting as PCI masters, may perform a slave access to the local bus for high speed data transfer. FIFOs in the 9060 ensure zero-wait state burst transfers even if the local bus and PCI bus run at different speeds.

Conversely, a master on the local bus, such as the i960, may access a PCI NIC as a slave. This operation would typically be performed for configuration of the PCI NIC.

The PCI 9060 also contains a two-channel DMA. Programmed by the PCI 9060, the PLX chip performs high-speed data transfers between the PCI bus and packet memory.

The 9060 also contains mailbox and doorbell registers which are used to transmit command and pointer information between the PCI and the local bus.

Some hub and router designs do not require the PCI 9060's DMA controller. For these designs, PLX provides the lower cost PCI 9060ES, which is a software- and pin- compatible subset of the PCI 9060.

In summary, the PCI 9060and the i960 processor family provide a compact, high-speed platform to build PCI-based network equipment.

For more information about the PCI 9060 products, contact PLX Technology, 415-960-0448.

For more information about the Intel i960 microprocessor family, contact Intel Corporation, 1-800-628-2283 and request document number 2068.

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