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i960® MICROPROCESSOR COMPETITIVE BENCHMARK REPORT

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i960® COMPETITIVE BENCHMARK REPORT

Introduction

This report describes the results of performance benchmarks run on the Intel i960® microprocessors and several competitors in the 32-bit RISC field. The microprocessors covered in this report are:

- Intel 80960SA, 80960SB, 80960KA, 80960KB, 80960CA, 80960CF
- Integrated Device Technology (IDT) 3081, 3051, 3052,3041
- Advanced Micro Devices (AMD) 29205, 29200, 29030
- Motorola 68040

The basis of the comparison is a set of synthetic benchmark programs.This report makes every attempt to 1) use accepted practices in running the benchmarks and 2) provide full and unambiguous disclosure of all factors that significantly affect the results.

Why synthetic benchmarks? It is not our contention that the results of synthetic benchmark programs should be the sole factor in selecting a microprocessor. The best indicator of performance is a customer's own benchmark program or — in the absence of that — one resembling the actual application. Developing a benchmark, however, costs time and money and may not be feasible for all customers. The customer may not have an application program developed when considering microprocessor performance. These constraints cause developers to turn to synthetic benchmarks for an indication of microprocessor performance.

Benchmark data in this report is presented using simple bar charts. The following figure is an example of such bar charts; it shows the relative performance of the present line of i960 microprocessors.

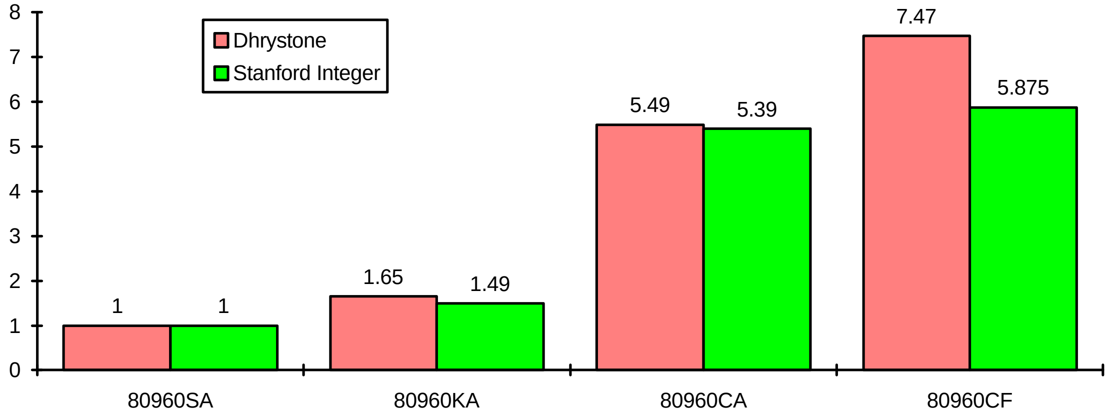

Figure 1. Relative Performance of i960® Microprocessors (not frequency normalized)

In charts comparing an 80960 against one or more competitors we have chosen to display the data as relative to the competitor. In the above chart the 80960CF, 80960CA and 80960KA are shown relative to the 80960SA. Data in these charts is normalized for processor clock frequency unless otherwise noted.

The raw results of each run are presented in tables at the end of this document. These tables contain all data obtained from the benchmarking process. The data in the tables was normalized for frequency and then used to generate the bar charts. The exception to this is the Whetstone test. The Whetstone results were not included in the floating point average. The magnitude of the 80960 Whetstone result may lead one to beleive that there is a mistake involved here. There is not. The high value is a result of the aggressive optimization that is possible on some types of program structure with the Intel CTOOLS960 compiler. We chose to leave the Whetstone result out of the floating point average to avoid skewing the graphical results. We chose to leave them in the result table because they were produced with procedures consistent with those set out for this exercise.

This document explores the tradeoffs between various choices of memory subsystem design. The following example shows the differences in performance between more aggressive, costly memory designs and simpler, less costly ones.

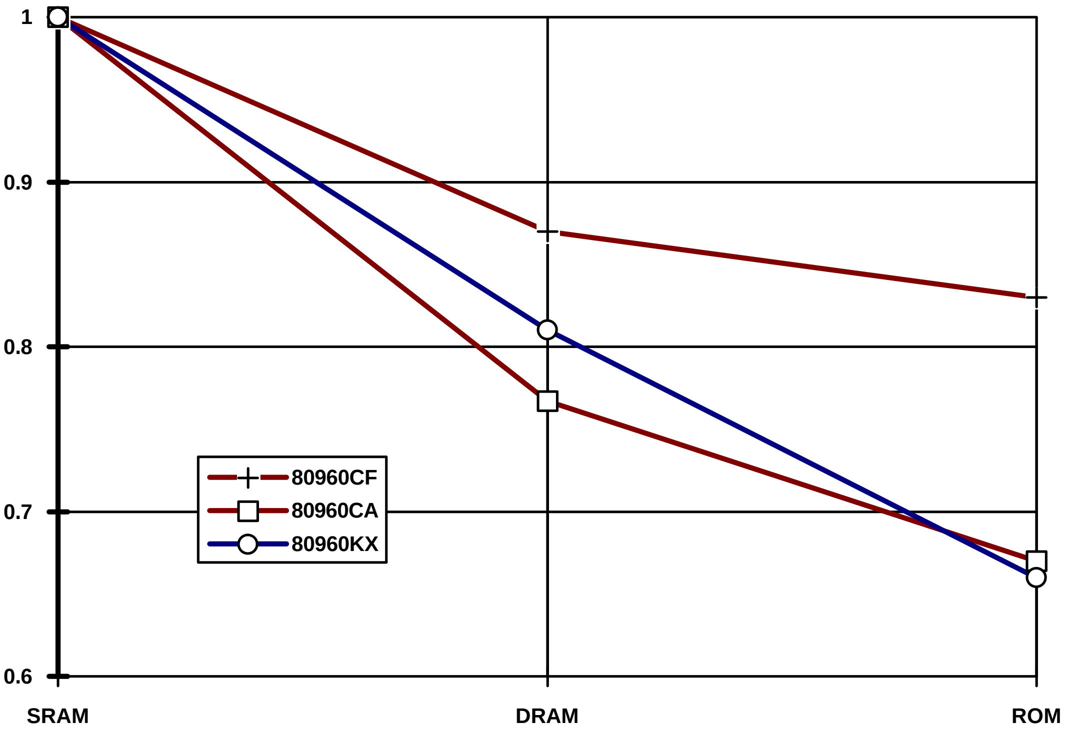

Figure 2. Comparison of High- and Low-Cost Memory Systems (KX and CX)

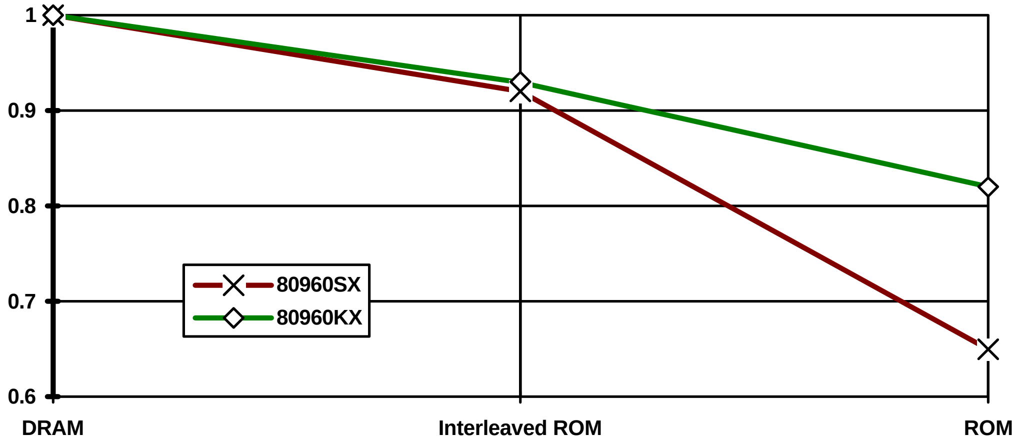

Figure 3. Comparison of high and low memory cost (KX and SX)

The graphs in figures 2 and 3 indicate the averaged results of the Stanford and Dhrystone integer test. Test results were averaged to avoid restricting the result to one type of program structure.

NOTE: the midpoint of the KX line in the second graph is extrapolated from the graph above it. We did not have a waitstate profile for the KX to match the corresponding SX setting.

Selection of programs used in this report was based on general acceptance, well-known behavior and the fact that each is written in the C programming language. Each makes an attempt at a relative measurement of the performance of the microprocessor/compiler combination. Selection was also influenced by the limitations imposed by some of the microprocessor evaluation boards used: some boards did not have adequate memory to support some of the desired programs.

The benchmark programs used include Dhrystone, Whetstone, Stanford integer and floating point sections and the Linpack floating point benchmark. Hardware evaluation platforms were used to generate the data for this report. None of the result data were obtained using software performance simulators.

Methodology

There are few choices in selection of memory technology when designing a microprocessor subsystem. DRAM is the predominant read/write memory technology. ROM, Flash, and EPROM are the predominant technologies for read-only (or read-mostly) memory subsystems. SRAM subsystems are expensive beyond practicality, as code and data size of applications continues to grow beyond the 1 Mbyte limit.

The system designer must work within the bounds of these available memory technologies. For example, if a system designer must use 80 ns DRAM technology, the relevant question of performance is — How fast can the microprocessor execute from 80 ns DRAM?

A 32-bit microprocessor memory subsystem typically resembles one of the three subsystems described in Table 1.

Table 1. Typical 32-Bit Microprocessor Memory Systems

Cost	Performance	Code Size	Description
high	**high**	**small to moderate**	Code and data are located in fast SRAM. SRAM provides access times on the order of 10 - 35 ns. Not a common design, but simple to implement. Practical for applications which have little code and are not cost-sensitive.
moderate	**moderate to high**	**moderate to large**	Code and data are located in DRAM. The code and initialized data are loaded from a backplane bus or inexpensive ROM at initialization. Mainstream, inexpensive DRAM technology typically provides 70 to 80 ns access time and fast page mode access capability. The system designer can trade off interface cost and performance using different degrees of complexity such as burst mode support and interleaving. Performance may also be enhanced in these systems with a small, fast SRAM memory dedicated to frequently accessed data.
low	**low to moderate**	**large**	Code is executed from ROM. Data is located in DRAM. The system designer can increase performance by interleaving the ROM subsystem. Since this design is driven by low cost, the DRAM subsystem is typically implemented at the lowest possible cost.

Microprocessor performance is influenced by several elements; categorized below as either *intrinsic* or *extrinsic*:

- *Intrinsic* elements generally are not or cannot be varied for performance analysis purposes. These properties are inherent to the microprocessor:
  - — Architecture and internal implementation (e.g. cache size, instruction set, registers)
  - — Efficiency of the external memory interface (e.g. instruction fetch bandwidth)
  - — Compiler efficiency (assuming that the best compiler is selected with the highest optimization turned on)
- *Extrinsic* elements can be varied depending on application requirements, performance and cost constraints:
  - — Clock speed
  - — Bus bandwidth (memory wait states)

Since many factors influence microprocessor performance, it is necessary to choose an equitable reference or baseline for a fair performance comparison. For this performance report, *memory technology* and clock speed have been chosen as the common reference for measuring performance of industry standard benchmarks.

We have chosen to equalize these key factors to make them common to all the comparison cases considered here.

- To equalize the clock rate factor, results of units with higher clock rates were scaled downward to reflect the lower clock rate. The highest rate in the group was the 33 MHz used on the Intel TomCAt board. The lowest was 16 MHz shared by the AMD29200, AMD29205 and the Intel EV80960SX boards.
- To equalize memory subsystem performance, the competitors' memory speed were considered on a case by case basis and the wait state profile of the corresponding Intel board was adjusted to emulate memory devices of equal speed.

Each processor's external bus interface is different; consequently, the logic used to implement the DRAM interface for each processor is also different. The relative complexity of the support logic required to implement a particular DRAM interface is significant to the system designer for consideration of system cost and engineering resources required for design and validation.

The competitors' evaluation hardware are designed with DRAM. The memory wait state profiles for this hardware cannot be altered, but are optimized for a particular subsystem complexity as follows:

- DRAM: 80 ns non-interleaved
- DRAM: 80 ns interleaved, CAS interleaving for reads only, no write posting
- DRAM: 80 ns interleaved, CAS and RAS interleaving

Benchmark Programs

Table 2. Benchmark Program Descriptions

Program	Description	Units of Measure
Dhrystone	Tests integer performance. String manipulation is a common action in this program. The version used here is 2.1.	Dhrystones/Second
Whetstone	Tests floating point performance.	Millions of Whetstones/Second
Stanford	Contains both integer and floating point sections. Uses a suite of well-known problems such as the towers of Hanoi and sorting algorithms.	Stanford integer composite; Stanford floating point composite (Smaller is better)
Linpack	Measures floating point performance using matrix manipulation.	Thousands of FLOPS/Second

Benchmark Environment

Development Software/Workstation

All test code was generated in a cross-development environment. None of the test programs were compiled on the machine on which they ran. Program generation was done on two machines.

All test programs for non-Intel targets were compiled on a Dell 450DE, 80486 machine running at 50 MHz. All software tools for the AMD, IDT and Motorola microprocessors are DOS based. Compile times were not documented; this was not the goal of this report. Care was taken to ensure that the compilers used were the latest revision.

Intel software tools used in this report are UNIX based. The 80960 applications department's benchmarking environment includes an 80386-based UNIX System V machine with several 80960 boards attached.

The manufacturers and versions of software development tools are as shown in Table 3.

Table 3. Software Development Tools

Manufacturer	Tool Name	Version	Target
Metaware	High C 29K	3.1	AMD 29030, 29200, 29205
Microtec Research Inc.	MCC68K	4.2I	Motorola EC68040
Integrated Device Technology	IDT/c	4.1	3051,3052,3081,3051
Intel	CTOOLS960	X4.0.324	80960SA, SB, KA, KB, CA, CF

All compilers used offer various levels of optimization. Runs were conducted at each of two optimization levels - default and maximum - to demonstrate the improvements offered by each tool's optimization efforts. All charts are based upon maximally optimized code. Maximum optimization is based on the recommendation of the compiler literature.

Target Hardware

Table 4 shows the hardware configurations and memory used to conduct these benchmarks.

Table 4. Hardware Configuration and Memory

CPU / Eval Board	Clocking	Memory Speed	Memory Description
Intel 80960SA/SB EV80960SX (Standalone, serial connect to host)	16 MHz (CPU); 16MHz (Bus)	100ns paged DRAM	2-way interleaved DRAM, CAS and RAS interleaving for reads only - no write posting Variable through the use of an added PC board. See comparative sections for a description of profiles.
Intel 80960 KA/KB QT960 (Standalone, serial connect to host)	20 MHz (CPU) 20 MHz (Bus)	15 ns SRAM	Programmatic control of wait state timing. Three profiles were used.See comparative sections for a description of profiles.
Intel 80960CA/CF TomCAt (Standalone, serial connect to host)	33 MHz (CPU) 33 MHz (Bus)	15 ns page SRAM	Programatic control of waitstate timing. Four profiles were used. See comparative sections for a description of profiles.
AMD 29030 EB29030 (ISA bus devel. card)	25 MHz (CPU) 25 MHz (Bus)	80 ns paged DRAM	2-way interleaved DRAM, CAS and RAS interleaving for reads only - no write posting Read cycle - A 3 2 1 D 1 D D D Write cycle - A 3 2 1 D 1 D 1 D 1
AMD 29200: SA29200 (Standalone, serial connect to host)	16 MHz (CPU) 16 MHz (Bus)	80ns paged DRAM	2-way interleaved DRAM, CAS and RAS interleaving for reads only - no write posting Read cycle - A 2 1 D D D D 1 A Write cycle - A 2 1 D 1 D 1 D 1 D 1 A
AMD 29205: SA29205 (Standalone, serial connect to host)	16 MHz (CPU) 16 MHz (Bus)	80ns paged DRAM	2-way interleaved DRAM, CAS and RAS interleaving for reads only - no write posting Read cycle - A 2 1 D D D D 1 A Write cycle - A 2 1 D 1 D 1 D 1 D 1 A
IDT 3081E, R30051E, R3041* R3052E: 7RS385 (Standalone, serial connect to host)	25 MHz (CPU) 25 MHz (Bus) * 3041 was run at 20MHz	80ns paged DRAM	2-way interleaved DRAM, CAS and RAS interleaving for reads only - no write posting Read cycle - A 2 1 D D D D 1 A Write cycle - A 2 1 D 1 D 1 D 1 D 1 A
Motorola EC68040 MVME167 (VME bus card)	25 MHz (CPU) 25MHz (Bus)	70ns paged DRAM	2-way interleaved DRAM, CAS and RAS interleaving for reads only - no write posting Read cycle - A 2 1 D D D D 1 A Write cycle - A 2 1 D 1 D 1 D 1 D 1 A

Platform Specifics

Memory Interface Configurations

As described above, the Intel boards used in this report were configured to simulate designs that use memory devices of particular performance. Tables 5, 6 and 7 list the configurations used, described by their bus cycles.

Table 5. TomCAt (80960CF/CA) Memory Interface Configuration

SRAM	Read Cycle A D D D D A Write Cycle A D D D D A
DRAM	Read Cycle A 2 1 D D D D 1 A Write Cycle A 2 1 D 1 D 1 D 1 D 1 A
ROM	Read Cycle A 3 2 1 D 3 2 1 D 3 2 1 D 3 2 1 D A Write Cycle A 3 2 1 D 3 2 1 D 3 2 1 D 3 2 1 D A

Table 6. QT960 (80960KA/KB) Memory Interface Configuration

SRAM	Read Cycle A D D D D 1 A Write Cycle A D D D D 1 A
DRAM	Read Cycle A 2 1 D 1 D 1 D 1 D 1 A Write Cycle A 2 1 D 1 D 1 D 1 D 1 A
ROM	Read Cycle A 3 2 1 D 3 2 1 D 3 2 1 D 3 2 1 D 1 A Write Cycle A 3 2 1 D 3 2 1 D 3 2 1 D 3 2 1 D 1 A

Table 7. EVSX (80960SA/SB) Memory Interface Configuration

SRAM	N/A
DRAM	Read Cycle A 1 D D D D D D D D 1 A Write Cycle A 1 D D D D D D D D 1 A
ROM	Read Cycle A 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 1 A Write Cycle A 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 2 1 D 1 A

Hardware Modifications

The EV80960SX board required the addition of a small PC board containing a PAL and a DIP switch to implement waitstate configurability. This was the only hardware modification performed during this exercise.

Relative Performance of the 80960 Family (not frequency normalized)

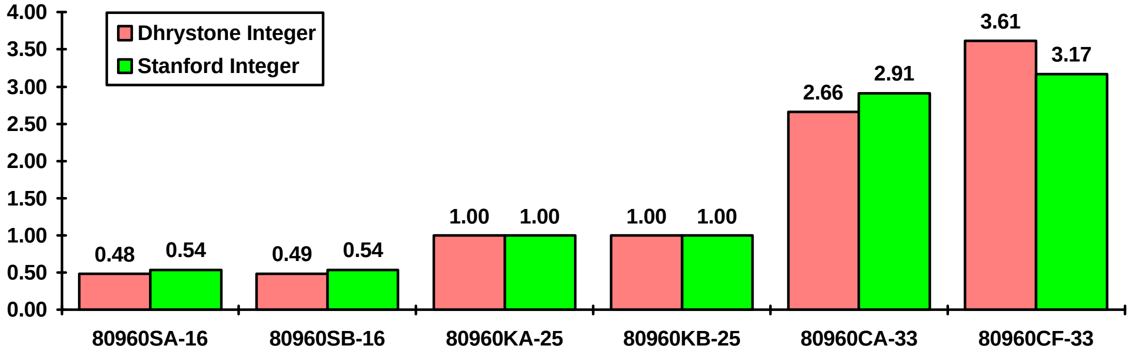

Figure 4. Intel i960 CPU Relative Integer Performance (relative to 80960KA)

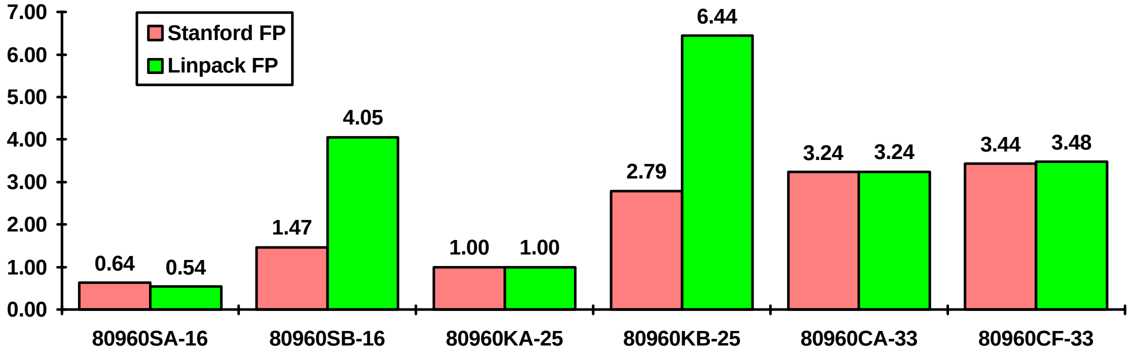

Figure 5. Intel i960 CPU Relative Floating Point Performance (relative to 80960KA)

Intel 80960 Sx vs. AMD 29200/29205

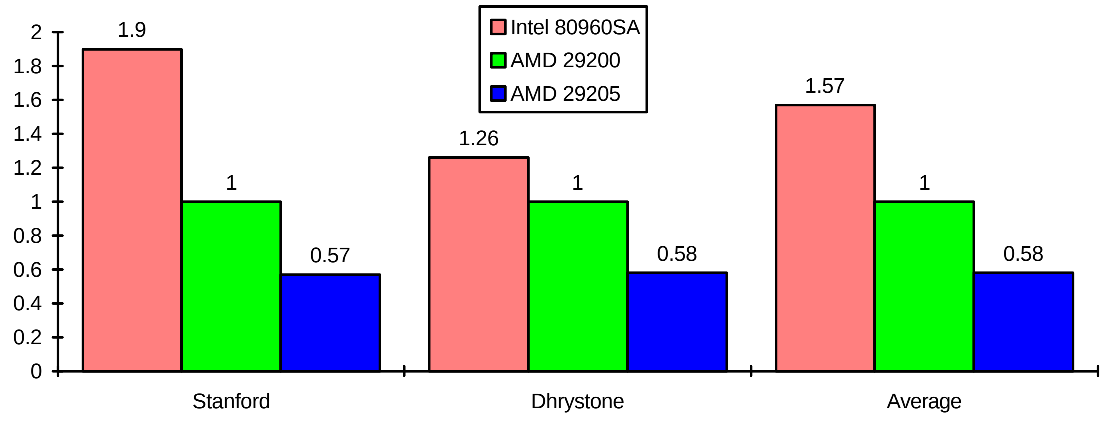

Figure 6. 80960 SX vs. AMD292xx Integer Tests

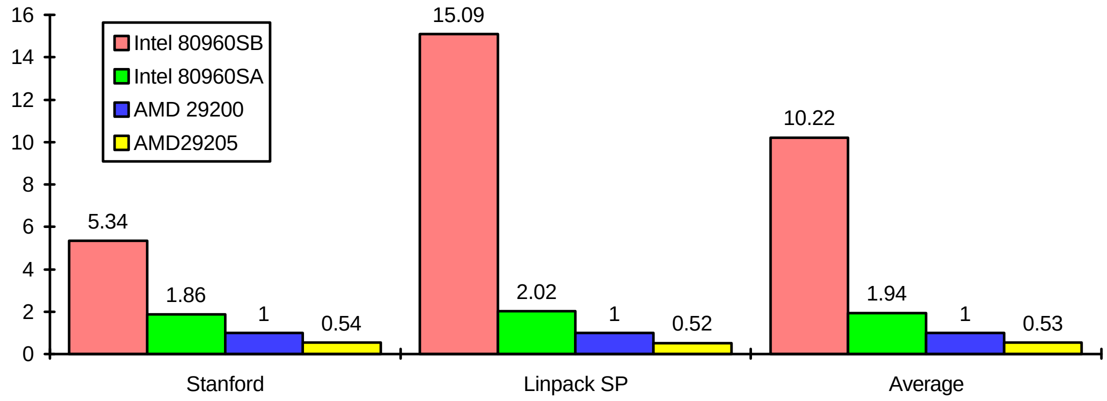

Figure 7. 80960 SX vs. AMD292xx Floating Point Tests

These tests were conducted with the Intel EVSX board in its DRAM configuration. It should be noted that the AMD evaluation boards used in this test arrived in a configuration that utilized floating point trap handlers located in ROM. This had the effect of making the 29205 appear faster than the 29200 on floating point tests. This is because the 16 bit SA29205 has 16 bit wide ROM while the 32 bit SA29200 has 8 bit wide ROM. Also included with the boards was a floating point trap library and some initialization code to change the trap vectors to point to DRAM. This initialization code was not located in the timed part of any test program.

The 80960SA, AMD29200 and AMD29205 utilize floating point emulation software while the 80960SB utilizes hardware dedicated to floating point operations.

Intel 80960 CA vs. AMD 29030

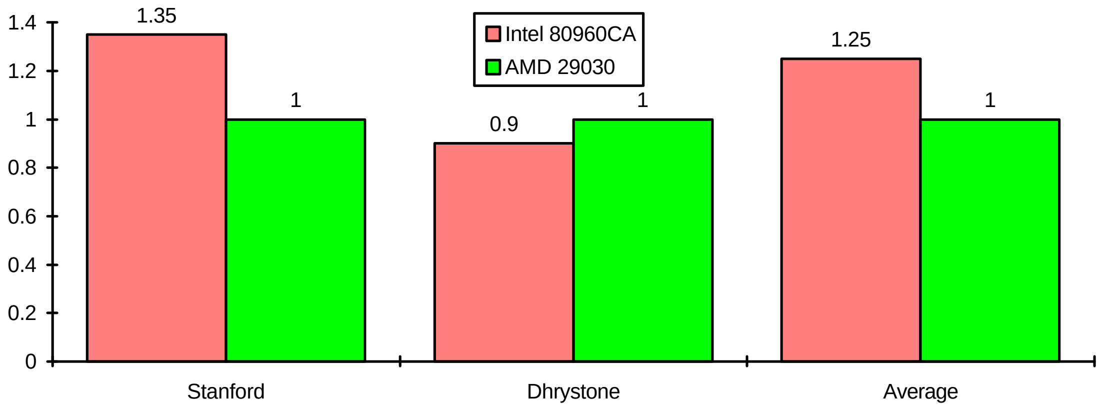

Figure 8. 80960 CA vs AMD 29030 Integer Tests

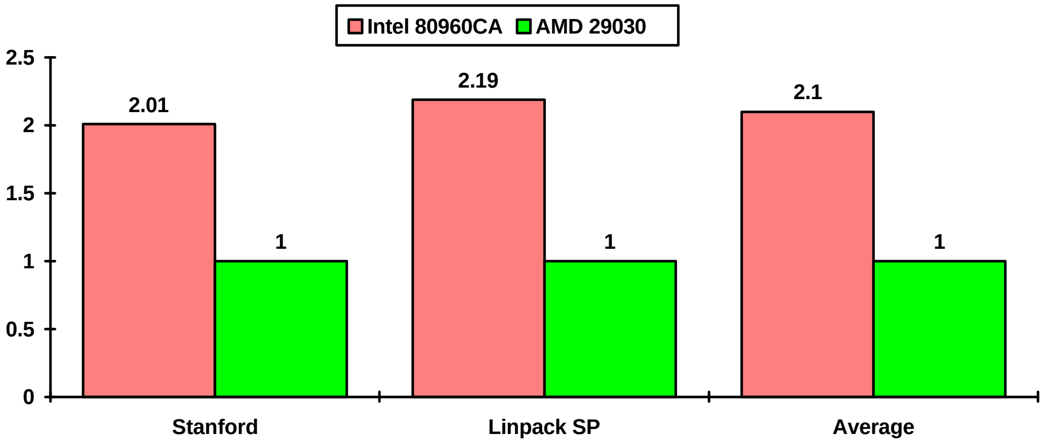

Figure 9. 80960 CA vs AMD 29030 Floating Point Tests

These tests were conducted with the Intel TomCAt board in its DRAM configuration.

Intel 80960 CF vs. IDT R3081E

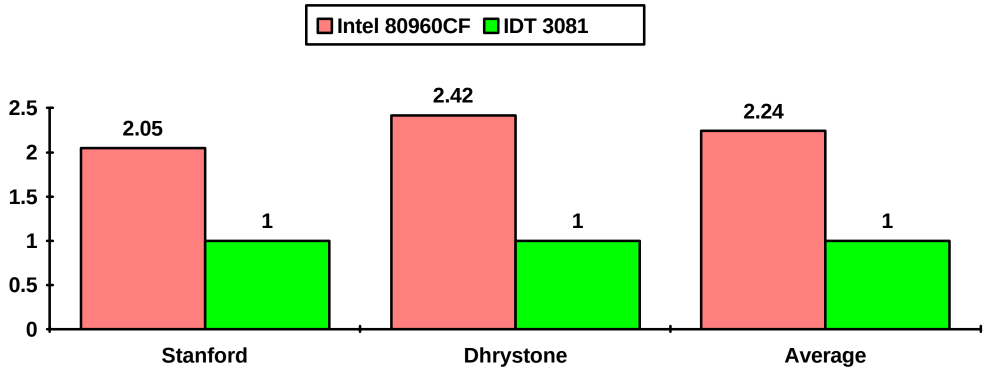

Figure 10. 80960CF vs IDT R3081E Integer Tests

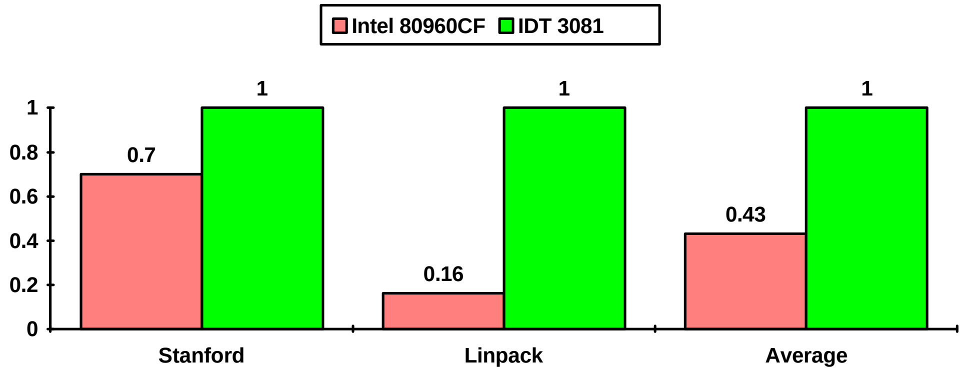

Figure 11. 80960CF vs IDT R3081E Floating Point Tests

These tests were conducted with the Intel TomCAt board in its DRAM configuration. The 80960CF utilizes floating point emulation software while the IDT 3081 utilizes hardware dedicated to floating point operations.

Intel 80960CA vs. IDT R3051E, R3052E

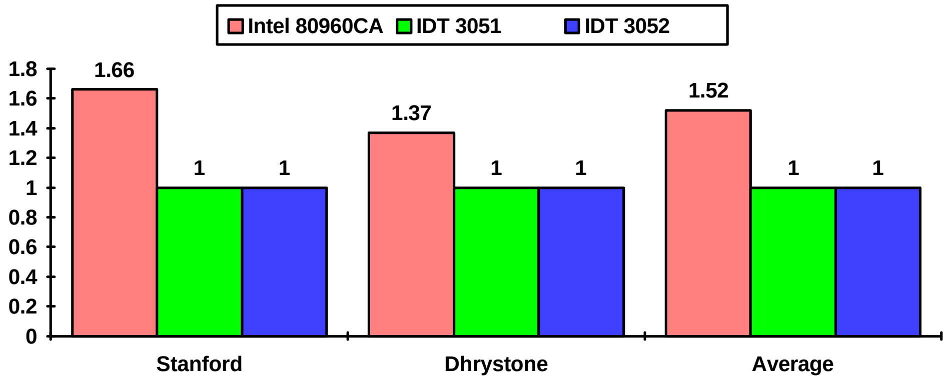

Figure 12. 80960CA vs IDT R3051, R3052 Integer Tests

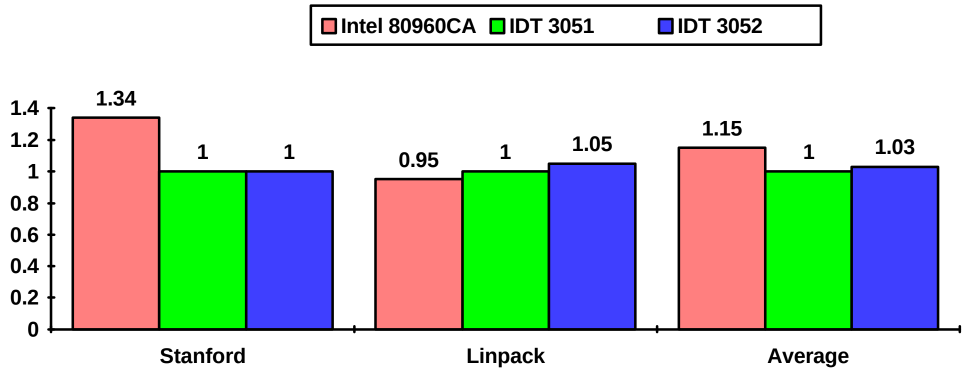

Figure 13. 80960CA vs IDT R3051, R3052 Floating Point Tests

These tests were conducted with the Intel TomCAt board in its DRAM configuration.

Intel 80960 SX vs. IDT R3041

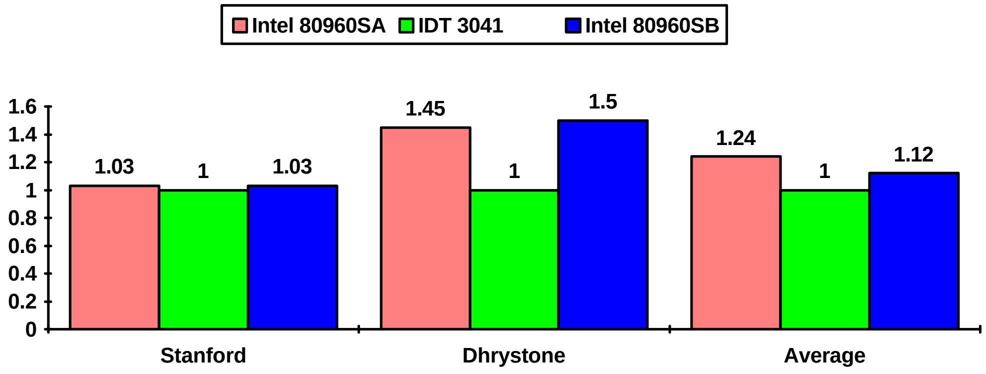

Figure 10. 80960SX vs IDT R3041 Integer Tests

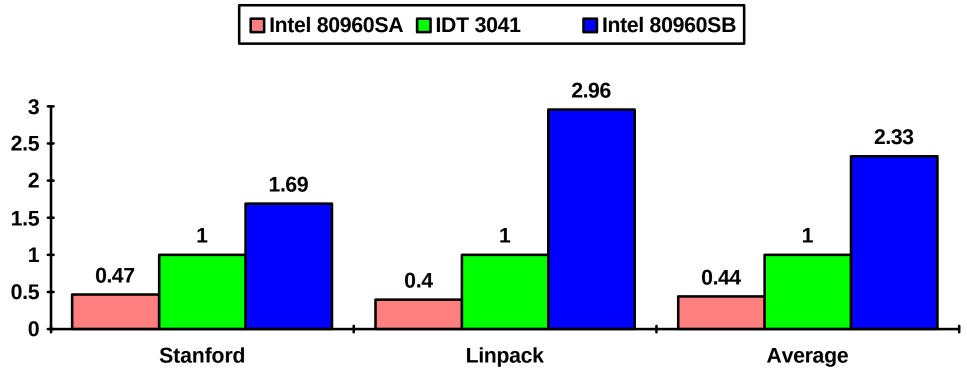

Figure 11. 80960SX vs IDT R3041 Floating Point Tests

Intel i960 CF vs. Motorola 68040

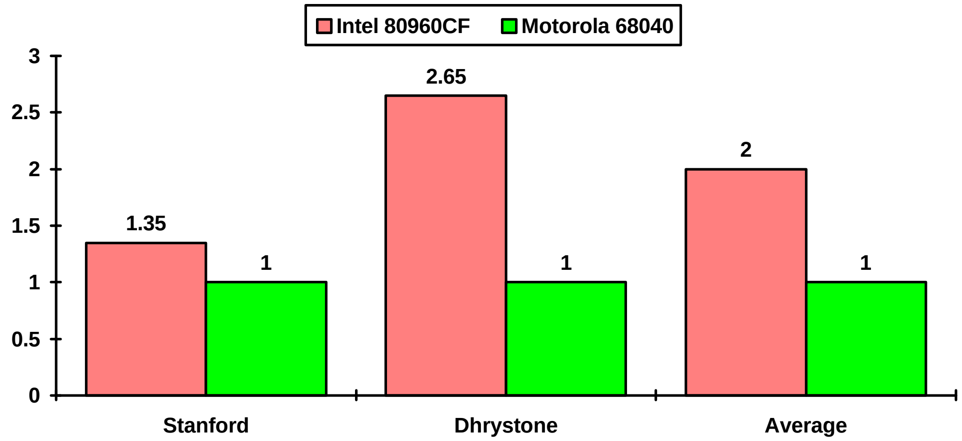

Figure 14. 80960CF vs Motorola 68040 Integer Tests

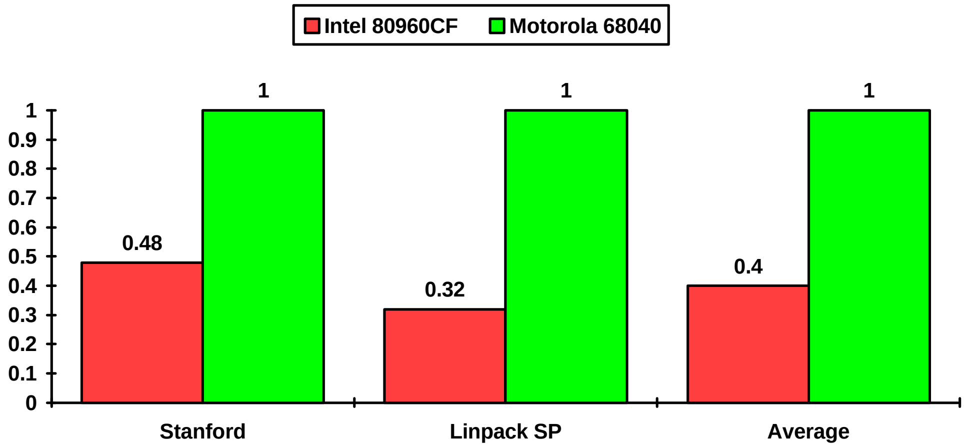

Figure 15. 80960CF vs Motorola 68040 Floating Point Tests

These tests were conducted with the Intel TomCAt board in its DRAM configuration. The 80960CF utilizes floating point emulation software while the Motorola 68040 utilizes hardware dedicated to floating point operations.

Benchmark Result Tables

Table 8. Intel 80960SA Default Optimization

	DRAM	ROM
Dhrystone	6959	3584
Whetstone - Single Pr.	.58	.36
Whetstone - Double Pr.	.50	.30
Stanford Suite - Integer	494	640
Stanford Suite - FP	1992	3059
Linpack - Single Pr.	89	57

Table 9. Intel 80960SA Maximum Optimization

	DRAM	ROM
Dhrystone	12145	6695
Whetstone - Single Pr.	3.97	2.59
Whetstone - Double Pr.	2.28	1.50
Stanford Suite - Integer	329	442
Stanford Suite - FP	1646	2506
Linpack - Single Pr.	89	59

Table10. Intel 80960SB Default Optimization

	DRAM	ROM
Dhrystone	6886	3590
Whetstone - Single Pr.	2.40	2.14
Whetstone - Double Pr.	2.24	1.93
Stanford Suite - Integer	492	631
Stanford Suite - FP	828	1018
Linpack - Single Pr.	499	439

Table11. Intel 80960SB Maximum Optimization

	DRAM	ROM
Dhrystone	12269	6858
Whetstone - Single Pr.	5.57	4.99
Whetstone - Double Pr.	4.13	3.56
Stanford Suite - Integer	330	448
Stanford Suite - FP	573	746
Linpack - Single Pr.	664	596

Table 12. Intel 80960KA Default Optimization

	SRAM	DRAM	ROM
Dhrystone	11800	8745	6164
Whetstone - Single Pr.	.83	.69	.53
Whetstone - Double Pr.	.75	.63	.48
Stanford Suite - Integer	345	392	433
Stanford Suite - FP	1333	1556	1911
Linpack - Single Pr.	124	108	86

Table 13. Intel 80960KA Maximum Optimization

	SRAM	DRAM	ROM
Dhrystone	19740	14727	10836
Whetstone - Single Pr.	5.81	5.17	4.28
Whetstone - Double Pr.	3.18	2.83	2.30
Stanford Suite - Integer	222	256	289
Stanford Suite - FP	1052	1252	1567
Linpack - Single Pr.	131	116	95

Table 14. Intel 80960KB Default Optimization

	SRAM	DRAM	ROM
Dhrystone	11800	8667	6114
Whetstone - Single Pr.	3.18	3.01	2.88
Whetstone - Double Pr.	2.98	2.82	2.65
Stanford Suite - Integer	345	394	435
Stanford Suite - FP	602	661	712
Linpack - Single Pr.	648	626	593

Table 15. Intel 80960KB Maximum Optimization

	SRAM	DRAM	ROM
Dhrystone	19840	14847	10890
Whetstone - Single Pr.	7.26	7.04	6.81
Whetstone - Double Pr.	5.45	5.21	4.89
Stanford Suite - Integer	222	258	292
Stanford Suite - FP	377	418	460
Linpack - Single Pr.	844	833	800

Note: There are small differences (≤ 1%) between the integer results of the 80960SA/SB and 80960KA/KB. The differences are do to the inclusion of a small amount of floating point code in the non-timed areas of both the Dhrystone and Stanford integer tests. This affects the manner in which code flows through the 512 byte caches of the 80960KA/KB and the 80960SA/SB.

Table 16. Intel 80960CA Default Optimization

	SRAM	DRAM	ROM
Dhrystone	30283	19673	11362
Whetstone - Single Pr.	3.15	2.53	1.65
Whetstone - Double Pr.	2.95	2.39	1.54
Stanford Suite - Integer	101	131	144
Stanford Suite - FP	353	412	470
Linpack - Single Pr.	508	473	423

Table 17. Intel 80960CA Maximum Optimization

	SRAM	DRAM	ROM
Dhrystone	65562	43441	31360
Whetstone - Single Pr.	22.38	20.60	16.24
Whetstone - Double Pr.	12.83	11.05	7.39
Stanford Suite - Integer	61	82	94
Stanford Suite - FP	260	304	356
Linpack - Single Pr.	531	486	405

Table 18. Intel 80960CF Default Optimization

	SRAM	DRAM	ROM
Dhrystone	46253	39773	31773
Whetstone - Single Pr.	4.00	3.94	3.72
Whetstone - Double Pr.	3.58	3.51	3.28
Stanford Suite - Integer	89	96	99
Stanford Suite - FP	332	344	353
Linpack - Single Pr.	520	520	518

Table 19. Intel 80960CF Maximum Optimization

	SRAM	DRAM	ROM
Dhrystone	89146	77072	72333
Whetstone - Single Pr.	24.09	24.08	24.06
Whetstone - Double Pr.	14.18	13.72	12.09
Stanford Suite - Integer	56	64	67
Stanford Suite - FP	245	260	268
Linpack - Single Pr.	570	567	565

Table 20. AMD Results

AMD 29000 Series[1]	29030	29200	29205
Dhrystone	34976/36488	8939/9604	5176/5572
Whetstone - Single Pr.	1.06/1.06	.27/.27	.14/.14
Whetstone - Double Pr.	.75/.75	.18/.18	.10/.10
Stanford Suite - Integer	153/148	642/628	1129/1097
Stanford Suite - FP	919/833	3467/3058	6385/5629
Linpack - Single Pr.	168/168	44/44	23/23

Table 21. IDT Results

IDT R3000 Series[1]	3081E	3051E	3041	3052E
Dhrystone	23574/24096	23574/24096	10326/10458	23574/24096
Whetstone - Single Pr.	5.26/5.26	1.41/1.41	0.93/0.93	1.51/1.51
Whetstone - Double Pr.	5.24/5.24	1.25/1.25	0.88/0.88	1.38/1.38
Stanford Suite - Integer	179/173	186/182	277/272	186/182
Stanford Suite - FP	248/240	493/536	845/775	492/535
Linpack - Single Pr.	2656/2656	389/389	280/280	407/407

Table 22. Motorola Results

EC68040[1]	
Dhrystone	17663/22059
Whetstone - Single Pr.	4.45/6.95
Whetstone - Double Pr.	4.45/6.77
Stanford Suite - Integer	186/114
Stanford Suite - FP	313/164
Linpack - Single Pr.	1302/1353

[1] In all table cells, the first number is the result of Default optimization; the second is the result of Maximum optimization.