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TECHNICAL PAPER

Interfacing the Byte-Wide SmartVoltage FlashFile™ Memory Family to the Intel486™ Microprocessor Family

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CONTENTS

REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

This technical paper describes the designs for interfacing Intel's byte-wide SmartVoltage FlashFile™ memory family to different processors in the Intel486™ microprocessor family. The techniques discussed in the following sections focus on interfacing the 28F008SC to the Intel486 processor family; however, these can be applied to other members of the byte-wide SmartVoltage FlashFile memory family as well. For the designs described below, any control logic as well as processor bus cycles have been simulated, but they have **not** been lab tested.

The 4-, 8-, and 16-Mbit byte-wide SmartVoltage FlashFile memories provide high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. For secure code storage applications where code is either directly executed out of flash or downloaded to RAM, these memories offer three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. Code and data storage applications are facilitated well by their enhanced suspend capabilities. The SmartVoltage technology allows a choice in V_{CC} and V_{PP} combinations to meet system performance and power expectations. Furthermore, their power management aids in power-sensitive applications.

The read and write operations of the these devices are controlled by three distinct signals—CE#, OE#, and WE#. The power-down and reset operations are controlled by one signal—RP#. These pins are described in Table 1.

2.0 INTEL486™ MICROPROCESSOR INTERFACE AT 33 MHZ

The Intel486™ microprocessor is a 32-bit processor with a 30-bit address bus and a 32-bit data bus. The interface discussed in this paper can be applied to the following 3.3V V_{CC} Intel486 family members: 25- and 33 MHz SX, 33 MHz DX, 40 MHz DX2 (20 MHz Max.), 50 MHz DX2 (25 MHz Max.), 40 MHz Write-Back Enhanced DX2 (20 MHz Max.), 50 MHz Write-Back Enhanced DX2 (25 MHz Max.), 75/25 MHz DX4 and 100/33 MHz DX4. The design is also valid for the following 5V V_{CC} Intel486 family members: 25- and 33-MHz SX, 33 MHz DX, 50 MHz SX2 (25 MHz Max.), 50 MHz DX2 (25 MHz Max.), 66 MHz DX2 (33 MHz Max.), 50 MHz Write-Back Enhanced DX2 (25 MHz Max.), and 66 MHz Write-Back Enhanced DX2 (33 MHz Max.).

Please refer to the Intel World Wide Web site, BBS, or your Intel or local distribution sales office to obtain the schematics, timing analysis files, and logic files for the interfaces documented in this paper.

The timing specifications used in these designs were taken from the datasheets listed in Appendix A. The Appendix contains the names and order numbers of the datasheets used. The byte-wide FlashFile memory datasheets used were revision -001. The Intel486™ Processor Family datasheet used was revision -003.

Please contact your Intel or local distribution sales office for up-to-date specifications before finalizing any design.

Table 1. Byte-Wide SmartVoltage FlashFile™ Memory Pin Descriptions

Sym	Type	Name and Function
CE#	I	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
OE#	I	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	I	**WRITE ENABLE:** Controls writes to the Command User Interface (CUI) and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
RP#	I	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode.

2.1 Processor Interface Signals

System logic uses the signals described in Table 2 in interfacing the 28F008SC to the Intel486 microprocessor.

2.2 Interface Considerations

The discussion below considers the interfacing of a 5V V_{CC} Intel486 processor operating at 33 MHz to 28F008SC-85s.

This design (shown in Figure 1) uses four 28F008SC-85s to match the 32-bit data bus of the Intel486 processor, providing 4 Mbytes of flash memory. Address bits A_{21}–A_2 select locations within the 28F008SC-85 memory space.

CLK Option

A 33 MHz clock signal drives the Intel486 microprocessor CLK input and the PLD.

Reset

An active-low reset signal, RESET#, drives the RESET# inputs of the Intel486 processor and PLD as well as the RP# input of the 28F008SC-85s.

Control Signal Generation

Combinational logic using the upper ten bits of the address and the byte enable signals generates the CE# control signals for the 28F008SC-85s as well as the CS# input for the state machine. The upper ten bits are used to determine if the bus cycle is directed to the flash's memory space. This logic is a ten-input OR gate, and the address range depicted in the schematic is 00000000h–003FFFFFh. If the memory range desired for the flash memory is 80000000h–803FFFFFh, the A_{31} input to the OR gate is inverted. The processor's ADS# and W/R# also serve as inputs to the state machine. The state machine generates the OE# and WE# signals for the 28F008SC-85s. The state machine also generates the RDY# signal to the Intel486 processor to control wait-state generation. When powered-up, the state machine will transition to state S0 within one clock cycle since the address decode logic will be driving the CS# signal high, and the state machine equations are written in such a way that if this signal is sampled high in the middle of a read or write cycle, the state machine immediately returns to state S0.

Table 2. Intel486™ Microprocessor Pin Descriptions

Sym	Type	Name and Function
A_{31}–A_2	I/O	**ADDRESS LINES:** 30-bit address bus
BE0–-3#	O	**BYTE ENABLES:** Signals which indicate active bytes during read and write cycles.
D_{31}–D_0	I/O	**DATA LINES:** 32-bit data bus.
W/R#	O	**WRITE/READ:** Identifies the transfer as a read (0) or write (1).
ADS#	O	**ADDRESS STROBE:** Indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus.
RDY#	I	**NON-BURST READY:** Indicates the current bus cycle is complete.
CLK	I	**CLOCK:** Clock input used to derive all bus signal timings.

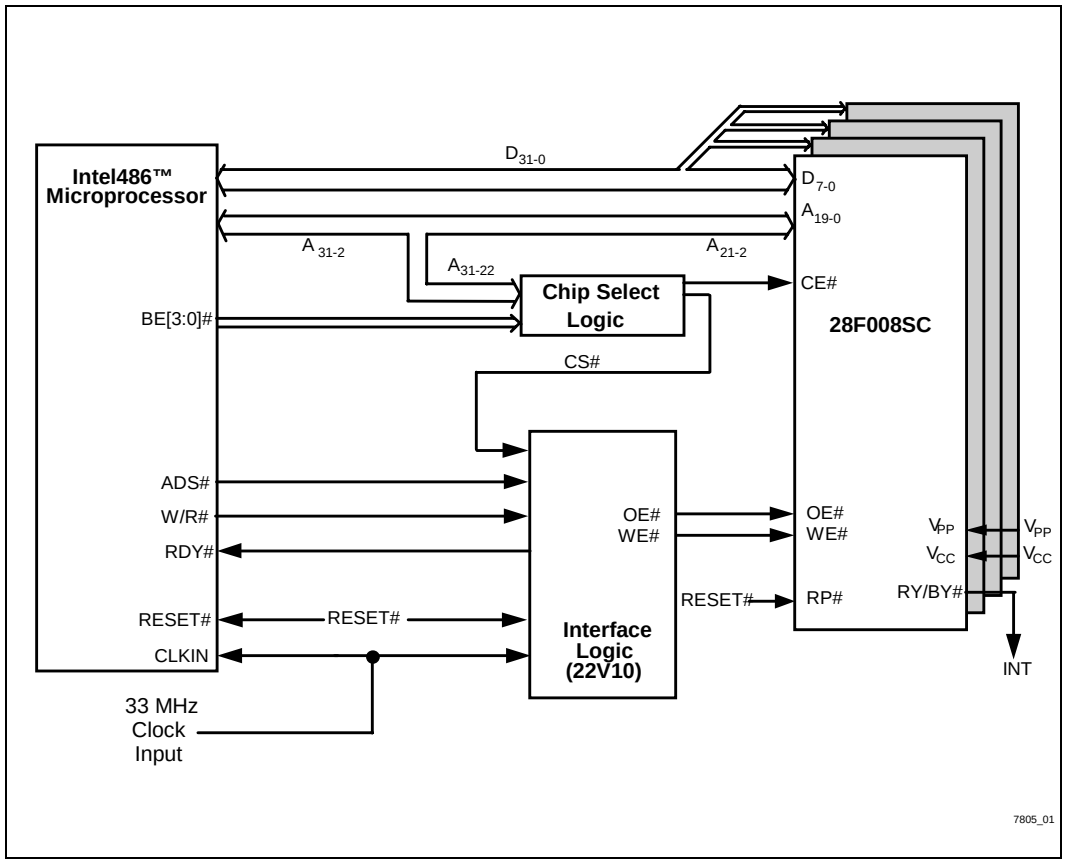

Figure 1. 28F008SC Interface to the Intel486™ Microprocessor

2.3 Read/Write Cycle Descriptions

Read Cycle

Refer to the state diagram (Figure 2) and read cycle timing diagram (Figure 3) for the following discussion of the read cycle.

When the Intel486 processor initiates a read cycle by asserting ADS#, the state machine enters an anticipation state. At the end of the T2 cycle, if CS# is asserted with W/R# = "0," the state machine asserts OE# to enable the 28F008SC-85s data output buffers. The OE# signal remains asserted and the RDY# signal is asserted after the T3 cycle to inform the processor that valid data is on the bus. At the end of cycle T4, the processor reads the data presented, and the state machine deasserts both OE# and RDY# as it returns to its idle state to wait for the next bus cycle.

Write Cycle

Refer to the state diagram (Figure 2) and the write cycle timing diagram (Figure 4) for the following discussion of the write cycle.

When the Intel486 processor initiates a write cycle by asserting ADS#, the state machine enters an anticipation state. At the end of the T2 cycle, if CS# is asserted with W/R# = "1," the state machine asserts WE#. After cycle T4, WE# is deasserted to latch the address and data to write, and the state machine asserts RDY# ending the bus cycle at the next clock edge. The RDY# signal is deasserted at the end of the T5 cycle as the state machine returns to its idle state to wait for the next bus cycle.

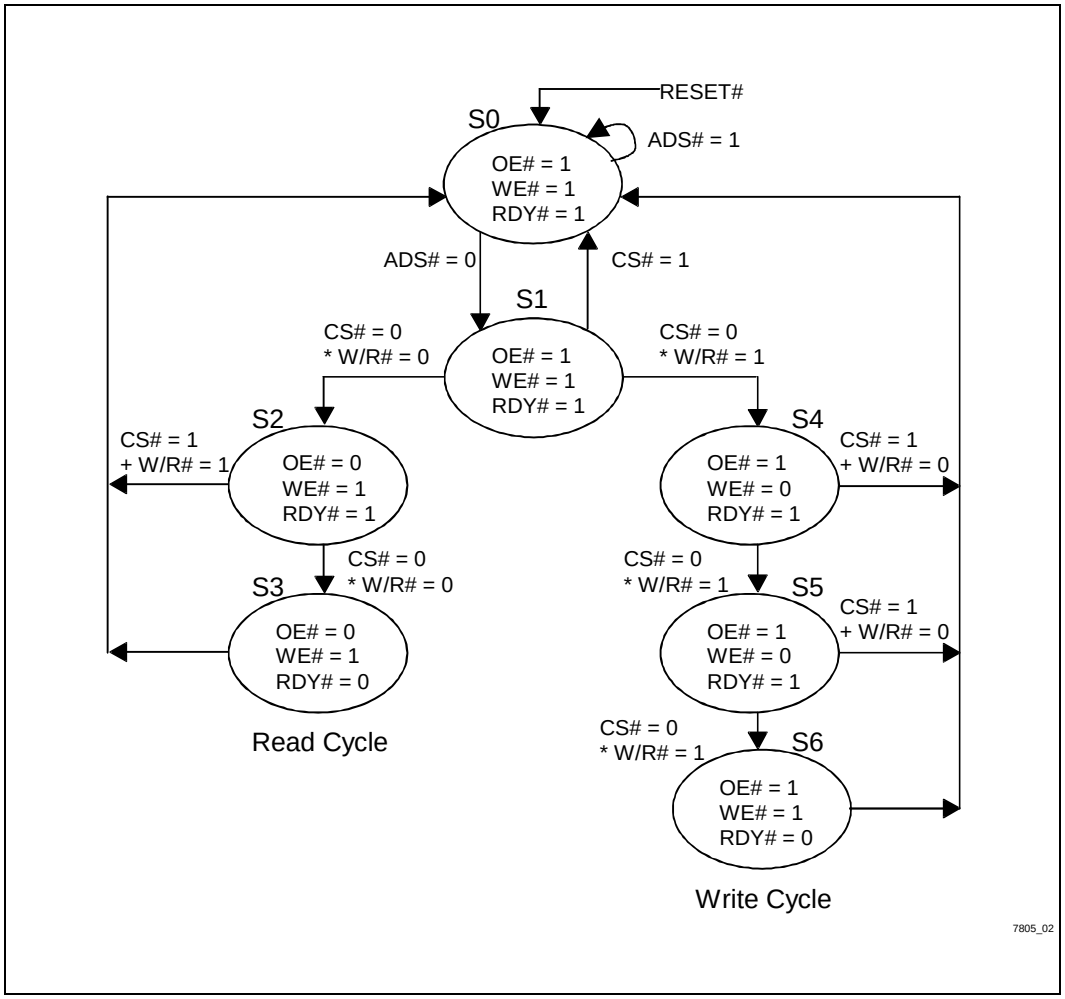

Figure 2. State Diagram for Intel486™ CPU Interface

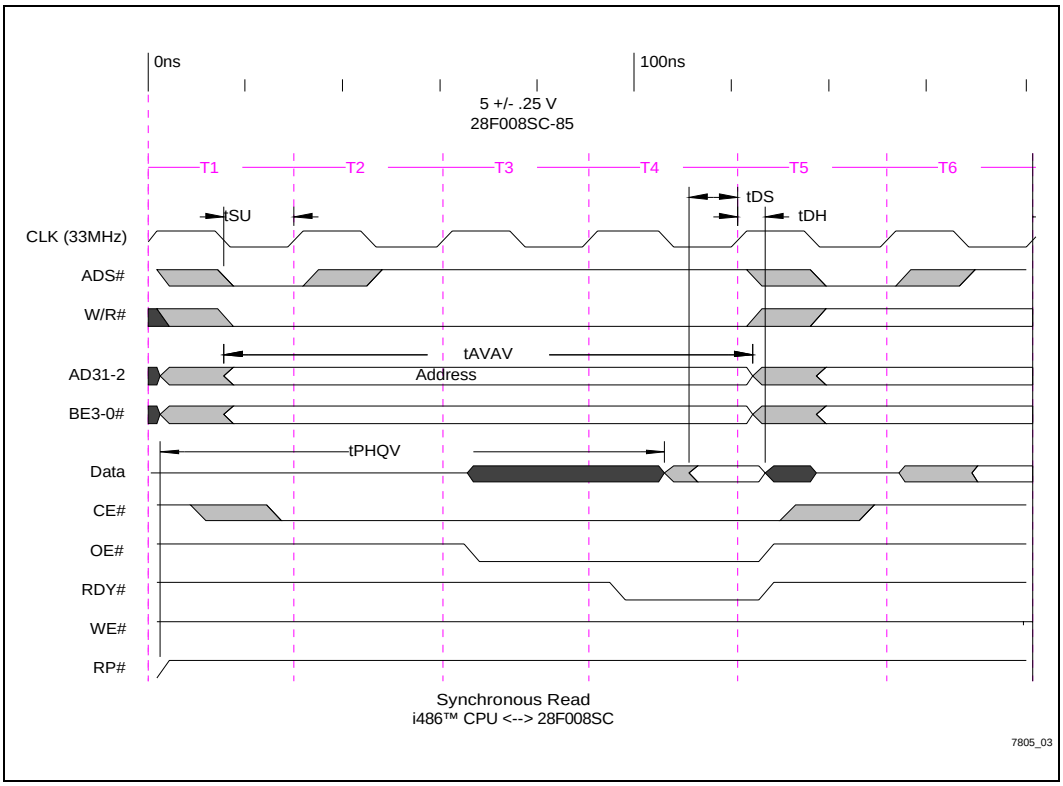

Figure 3. Read Cycle for Intel486™ CPU Interface

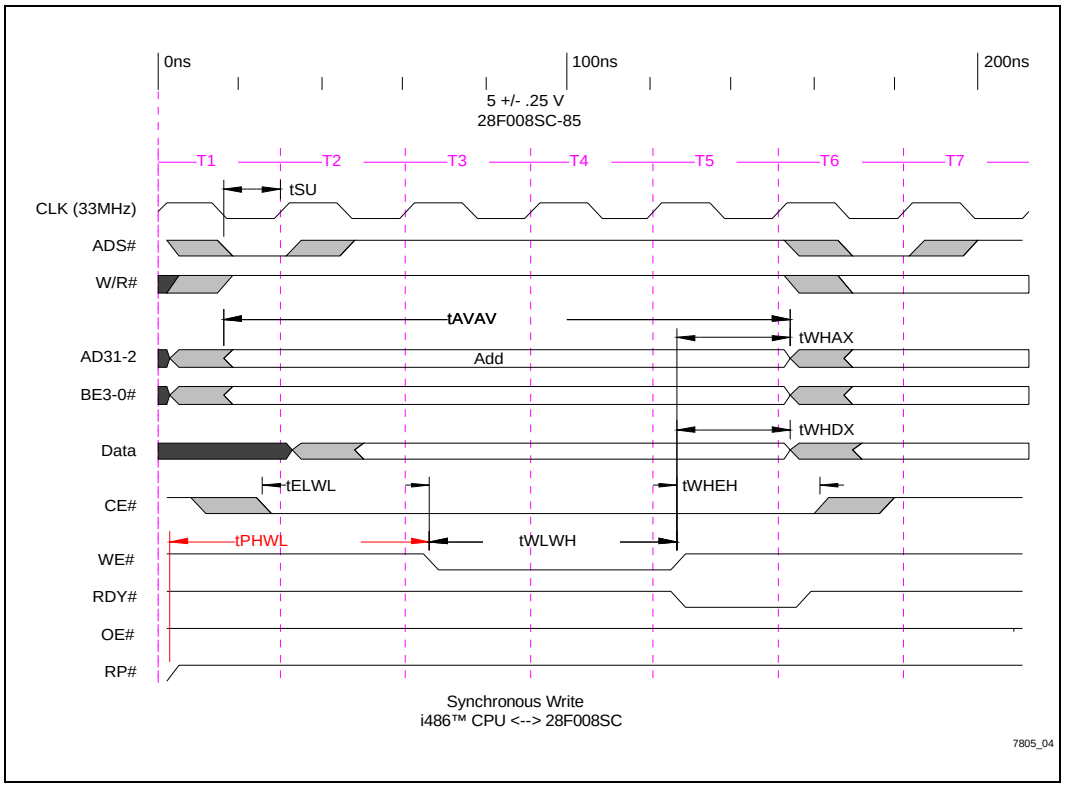

Figure 4. Write Cycle for Intel486™ CPU Interface

2.4 Alternate Interface Configurations

The following section describes the changes which must be made to the state machine described earlier to interface at different Intel486 CPU frequencies as well as different 28F008SC speeds.

3.3V V_{CC} Operation:

When operating at 25 MHz, an additional wait-state is needed between states S2 and S3 when reading from 28F008SC-150s. If the processor is interfacing at 33 MHz, two wait-states must be inserted between states S2 and S3 in the read cycle for the 28F008SC-120s, and three wait-states are needed when reading from -150s. An additional wait-state must also be inserted between states S5 and S6 for the 28F008SC-150s' write cycle.

5V V_{CC} Operation:

If interfacing at 33 MHz, one additional wait-state is necessary between states S2 and S3 when reading from 28F008SC-90s and two wait-states must be added when reading from 28F008SC-120s between states S2 and S3.

Table 3 and Table 4 summarize these changes. An "NC" entry in the table signifies that "No Change" is necessary to the state diagram described above to work in this configuration. A "WS Sx→Sy" entry means a wait-state must be inserted between states Sx and Sy of the state machine. If a state can be omitted from the state machine, a "Skip Sx" is the table entry.

Table 3. 3V V_{CC} Interface Configurations

i486™ CPU	28F008SC	
	-120 ns	-150 ns
20 MHz	**R:** NC **W:** Skip S4	**R:** NC **W:** Skip S4
25 MHz	**R:** NC **W:** NC	**R:** 1 WS S2→S3 **W:** NC
33 MHz	**R:** 2 WS S2→S3 **W:** NC	**R:** 3 WS S2→S3 **W:** 1 WS S5→S6

Table 4. 5V V_{CC} Interface Configurations

i486™ CPU	28F008SC		
	-85 ns	-90 ns	-120 ns
25 MHz	**R:** NC **W:** NC	**R:** NC **W:** NC	**R:** NC **W:** NC
33 MHz	----	**R:** 1 WS S2→S3 **W:** NC	**R:** 2 WS S2→S3 **W:** NC

2.5 Interfacing the Intel486™ Microprocessor to Other Flash Components

For the 28F008SC designs described above, Smart 3 (28F008S3) flash memory is interchangeable with the 28F008SC at 3.3V V_{CC} operation, and Smart 5 (28F008S5) flash memory is interchangeable with the 28F008SC at 5V V_{CC} operation.

This section describes the changes necessary when interfacing with byte-wide 4- and 16-Mbit SmartVoltage (28F004SC/28F016SC), Smart 3 (28F004S3/28F016S3) or Smart 5 (28F004S5/28F016S5) flash memory.

2.5.1 INTERFACING WITH 4-MBIT COMPONENTS

When a 4-Mbit component is used, the A_{21} pin becomes another input to the OR gate, requiring an 11-input OR gate in the interface design.

For 3.3V V_{CC} Operation:

28F004SC/S3-120s and -150s can replace 28F008SC/S3-120s and -150s, respectively, with no changes.

For 5V V_{CC} Operation:

28F004SC/S5-85s, -90s, and -120s can replace 28F008SC/S5-85s, -90s and -120s, respectively, with no changes.

2.5.2 INTERFACING WITH 16-MBIT COMPONENTS

When a 16-Mbit component is used, the A_{22} pin becomes an input to the flash chip, requiring a 9-input OR gate in the interface design.

For 3.3V V_{CC} Operation:

28F016SC/S3-120s and -150s can replace 28F008SC/S3-120s and -150s, respectively, with no changes.

For 5V V_{CC} Operation:

28F016SC/S5-95s can replace 28F008SC/S5-85s with one modification. In the 33 MHz interface, a wait-state is necessary between states S2 and S3 of the read cycle.

28F016SC/S5-100s can replace 28F008SC/S5-90s with no changes.

28F016SC/S5-120s can replace 28F008SC/S5-120s with no changes.

APPENDIX A
ADDITIONAL INFORMATION

Related Intel Documentation(1,2)

Order Number	Document
290597	*Byte-Wide Smart 5 FlashFile™ Memory Family Datasheet*
290598	*Byte-Wide Smart 3 FlashFile™ Memory Family Datasheet*
290600	*Byte-Wide SmartVoltage FlashFile™ Memory Family Datasheet*
242202	*Intel486™ Processor Family Datasheet*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.