TECHNICAL
PAPER

Interfacing the 28F016XS to the Intel486™ Microprocessor Family

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1.0 INTRODUCTION

This technical paper describes designs interfacing the high performance 28F016XS flash memory to the Intel486™ microprocessor. These designs are based on preliminary 28F016XS specifications. Please contact your Intel or distribution sales office for up-to-date information.

The 28F016XS is a 16-Mbit flash memory with a synchronous pipelined read interface. This optimized flash memory interface delivers equivalent or better read performance compared to DRAM. The 28F016XS combines ROM-like nonvolatility, DRAM-like read performance and in-system updateability into one memory technology. These inherent capabilities will improve performance and lower the over-all system cost.

The 28F016XS delivers optimal performance when interfacing to a burst processor, such as the Intel486 microprocessor. The Intel486 microprocessor sees widespread use in a variety of applications ranging from the PC to numerous embedded products, while providing code compatibility with thousands of commercially available software packages and the performance necessary for today's leading-edge systems. The Intel486 microprocessor's bus interface provides a burst transfer mechanism whereby four consecutive data items are fetched in one access sequence. The 28F016XS's synchronous pipelined read interface makes special use of the burst transfer mechanism to achieve extremely high read performance.

When interfacing the 28F016XS to a processor that executes an Intel or linear burst cycle, up to three simultaneous read accesses can be pipelined into the 28F016XS, sustaining a high read transfer rate. At 33 MHz, the 28F016XS-15 delivers zero wait-state performance after the initial pipeline fill. This enhanced read performance eliminates the costly expense of shadowing code from slow nonvolatile memory (ROM, hard disk drive, etc.) to fast DRAM for increased system performance. The 28F016XS enables direct code execution out of the flash memory array, eliminating unnecessary software and hardware overhead involved in shadowing code.

In an Intel486 microprocessor-based environment, BAPCo benchmarking analysis revealed a ***13%*** system performance improvement using the 28F016XS-15 over 70 ns DRAM.

In addition to the increased read performance, the 28F016XS offers an Intel486 microprocessor-based system a low power, nonvolatile memory that is electrically updateable via local processor control. The 28F016XS's low power consumption reduces system power dissipation and heat emission, and its updateability increases code flexibility and system reliability. Combined, the 28F016XS and the Intel486 microprocessor deliver a high performance, low power and cost-effective system solution.

The Intel486 microprocessor interface to the 28F016XS requires minimal logic while offering significant system enhancements. One programmable logic device (PLD), a 22V10-15, generates and monitors all 28F016XS and Intel486 microprocessor control signals. This technical paper explores the interface between the 28F016XS-15 and the Intel486™ SX-33 microprocessor, describing the interface circuitry, explaining the read and write cycles and providing the interfacing PLD equations. It also provides detailed design suggestions for interfacing the 28F016XS to other Intel486 microprocessors.

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2.0 OPTIMIZED 28F016XS/INTEL486™ SX MICROPROCESSOR INTERFACE

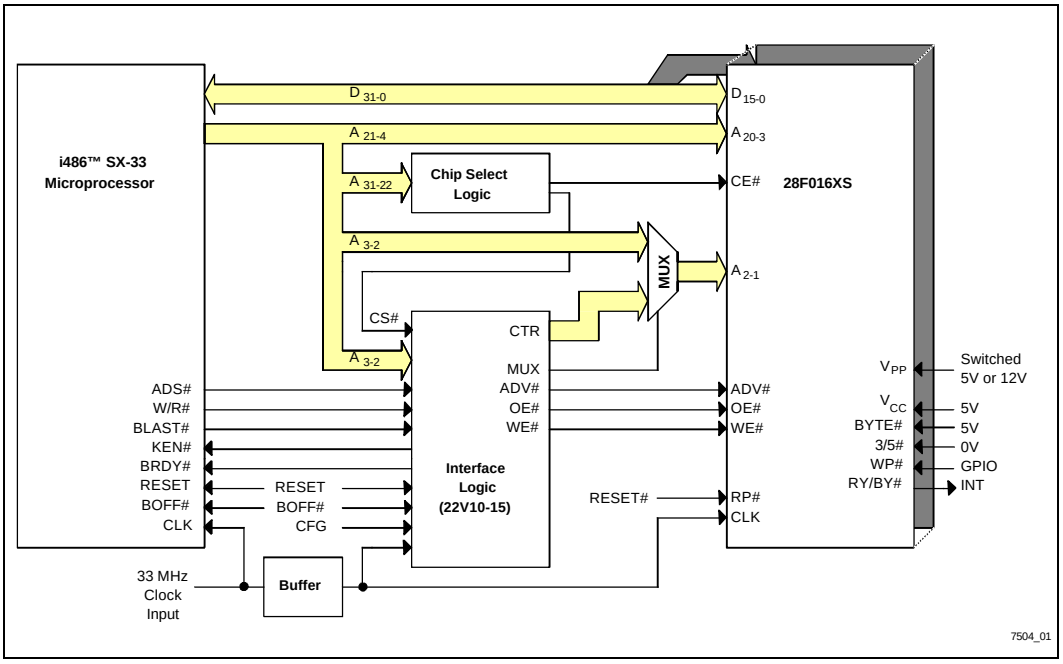

Figure 1. Optimized 28F016XS Interface to the Intel486 Microprocessor with Wait-State Profile of 2-0-0-0 up to 33 MHz

The 28F016XS-15 interface to the Intel486 SX-33 microprocessor, illustrated in Figure 1, delivers 2-0-0-0 wait-state read performance. Consult your Intel or distribution sales office for schematic and PLD files for this design.

See Section 3.0 for an alternative design.

2.1 Circuitry Description

This section will describe the circuitry involved in this design.

Memory Configuration

This design uses two 28F016XS-15s, each configured in x16 mode and arranged in parallel to match the Intel486 SX microprocessor's 32-bit data bus. This memory configuration provides 4 Mbytes of flash memory for system usage. Signals $A_{21–4}$ from the Intel486 SX microprocessor and $CTR_{1–0}$ from the PLD select locations within the 28F016XS memory space. The two-bit counter implemented in the PLD supplies burst addresses to the 28F016XSs.

Reset

The Intel486 SX microprocessor requires an active high reset signal, while the 28F016XSs use an active low RESET#. Figure 2 illustrates a suggested logic configuration for generating both an active high and low reset signal. The active high RESET controls the Intel486 SX microprocessor and PLD reset inputs, while the active low RESET# drives the 28F016XS RP# input.

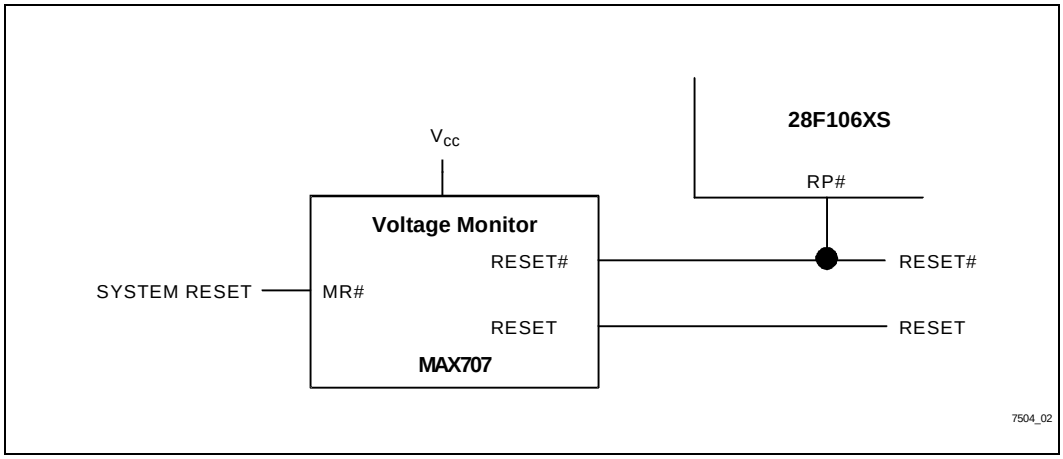

Figure 2. RESET Generation Method

Chip Select Logic

Chip select decode logic may use A_{31-22} to generate active low chip select signals, CE_X#, for the 28F016XS memory space and other system peripherals. The chip select addressing the 28F016XS memory space drives CE_0# on each 28F016XS-15 and a control input to the PLD. The 28F016XS-15s' CE_1# inputs are grounded. For many systems, using the upper address bits in a linear selection scheme may provide a sufficient number of chip select signals, thus eliminating chip select decode logic. (See Figure 3 for an example of using linear selection for chip selects.) When using a linear chip select scheme however, software must avoid using addresses that may select more than one device, which could result in bus contention. For example, addresses 01000000H through 010FFFFFH drive both A_{22} and A_{23} to a logic "0," which inadvertently selects two peripheral devices.

CLK Option

A 33 MHz CLK drives the Intel486 SX microprocessor. The buffer in Figure 1 delays this processor CLK input and drives the PLD and the 28F016XS-15s. The buffer introduces an intentional system clock skew. This skew provides additional time for the processor to meet the 28F016XSs' address setup time.

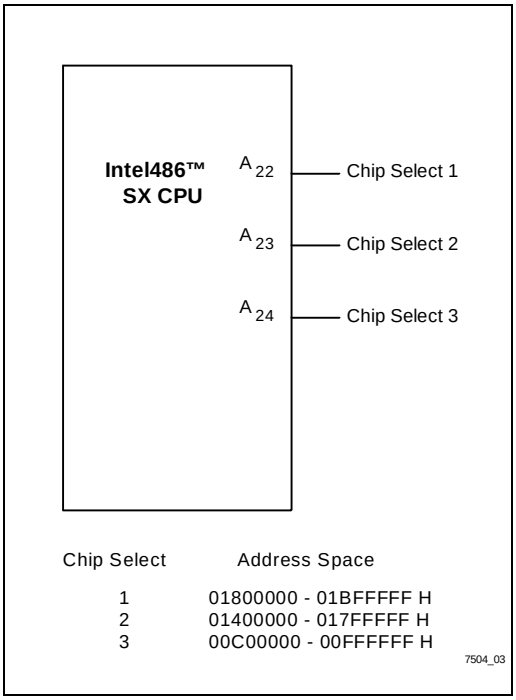

Figure 3. Example of Using Linear Chip Selection with Active Low Chip Select Signals

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Multiplexer (MUX)

To achieve this type of wait-state profile, the Intel486 SX microprocessor directly loads the 28F016XSs with the initial address. The interface logic enables the MUX to permit the processor's lower address lines A_{3-2} access to the lower flash memory address lines. Next, the interface logic switches the data flow path through the MUX in anticipation of a burst transaction. The two-bit counter integrated into the control logic takes over driving the 28F016XSs' A_{2-1}. The counter supplies the flash memory with consecutive burst addresses for the remaining duration of the transaction.

Interface Control Signals

The interfacing state machine monitors the Intel486 SX microprocessor's external bus signals to identify the type, start and end of the bus cycle. At the beginning of a burst cycle, the interface logic loads a two-bit counter and generates the flash memory control signals. The state machine also generates KEN# and BRDY# signals, informing the Intel486 SX microprocessor of the nature of the bus cycle.

Configuration Signal

A general purpose input/output (GPIO) generates the configuration signal input (CFG) to the state machine. CFG must reset to logic "0" on power-up and system reset to ensure coherency between and 28F016XS-15s. After optimizing the 28F016XSs' SFI Configuration, CFG must switch to logic "1" in order to take advantage of the optimized flash memory state. See Section 2.3 for more information regarding the configuration signal.

Additional 28F016XS Control Signals

The BYTE# input to the 28F016XS-15s is tied to 5.0V to configure the 28F016XS-15s for x16 mode, and 3/5# and A_0 are tied to GND (A_0 is only used for byte addressing). A GPIO controls the write protect input, WP#, to the 28F016XS-15s. The 28F016XS is compatible with either a 5.0V or a 12.0V V_{PP} voltage and is completely protected from data alteration when V_{PP} is switched to GND. With $V_{PP} \leq V_{PPLK}$, the 28F016XS will not successfully complete data write and erase operations, resulting in absolute flash memory data protection. Figure 1 also illustrates the 28F016XS-15's RY/BY# output connecting directly to a system interrupt, which enables background write/erase operations. RY/BY#, WP#, and V_{PP} implementations are application dependent. Consult the Additional Information section of this technical paper for documentation covering these topics in more detail.

2.2 Interfacing Signal Definitions

The interface logic that controls the 28F016XS-15 interface to the Intel486™ SX-33 microprocessor monitors and regulates specific system signals. The next two sections describe these signals in detail.

2.2.1 28F016XS Signal Descriptions

This section describes the 28F016XS signals that are pertinent to this design.

ADV# - Address Valid (Input)

This active low signal informs the 28F016XS that a valid address is present on its address pins. ADV#, in conjunction with a rising CLK edge, initiates a read access to the 28F016XS. This signal is ignored during write operations.

CLK - Clock (Input)

CLK provides the fundamental timing and internal operating read frequency for the 28F016XS. CLK initiates read accesses (in conjunction with ADV#), times out the SFI Configuration, and synchronizes device outputs. CLK can be slowed or stopped with no loss of data synchronization. This signal, like ADV#, is ignored during write operations.

OE# - Output Enable (Input)

This active low signal activates the 28F016XS's output buffers when OE# equals "0." The outputs tri-state when OE# is driven to "1."

WE# - Write Enable (Input)

This active low signal controls access to the Control User Interface (CUI). Addresses (command or array) and data are latched on the rising edge of WE# during write cycles.

2.2.2 INTEL486™ SX Microprocessor Signal Descriptions

This section describes the Intel486 SX microprocessor signals that are relevant to this interface. This interface assumes processor inputs are driven by only one controlling device (the PLD). If more than one device drives a processor input, the PLD output should be configured as an open drain to avoid signal contention. Many PLDs, FPGAs and ASICs provide output configuration capability.

ADS# - Address Status (Output)

This active low output signal from the Intel486 SX microprocessor indicates the presence of valid bus cycle and address signals on the bus. ADS# is driven in the same clock as the address signals. Typically, external circuitry uses ADS# to indicate the beginning of a bus cycle.

KEN# - Cache Enable (Input)

This active low input to the Intel486 SX microprocessor determines whether data being returned in the current bus cycle will be cached. In order for the current data to be cached, KEN# must be returned active in the clock prior to the first RDY# or BRDY# of the cycle and must also be returned active in the last clock of the data transfer.

BRDY# - Burst Ready (Input)

This active low input to the microprocessor performs the same function during a burst cycle as RDY# performs during a non-burst cycle. During a burst cycle, BRDY# is sampled on the rising edge of every clock. Upon sampling BRDY# active, the data on the data bus will be latched into the microprocessor (for burst reads). ADS# will be negated during the second transfer of the burst cycle; however, the lower address lines and byte enables may change to indicate the next data item requested by the processor.

BLAST# - Burst Last (Output)

This active low output from the microprocessor signals the final transfer in a burst cycle. The next time BRDY# is returned, it will be treated the same as RDY# and thus terminate any multiple cycle transfers.

2.3 System Interface Requirement

The system logic controlling the 28F016XS-15 interface to the Intel486 SX microprocessor incorporates an initial and an optimized read configuration, which correlates to specific SFI Configuration values. The interface read configuration is dependent upon the value of CFG (PLD input). CFG informs the interface of the SFI Configuration status. Note, the SFI Configuration status does not affect Write operations.

Initial Read Configuration

Upon power-up/reset, the 28F016XS-15 defaults to a SFI Configuration value of 4, and the interface logic supports burst read accesses to the flash memory space. The interface returns BRDY# to inform the processor that the interface supports burst read transaction. A general purpose input/output (GPIO) informs the system interface of the status of the SFI Configuration.

The GPIO entitled CFG is set to logic “0” on power-up/reset. With CFG driven low, the state machine correctly matches the 28F016XS-15s’ default configuration.

Optimized Read Configuration

At 33 MHz, the 28F016XS-15 operates at highest performance with a SFI Configuration value set to 2. To reconfigure the 28F016XS-15, program control should jump to an area of RAM to execute the configuration sequence. After reconfiguring the 28F016XS-15, the GPIO value must change to logic “1,” in order to take advantage of the 28F016XS-15’s optimized configuration. A pseudocode flow for this configuration sequence is shown below.

Execute Device Configuration command sequence
Activate CFG signal
End

In the optimized read configuration, the system logic supports burst cycles by generating BRDY#, which informs the microprocessor that the memory subsystem is capable of handling a burst transfer. The 28F016XS-15 memory array, after the initial pipeline fill delay from the first access, transfers data to the processor at a rate of 133 Mbytes/sec.

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2.4 Read Control for Burst Transactions

The interface logic controlling the handshaking between the 28F016XS and processor performs one of two different read cycles, depending upon the value of CFG.

Read Abort Condition

A read cycle will abort only when an external system bus master asserts BOFF#, which forces the processor to give immediate bus control to the requester. When this situation occurs, the Intel486 SX microprocessor floats the address bus, which will cause the address decode logic to de-select the 28F016XS memory space. Detecting BOFF# active, the interfacing logic will transition to an idle state and wait for the processor to re-initiate the interrupted bus cycle after the bus master has relinquished the bus to the processor. OE# is immediately driven high, deactivating the 28F016XS-15's output buffers, upon detecting BOFF# driven active. This BOFF# condition can occur in both the initial and optimized configurations described in the paragraphs that follow.

Initial Configuration

Refer to Figures 4 and 5 for the following read cycle discussion.

With CFG set to logic "0," the interfacing read state machine executes cacheable burst read cycles. This configuration occurs upon power-up and reset.

Initially, the interface logic drives ADV# and MUX active while waiting for the Intel486 SX processor to initiate a bus cycle targeting the 28F016XS. With the MUX active, the processor's A_{3-2} drive the lower flash memory address lines in anticipation of a flash memory access. During this anticipation state, CE# is active to prevent a t_{ELCH} violation on the first access initiated by the processor. The delayed CLK prevents a possible timing violation. It provides the processor with sufficient time to meet the 28F016XSs' t_{AVCH} specification when initiating the first access.

When the microprocessor initiates a read access to the 28F016XS memory space, it provides an address and drives W/R# and ADS# low. Monitoring these signals, the state machine transitions into read control.

If ADS# = 0 and W/R# = 0 then READ CONTROL

At this point, CFG and CS# are examined to determine the configuration status of the 28F016XS-15s, and whether or not the current address targets the 28F016XS memory space. If CS# = "1," the state machine returns to an idle state waiting for a new access. Otherwise, the state machine will continue the read access, regulating ADV#, BRDY# and OE#.

At N = 1 (Figure 5), the interfacing read state machine loads and increments the two-bit counter. The counter is incremented because the processor supplies the flash memory with the initial address. The counter then provides the flash memory with the subsequent burst addresses throughout the remaining duration of the bus transaction.

With ADV# at logic "0," the interface initiates a read access to the 28F016XS-15s at N = 1. Next, ADV# immediately switches to a logic "1" at N = 1 and then toggles active on every other clock edge until N = 8. After this time, ADV# will remain inactive.

In the default SFI Configuration (SFI Configuration = 4), the first data will be accessible to the processor at N = 6. The remaining data will be available for the processor to retrieve at N = 8, 10 and 12. The 28F016XS-15's output buffers are enabled at N = 3 and BRDY# is driven low at N = 5. The processor will sample BRDY# active and latch the information residing on the data bus at N = 6. If the processor drives BLAST# inactive, indicating a burst transaction is in process, the interface logic will drive BRDY# active on every other clock edge until BLAST# is sampled active by the interface logic. The state machine will transition to an idle state where it deactivates OE# and waits for the processor to initiate a new bus cycle.

Initial Configuration Timing Consideration

In this initial read configuration, there are important timing considerations that need examination.

First, the buffer delay can cause possible timing violations if not chosen correctly. The purpose of the buffer is to provide time for the processor to load the 28F016XSs with the initial address during read transactions. Therefore, the buffer must have a minimum delay which satisfies the flash memory's t_{AVCH}.

$$t_{AVCH} + t_6 - 1/33\ MHz = 1\ ns$$

The buffer can also affect the processor's data setup time. Hence, the buffer must have a maximum delay of no greater than:

$$1/33\ MHz - t_{CHQV} - t_{22} = 5\ ns$$

Another important timing parameter is the Intel486 SX microprocessor's data hold time. Since the 28F016XS specifies a 0 ns guaranteed data hold time from CE# or OE# high, these two signals must be driven active until the processor's hold time is satisfied. CE# hold delay will not be concern because CE# is held active during the state machine's idle state. OE# has only .5 ns of margin to the processor's specification for the buffer used in this design. OE# hold time equals:

$$t_{PZX(min)} + t_{PHL(min)} = 3.5\ ns$$

Consult the appropriate datasheets for full timing information.

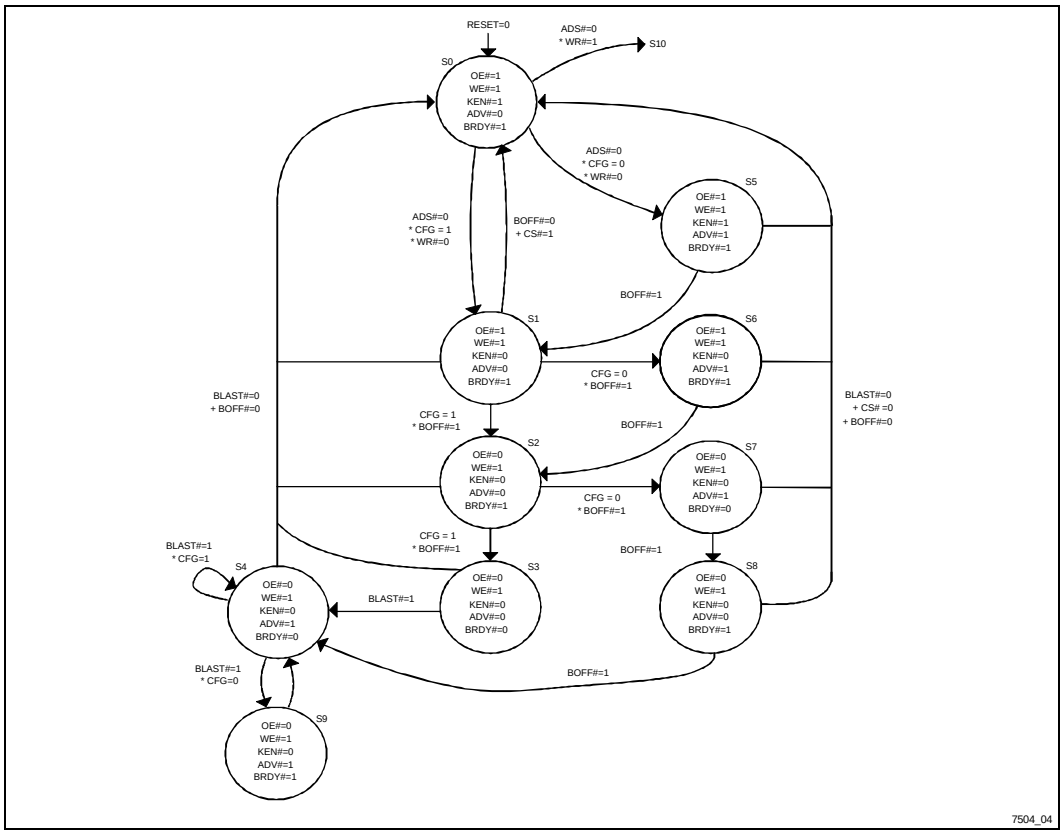

Figure 4. Optimized Read State Diagram for Burst Read Control (Interface Shown in Figure 1)

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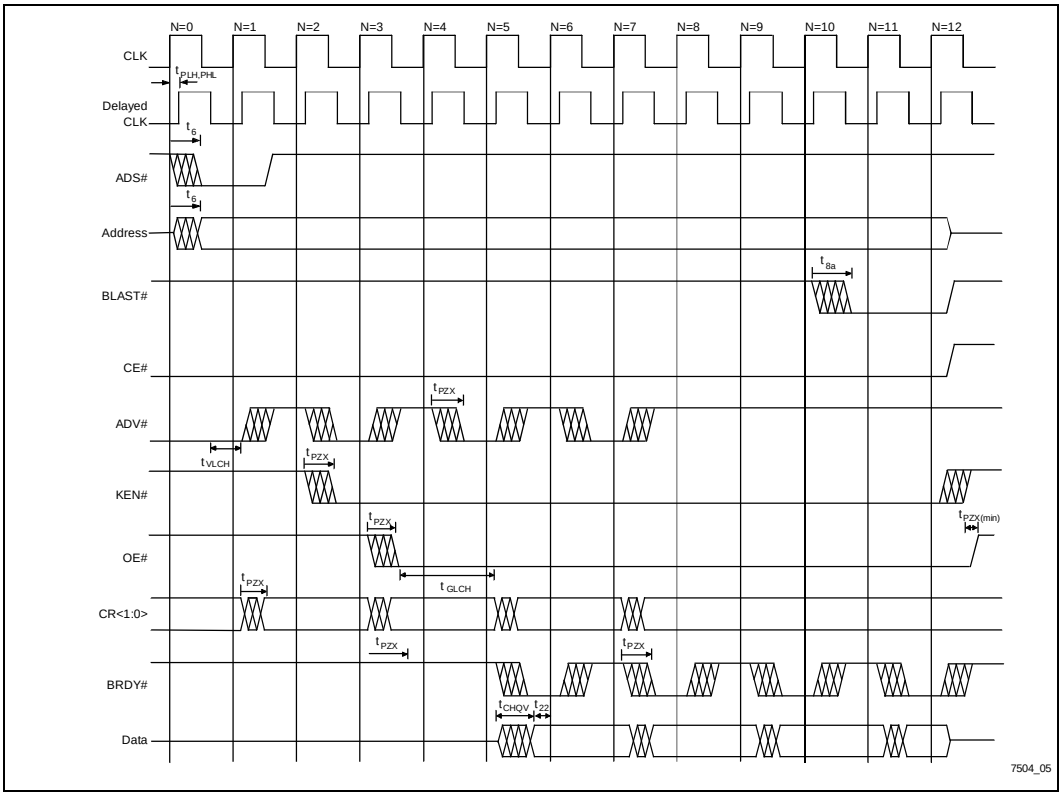

Figure 5. Example Initial Burst Read Cycle Showing Key Timing Specifications Requiring Consideration

Table 1. Example Optimized Read Cycle Specifications at 5V V_{CC}

Symbol	Description	Min	Max	Unit
$t_{PHL,PLH}$	Buffer Delay	1.5	5	ns
t_6	ADS# Delay (Intel486™ SX-33 microprocessor)	3	16	ns
t_{8a}	BLAST# Delay (Intel486 SX-33 microprocessor)	3	20	ns
t_{22}	D_{31-0} Setup Time (Intel486 SX-33 microprocessor)	5		ns
t_{ELCH}	CE_X# Setup Time to CLK (28F016XS-15)	25		ns
t_{VLCH}	ADV# Setup Time to CLK (28F016XS-15)	15		ns
t_{GLCH}	OE# Setup Time to CLK (28F016XS-15)	15		ns
t_{CHQV}	CLK to Data Delay (28F016XS-15)		20	ns
t_{PZX}	CLK Output Delay (22V10-15)	2	8	ns

NOTE:
Consult appropriate datasheets for up-to-date specifications.

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Optimized Configuration

Refer to Figures 4 and 6 for the following discussion.

With the 28F016XS-15s in the optimized configuration (SFI Configuration = 2 at 33 MHz), and CFG set to a logic "1" value, the system interface executes cacheable burst cycles.

Like the initial configuration, the connecting logic initially drives ADV# and MUX active while waiting for the Intel486 SX processor to initiate a bus cycle targeting the 28F016XS. With the MUX active, the processor's A_{3-2} drive the lower flash memory address lines in anticipation of a flash memory access. During this anticipation state, CE# is active to prevent a t_{GLCH} violation on the first access initiated by the processor. The delayed CLK also inhibits also possible timing violations from occurring. It provides the processor with sufficient time to meet the 28F016XSs' t_{AVCH} specification when initiating the first access.

When the processor drives ADS# low, it notifies the interface logic that a valid address is on the address bus. Monitoring the external bus of the Intel486 SX microprocessor, the state machine then transitions into read control.

If ADS# = 0 and W/R# = 0 then READ CONTROL

In optimized read control, the state machine controls OE#, KEN# and BRDY#. If CS# = "0," the state machine at N = 1 loads and increments the two-bit counter, switches the data flow path through the MUX and holds ADV# active for the next three consecutive clock periods. While ADV# is driven low, the counter increments through the Intel burst order (Table 2), supplying the 28F016XS-15s with a new address at N = 2, 3 and 4. If CS# = "1," the state machine returns to an idle state waiting for a new memory access.

Table 2. Intel Burst Order (A_{3-2})

First Address	Second Address	Third Address	Fourth Address
0	4	8	C
4	0	C	8
8	C	0	4
C	8	4	0

At N = 2, the state machine drives KEN# active and holds it active until the end of the burst cycle, thereby executing a cache line fill.

The state machine activates the 28F016XS-15 output buffers (OE# driven to a logic "0" value) at N = 2 and holds them active throughout the burst read cycle.

With the SFI Configuration value set to 2, data will be available at N = 4, 5, 6 and 7. Driving BRDY# low at N = 3, the Intel486 SX microprocessor will sample BRDY# active at N = 4, which informs the processor of valid information on data pins D_{31-0} and that the 28F016XS memory space supports a burst read transfer. BRDY# is held low until the end of the burst cycle while the processor retrieves data on every rising clock edge. BRDY# is driven high upon sampling BLAST# low, marking the end of the burst cycle. Then the state machine will transition to and idle state where it deactivates OE# and waits for the processor to initiate a new bus cycle.

Optimized Configuration Timing Considerations

In the optimized configuration, the same timing consideration regarding the buffer propagation delay and OE# hold time require attention. For information regarding these concerns, see Section 2.4 Initial Configuration Timing Considerations.

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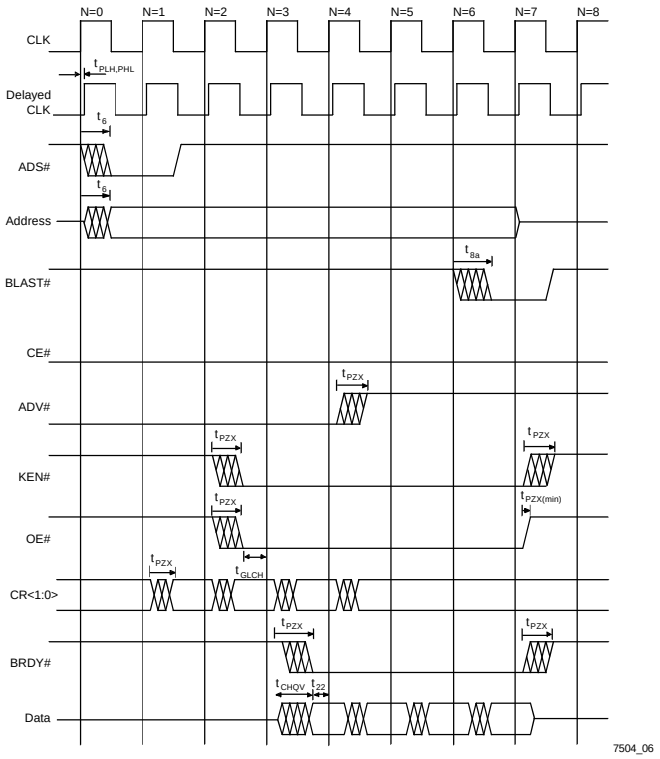

Figure 6. Example Burst Read Timing Waveform Illustrating Key Timing Specifications Requiring Consideration

Table 3. Example Optimized Read Cycle Specifications at 5V V_{CC}

Symbol	Description	Min	Max	Unit
$t_{PHL,PLH}$	Buffer Delay	1.5	5	ns
t_6	ADS# Delay (Intel486™ SX-33 microprocessor)	3	16	ns
t_{8a}	BLAST# Delay (Intel486 SX-33 microprocessor)	3	20	ns
t_{22}	D_{31-0} Setup Time (Intel486 SX-33 microprocessor)	5		ns
t_{ELCH}	CE_X# Setup Time to CLK (28F016XS-15)	25		ns
t_{VLCH}	ADV# Setup Time to CLK (28F016XS-15)	15		ns
t_{GLCH}	OE# Setup Time to CLK (28F016XS-15)	15		ns
t_{CHQV}	CLK to Data Delay (28F016XS-15)		20	ns
t_{PZX}	CLK Output Delay (22V10-15)	2	8	ns

NOTE:
Consult appropriate datasheets for up-to-date specifications.

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2.5 Write Cycle Control

Refer to Figures 7 and 8 for the following write cycle discussion.

Write Abort Condition

A write cycle will abort only when an external system bus master asserts BOFF#, which forces the processor to give immediate bus control to the requester. When this situation occurs, the Intel486 SX microprocessor will float the address bus, causing the address decode logic to de-select the 28F016XS memory space. The interfacing logic, monitoring BOFF#, will transition to an idle state where it will wait for the processor to re-initiate the interrupted bus cycle after the bus master has relinquished the bus to the processor. WE# is immediately deactivated upon sensing BOFF# low.

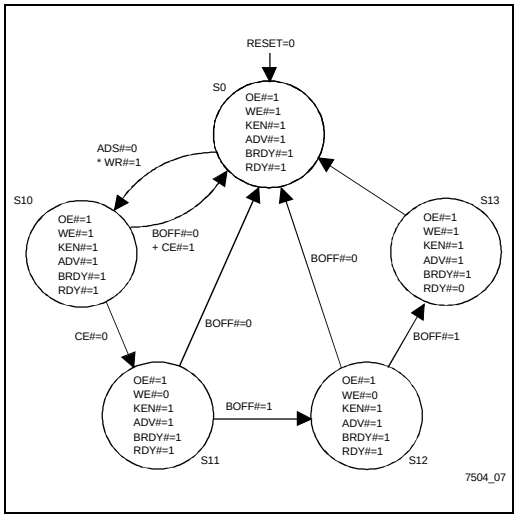

Figure 7. Non-Burst Write State Diagram Controlling the Interface Shown in Figure 1

Write Cycle Description

The 28F016XS-15 executes asynchronous write cycles like traditional flash memory components such as the 28F016SA/SV. The SFI Configuration does not influence write operations; therefore, the interfacing state machine does not examine CFG once detecting a write cycle.

During the first clock period, the Intel486 SX microprocessor drives ADS# low and W/R# high. The state machine, upon detecting a write cycle, immediately switches the data flow path through the MUX. The processor does not drive the flash memory's lower address lines during write cycles. The counter loads and supplies the address to the 28F016XSs' lower two address lines, A_{2-1}. The state machine then transitions to write control at N = 1. The counter only supplies the 28F016XS-15 with one address throughout the entire write operation. A write transaction must compete fully before issuing a second write operation.

If ADS# = 0 and W/R# = 1 then WRITE CONTROL

In write control, the state machine performs WE#-Controlled Command Write operations to the 28F016XS-15s. Data is written to the 28F016XS memory space via processor control. The interface only supports double word writes.

For the next two clock periods the state machine holds WE# low to satisfy the 28F016XS-15s' WE# active requirement. At N = 4, WE# transitions to a logic "1," which latches the address and data into the 28F016XS-15s.

BRDY# is not returned to the processor at N = 4 because the Intel486 SX microprocessor will only hold an address 3 ns after sampling BRDY# low. Instead, the interface activates BRDY# after N = 4, causing the processor to hold the address valid for an additional clock cycle, which satisfies the 28F016XS-15's address hold specification (t_{WHAX}). The state machine then returns to an inactive state at N = 5, waiting for a new memory access.

Write Timing Consideration

When performing a write operation, CS# is a critical system timing parameter, which must satisfy the interface logic's required setup time. The 22V10-15 requires a 9 ns setup time to CLK. Therefore, the system decode logic must generate a valid CS# to the interface within:

$$2 \times 1/33\ \text{MHz} - t_6 - t_{SU} = 35\ \text{ns}$$

Consult the appropriate datasheets for full timing information.

PRODUCT PREVIEW

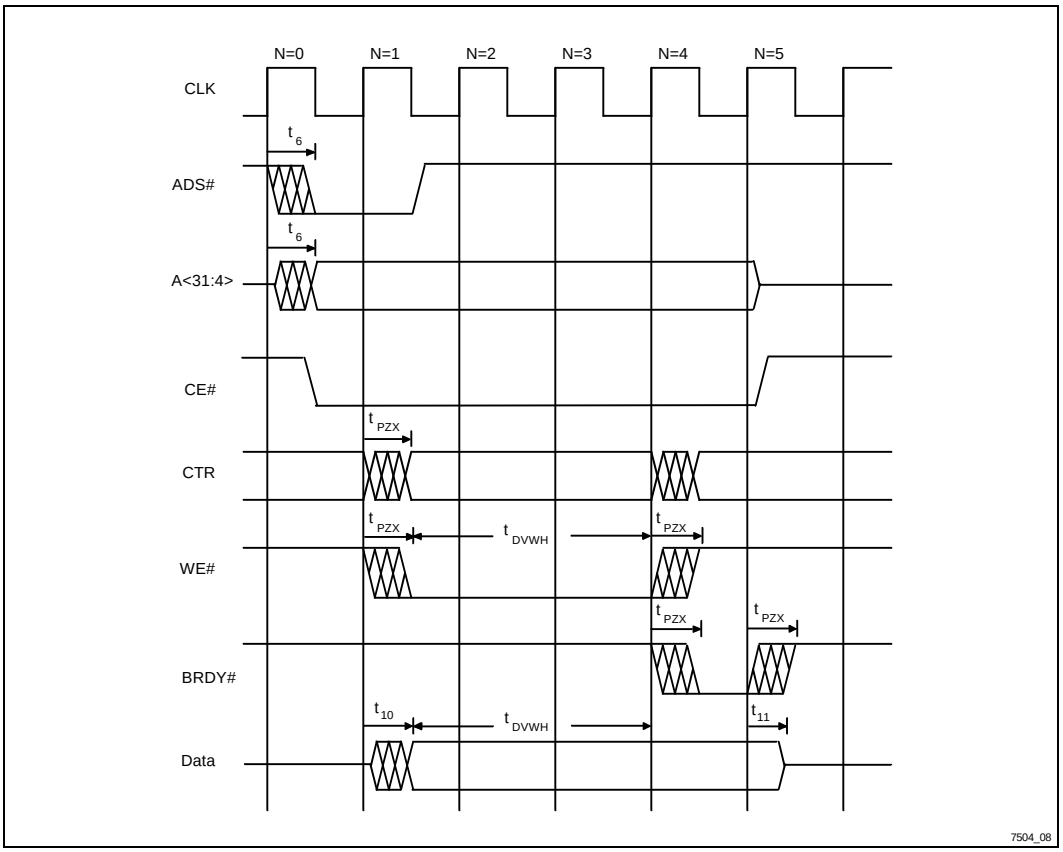

Figure 8. Example Write Cycle Showing Key Timing Specifications Requiring Consideration

Table 4. Example Write Cycle Timing Specifications at 5V V_{CC}

Symbol	Description	Min	Max	Unit
t_6	ADS# Delay(Intel486™ SX-33 microprocessor)	3	16	ns
t_{10}	Data Write Valid Delay (Intel486 SX-33 microprocessor)	3	18	ns
t_{11}	Data Write Float Delay (Intel486 SX-33 microprocessor)		20	ns
t_{WLWH}	WE# Pulse Width (28F016XS-15)		50	ns
t_{DVWH}	Data Setup to WE# Going High (28F016XS-15)		50	ns
t_{PZX}	CLK Output Delay (22V10-15)	2	8	ns

NOTE:
Consult appropriate datasheets for up-to-date specifications.

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3.0 STANDARD 28F016XS/INTEL486 SX MICROPROCESSOR INTERFACE

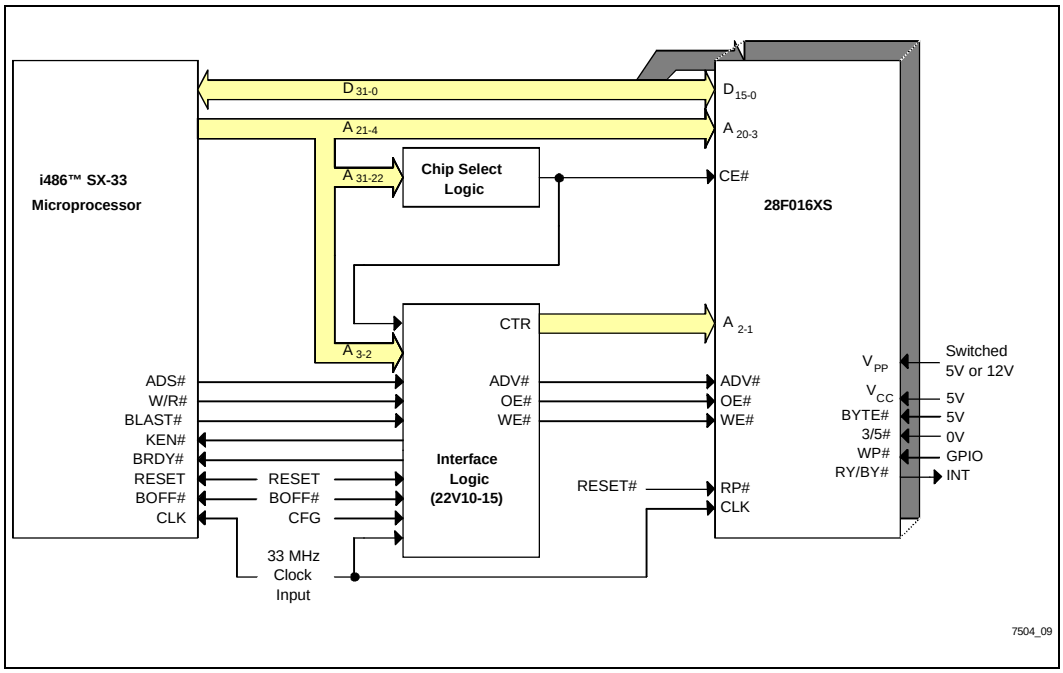

Figure 9. Minimal Glue Logic in Interfacing the 28F016XS-15 to the Intel486™ SX-33 Microprocessor with a Wait-State Profile of 3-0-0-0 Up to 33 MHz

The 28F016XS-15 interface to the Intel486 SX-33 microprocessor illustrated in Figure 9 delivers 3-0-0-0 wait-state read performance. The design requires only one 22V10 to handle all interfacing requirements. Consult your Intel or distribution sales office for schematic and PLD equations for the interface documented in this section.

See Section 2.0 for an alternative design.

3.1 Interface Circuitry Description

This interface is extremely similar to the optimized design described in Section 2. The circuitry elements involved in the design are exactly the same except for the elimination of the buffer and multiplexer. For specific circuitry information about the individual aspects of this design, refer to Section 2.

CLK Option

Unlike the optimized 28F016XS/Intel486 SX microprocessor interface, a buffer is not implemented in this design. The processor's 33 MHz CLK input drives both the PLD and flash memory. To reduce system clock skew, position the PLD and 28F016XSs within close proximity to the microprocessor.

3.2 Read Control for Burst Transactions

Similar to the optimized design described in Section 2, the read state machine will perform one of two different read cycles, depending upon the CFG input value. This section will concentrate on the differences between the read two read configurations.

PRODUCT PREVIEW

Initial Configuration

Refer to Figures 10 and 11 for the following read cycle discussion.

With CFG set to logic "0," the interfacing read state machine executes cacheable burst read cycles. This configuration will occur upon power-up and reset.

The microprocessor initiates a read access to the 28F016XS memory space by providing an address, driving W/R# low and activating ADS#. Monitoring the external bus of the Intel486 SX microprocessor, the state machine transitions into read control.

If ADS# = 0 and W/R# = 0 then READ CONTROL

At this point, CFG and CE# are examined to determine the configuration status of the 28F016XS-15s, and whether or not the current address targets the 28F016XS memory space. If CE# = "1," the state machine returns to an idle state waiting for a new access. Otherwise, the state machine will continue read access. In the initial configuration (CFG = "0"), read control will regulate ADV#, BRDY# and OE#.

At N = 1 (Figure 5), the counter loads address bits A_{3-2} and transitions ADV# low. With ADV# at logic "0," the interface initiates a read access to the 28F016XS-15s at N = 2. After initiating the read access, ADV# immediately switches to a logic "1" at N = 2 and then toggles active on every other clock edge until N = 8. After which, ADV# will remain inactive.

In the default SFI Configuration (SFI Configuration = 4), the first data will be accessible to the processor at N = 7. The rest of the data will be available for the processor to retrieve at N = 9, 11 and 13. The 28F016XS-15's output buffers are enabled at N = 4 and BRDY# is driven low at N = 6. The processor will sample BRDY# active and latch the information residing on the data bus at N = 7. If the processor drives BLAST# inactive indicating a burst transaction is in process, the interface logic will drive BRDY# active on every other clock edge until BLAST# is sampled active by the interface logic.

The Intel486 SX microprocessor requires a 3 ns hold time after sampling BRDY# active, therefore, the state machine will hold OE# active for 15 ns after the processor reads the last double-word. Then, the state machine will transition to an idle state where it deactivates OE# and waits for the Intel486 SX microprocessor to initiate a new bus cycle targeting the 28F016XS memory space.

Initial Configuration Timing Consideration

In the initial read configuration, CE# setup is a key system timing parameter.

To satisfy the 28F016XS-15 setup requirement, CE# must be valid 25 ns prior to the first rising CLK edge with ADV# = "0." Therefore, the maximum time allotted for the address decoding logic to generate CE# equals:

$$2 \times 1/33\ \text{MHz} - t_6 - t_{ELCH} = 19\ \text{ns}$$

Consult the appropriate datasheets for full timing information.

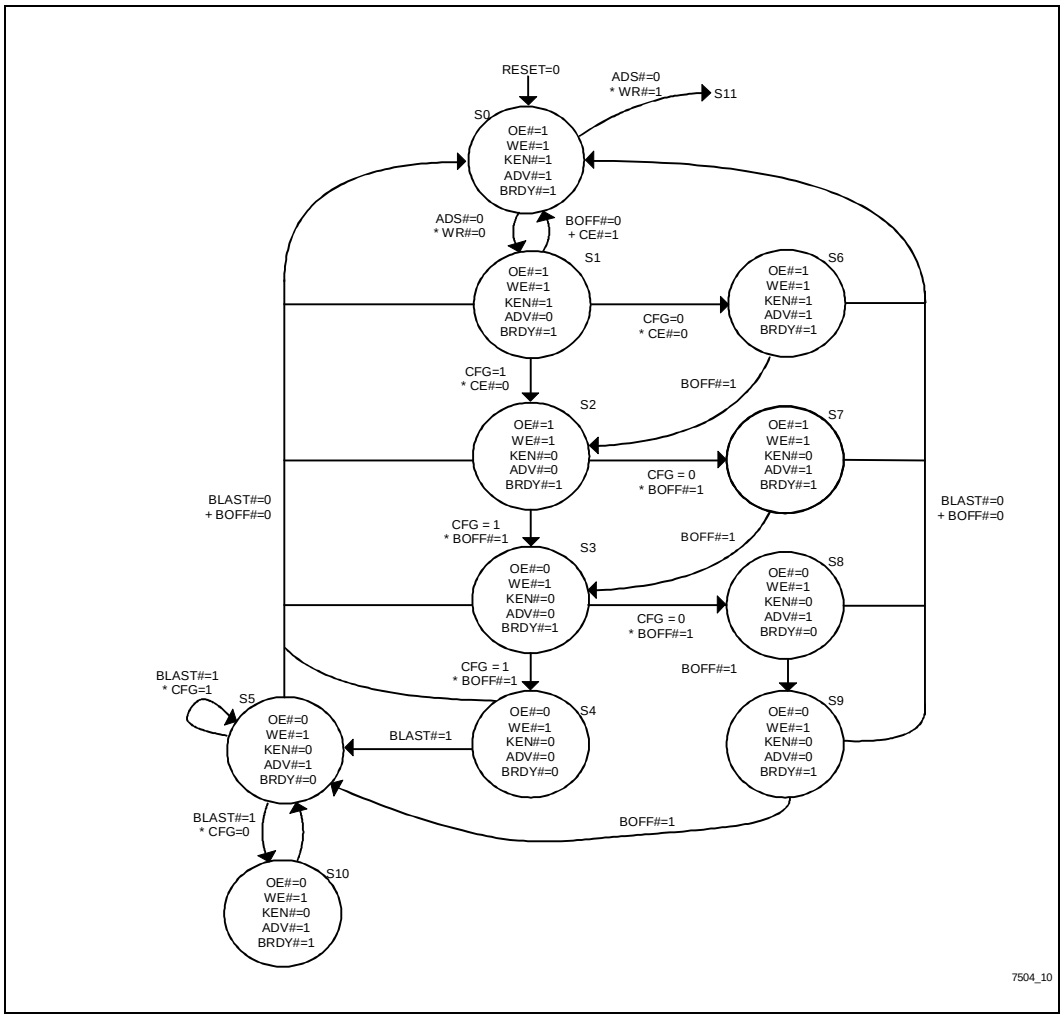

Figure 10. State Diagram of Single and Burst Read Control (Interface Shown in Figure 9)

PRODUCT PREVIEW

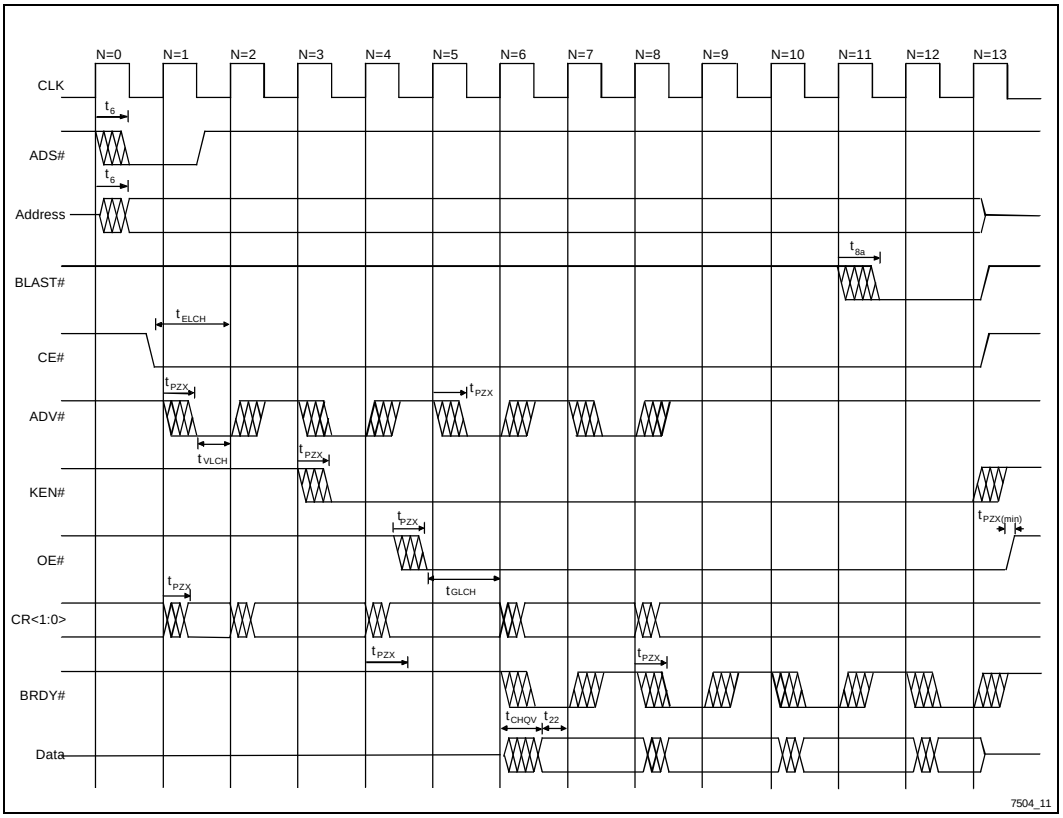

Figure 11. Example Initial Burst Read Cycle Showing Key Timing Specifications Requiring Consideration

Table 5. Example Initial Read Cycle Timing Specifications at 5V V_{CC}

Symbol	Description	Min	Max	Unit
t_6	ADS# Delay (Intel486™ SX-33 microprocessor)	3	16	ns
t_{16}	RDY# Setup Time (Intel486 SX-33 microprocessor)	5		ns
t_{22}	D_{31-0} Setup Time (Intel486 SX-33 microprocessor)	5		ns
t_{ELCH}	CE_X# Setup Time to CLK (28F016XS-15)	25		ns
t_{VLCH}	ADV# Setup Time to CLK (28F016XS-15)	15		ns
t_{GLCH}	OE# Setup Time to CLK (28F016XS-15)	15		ns
t_{CHQV}	CLK to Data Delay (28F016XS-15)		20	ns
t_{PZX}	CLK Output Delay (22V10-15)	2	8	ns

NOTE:
Consult appropriate datasheets for up-to-date specifications.

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Optimized Configuration

Refer to Figures 10 and 12 for the following discussion.

With the 28F016XS-15s in the optimized configuration (SFI Configuration = 2 at 33 MHz), and CFG set to a logic "1" value, the system interface executes cacheable burst cycles.

The Intel486 SX processor drives ADS# low, notifying the interface logic that a valid address is on the address bus. Monitoring the external bus of the Intel486 SX microprocessor, the state machine then transitions into read control.

If ADS# = 0 and W/R# = 0 then READ CONTROL

In optimized read control, the state machine controls OE#, KEN# and BRDY#. If CE# = "0," the state machine at N = 1 loads the two-bit counter (A_{3-2}) and activates ADV# (ADV# = "0") for the next four consecutive clock periods (N = 1 through 5). While ADV# is driven low, the counter increments through the Intel burst order (Table 2), supplying the 28F016XS-15s with a new address at N = 2, 3, 4 and 5. If CE# = "1," the state machine returns to an idle state waiting for a new memory access.

With the SFI Configuration value set to 2, new data will be available at N = 5, 6, 7 and 8. Driving BRDY# low at N = 4, the Intel486 SX microprocessor will sample BRDY# active at N = 5, which informs the processor of valid information on data pins D_{31-0} and that the 28F016XS memory space supports a burst read transfer. BRDY# is held low until the end of the burst cycle while the processor retrieves data on every rising clock edge. BRDY# is driven high upon sampling BLAST# low, marking the end of the burst cycle.

The Intel486 SX microprocessor requires a 3 ns hold time after sampling the last BRDY# active in a burst cycle. Therefore, the state machine will hold OE# active for 15 ns after the microprocessor samples the last double-word. At N = 9, the state machine transitions to an idle state, where it deactivates OE# and waits for the Intel486 SX microprocessor to initiate a new bus cycle targeting the 28F016XS memory space.

Optimized Configuration Timing Considerations

In the optimized configuration, CE# setup time is again a key system timing parameter. For information regarding the CE# setup time requirement, see the Initial Configuration Timing Considerations Timing section.

PRODUCT PREVIEW

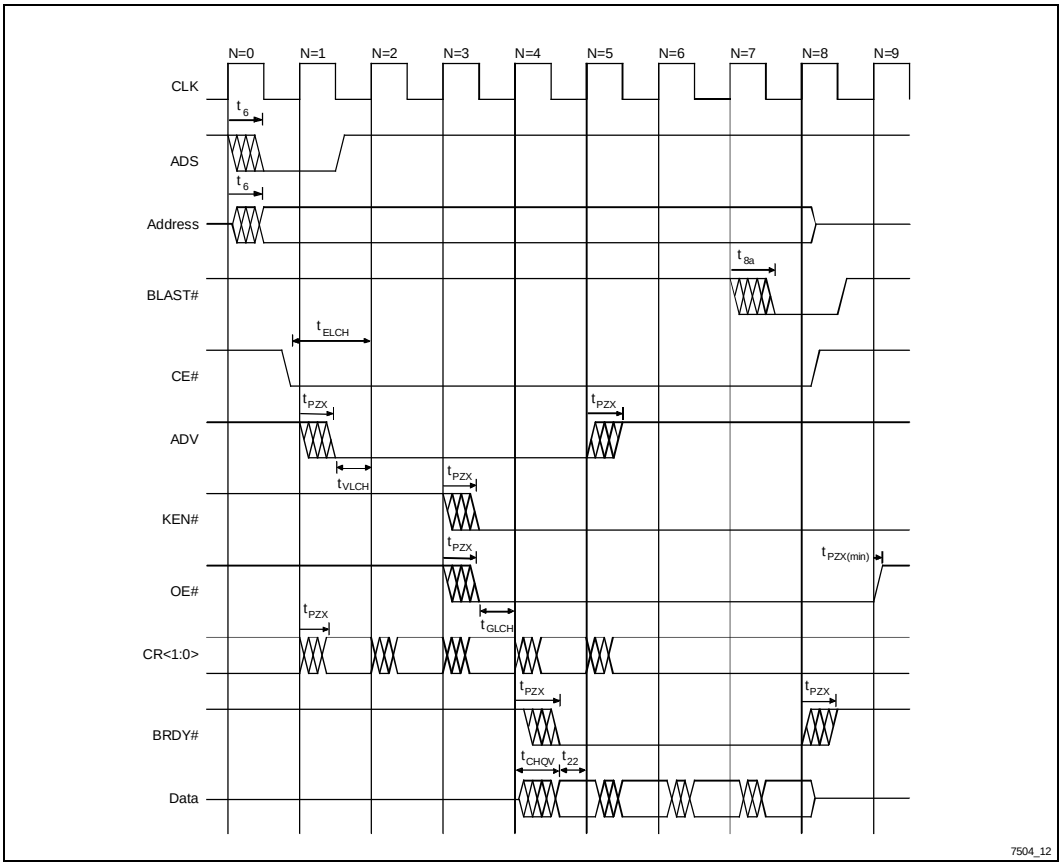

Figure 12. Example Burst Read Cycle Showing Key Timing Specifications Requiring Consideration

Table 6. Example Optimized Read Cycle Specifications at 5V V_{CC}

Symbol	Description	Min	Max	Unit
t_6	ADS# Delay (Intel486™ SX-33 microprocessor)	3	16	ns
t_{8a}	BLAST# Delay (Intel486 SX-33 microprocessor)	3	20	ns
t_{22}	D_{31-0} Setup Time (Intel486 SX-33 microprocessor)	5		ns
t_{ELCH}	CE_X# Setup Time to CLK (28F016XS-15)	25		ns
t_{VLCH}	ADV# Setup Time to CLK (28F016XS-15)	15		ns
t_{GLCH}	OE# Setup Time to CLK (28F016XS-15)	15		ns
t_{CHQV}	CLK to Data Delay (28F016XS-15)		20	ns
t_{PZX}	CLK Output Delay (22V10-15)	2	8	ns

NOTE:
Consult appropriate datasheets for up-to-date specifications.

PRODUCT PREVIEW

3.3 Write Cycle Control

The write interface in for this design functionally behaves like the optimized design's write interface. The only difference between the two designs is the absence of the MUX in the standard interface. Therefore, the interface logic for this design does not have to concern itself with changing the data flow through the MUX. Instead, the interface simply loads and holds the address for the duration of the write operation.

For further detailed information about this cycle and write timing waveform, refer to Section 2.5.

4.0 INTERFACING TO OTHER INTEL486™ MICROPROCESSORS

The Intel486 microprocessor family provides designers a large and diverse selection of CPUs, which offers designers different performance points to meet different market segment needs. Throughout the product family, the external bus architecture has remained consistent, which makes the 28F016XS interface to the entire Intel486 microprocessor family similar, if not identical, to the Intel486 SX microprocessor interface described in Sections 2 and 3. The 28F016XS-15 interface to the Intel486 SX-33 microprocessor works equally well for the following microprocessors at 5.0V V_{CC}.

- Intel486™ SX-20, -25 processors
- Intel486™ SX2-50 processor
- Intel486™ DX-25, -33 processors
- Intel486™ DX2-40, -50, -66 processors
- IntelDX4™-75, -100 processors(I/O buffers configured for 5.0V, V_{CC5} = 5.0V)

The 28F016XS-15 interface to the Intel486 SX-33 microprocessor also works well for the following Intel486 microprocessors at 3.3V V_{CC}. The 3.3V V_{CC} design utilizes a 22V10-15 low voltage PLD to control the interface between the 28F016XS-15 (operating at 3.3V V_{CC}) and the processor.

- Intel486 SX-20, -25 processors
- Intel486 DX-25 processor
- Intel486 DX2-40, -50 processors
- IntelDX4-75 processors (I/O buffers configured for 3.3V, V_{CC5} = 3.3V)

When the external bus frequency falls outside the 16.7 MHz through 33 MHz frequency range at 5.0V V_{CC} (12.5 MHz through 25 MHz at 3.3V V_{CC}), the optimized SFI Configuration value for the 28F016XS-15 differs in respect to the Intel486 SX-33 microprocessor design documented earlier. The state machine, therefore, requires slight modifications to accommodate the different SFI Configuration. Note, the initial read configuration and write control state machine remains consistent throughout all designs because they are not affected by the optimized SFI Configuration.

Intel486™ SX-16 Microprocessor Interface at 5.0V V_{CC}

The 28F016XS-15's optimized SFI Configuration at 16 MHz equals 1. Therefore, 28F016XS-15 will begin driving data one CLK period after initiating the first read access. The optimized state machine must drive BRDY# and OE# active upon initiating the first access to the 28F016XS-15. BRDY# and OE# remain low throughout the burst cycle. The optimized and standard 28F016XS-15 interface to the Intel486 SX-16 microprocessor at this specific frequency deliver 1-0-0-0 and 2-0-0-0 wait-state read performance respectively.

Intel486™ DX-50 Microprocessor Interface at 5V V_{CC}

Operating at 50 MHz, the 28F016XS-15's optimized SFI Configuration equals 3. The interface loads the two-bit counter and drives ADV# active at the first rising CLK edge after the processor initiates the read access. The optimized read state machine increments the two-bit counter and drives ADV# low every other CLK, thereby adhering to the *Alternating-A_1* and *Same-A_1* access rules (see Additional Information). The optimized and standard 28F016XS-15 interface to the Intel486 DX-50 microprocessor at this given frequency deliver 4-1-1-1 and 5-1-1-1 wait-state read performance respectively.

Intel486™ DX-33 and IntelDX4-100 Microprocessor Interface at 3.3V V_{CC}

Operating at 33 MHz with 3.3V V_{CC}, the 28F016XS-15's optimized SFI Configuration equals 3. The interface loads the two-bit counter and drives ADV# active at the first rising CLK edge after the processor initiates the read access. The optimized read state machine increments the two-bit counter and drives

ADV# low for two CLK periods and then strobes ADV# high for one CLK period. ADV# is again driven low for two CLK periods finishing the burst cycle. Refer to the *Alternating-A_1* and *Same-A_1* access rules (see Additional Information) for further information on consecutive accesses. The optimized and standard 28F016XS-15 interface to the Intel486 microprocessor at this frequency deliver 3-0-1-0 and 4-0-1-0 wait-state read performance respectively.

5.0 CONCLUSION

This technical paper has described the interface between the 28F016XS 16-Mbit flash memory component and the Intel486 microprocessor. This simple design has been implemented with a minimal number of components and achieves exceptional read performance. The 28F016XS provides the microprocessor with the nonvolatility and updateability of flash memory and the performance of DRAM. For further information about 28F016XS-15, consult reference documentation for a more comprehensive understanding of device capabilities and design techniques. Please contact your local Intel or distribution sales office for more information on Intel's flash memory products.

ADDITIONAL INFORMATION

Order Number	Document/Tools
290532	28F016XS 16-Mbit (1 Mbit x 16, 2 Mbit x 8) Synchronous Flash Memory Datasheet
297500	"Interfacing the 28F016XS to the i960 ® Microprocessor Family" (Technical Paper)
292147	AP-398, "Designing with the 28F016XS"
292146	AP-600, "Performance Benefits and Power/Energy Savings of 28F016XS-Based System Designs"
292163	AP-610, "Flash Memory In-System Code and Data Update Techniques"
292165	AB-62, "Compiled Code Optimizations for Flash Memories"
297372	16-Mbit Flash Product Family User's Manual,
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XS Benchmark Utility
Contact Intel/Distribution Sales Office	28F016XS iBIS Models
Contact Intel/Distribution Sales Office	28F016XS VHDL Models
Contact Intel/Distribution Sales Office	28F016XS Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016XS Orcad and ViewLogic Schematic Symbols

REVISION HISTORY

Number	Description
001	Original Version
002	Incorporated initial read burst configuration, replacing the single read cycle Added optimized design, improving system read performance
003	Added 3/5# pin reference to text and block diagrams (Figures 1 and 9) Revised state diagram numbering (Figures 4 and 7) General cosmedic changes

PRODUCT PREVIEW

APPENDIX A
PLD FILE FOR THE 28F016XS INTEL486™ MICROPROCESSOR INTERFACE

PLD file for the optimized interface described in Section 2.

```
TITLE                   Optimized 28F016XS / 486 Interface
PATTERN                 PDS
REVISION                1
AUTHOR                  Example
COMPANY NAME            Intel
DATE                    2/6/95

CHIP  OPTIMIZED_28F016XS_486_INTERFACE 85C22V10

; input pins
PIN    1     CLK            ; clk frequency 33mhz
PIN          ADS            ; address strobe from 486
PIN          WR             ; multiplexed read/write strobe
PIN          BLAST          ; BLAST from the 486
PIN          CE             ; CE from the address decoding logic
PIN          CFG            ; informs interface to changes to the SFI Configuration
PIN          A2             ; lower address lines from the 486 used
PIN          A3             ; in loading the counter
PIN          RESET          ; system reset
PIN    25    GLOBAL
; output pins
PIN          ADV            ; address valid input
PIN          /KEN           ; cache control
PIN          /OE            ; output enable input
PIN          /WE            ; write enable input
PIN          /BRDY          ; initiating a burst cycle, 486 input
PIN          SWITCH         ; control MUX switching
PIN          Q0             ; state variable
PIN          CTR0           ; lower bit of the 2bit counter
PIN          CTR1           ; higher bit of the 2bit counter

STRING  LD '(/ADS)'         ; load
STRING  INC '(/ADV)'        ; increment

STATE MOORE_MACHINE
DEFAULT_BRANCH S0

; state assignments
S0  = /ADV * /BRDY * /OE * /WE * /KEN * /SWITCH * /Q0
S1  = /ADV * /BRDY * /OE * /WE * /KEN *  SWITCH * /Q0
S2  = /ADV * /BRDY *  OE * /WE *  KEN *  SWITCH * /Q0
S3  = /ADV *  BRDY *  OE * /WE *  KEN *  SWITCH * /Q0
S4  =  ADV *  BRDY *  OE * /WE *  KEN *  SWITCH * /Q0
S5  =  ADV * /BRDY *  OE * /WE *  KEN *  SWITCH * /Q0
```

PRODUCT PREVIEW

```
S6  =  ADV * /BRDY * /OE * /WE * /KEN *  SWITCH *  Q0
S7  =  ADV * /BRDY * /OE * /WE *  KEN *  SWITCH *  Q0
S8  =  ADV *  BRDY *  OE * /WE *  KEN *  SWITCH *  Q0
S9  = /ADV * /BRDY *  OE * /WE *  KEN *  SWITCH *  Q0
S10 =  ADV * /BRDY * /OE * /WE * /KEN *  SWITCH * /Q0
S11 =  ADV * /BRDY * /OE *  WE * /KEN *  SWITCH * /Q0
S12 =  ADV * /BRDY * /OE *  WE * /KEN *  SWITCH *  Q0
S13 =  ADV *  BRDY * /OE * /WE * /KEN *  SWITCH * /Q0

; state transitions
S0 :=   (/ADS * /WR * /CFG)              -> S6   ; initial config READ cycle
   +   (/ADS * /WR *  CFG)               -> S1   ; optimized config READ cycle
   +   (/ADS *  WR)                      -> S10
                                        +-> S0
S1 :=   (/CFG * /CE *  BOFF)             -> S7
   +   ( CFG * /CE *  BOFF)              -> S2
   +    CE * /BOFF                      -> S0
S2 :=    /CFG * BOFF          -> S8
   +    CFG * BOFF                      -> S3
                                       +-> S0
S3 :=    /BLAST + /BOFF                  -> S0
   +    BLAST                           -> S4
S4 :=    /BLAST + /BOFF                  -> S0
   +   ( BLAST * /CFG)        -> S5
   +   ( BLAST *  CFG)        -> S4
S5 :=     BOFF                           -> S4
   +    /BOFF                           -> S0
S6 :=     BOFF                           -> S1
   +    /BOFF                           -> S0
S7 :=     BOFF                           -> S2
   +    /BOFF                           -> S0
S8 :=    /BLAST + /BOFF                  -> S0
   +    BLAST                           -> S9
S9 :=     BOFF                           -> S4
   +    /BOFF                           -> S0
S10:=    /CE                             -> S11  ; write cycle
   +    CE + /BOFF                      -> S0
S11:=     BOFF                           -> S12  ; WE low for two clocks
   +    /BOFF                           -> S0
S12:=     BOFF                           -> S13
   +    /BOFF                           -> S0
S13:=     VCC                            -> S0   ; ready

EQUATIONS
 ; implement RESET
   GLOBAL.RSTF = /RESET
 ; implement 2-bit burst counter
   CTR1 := (LD * A3) + (/LD * INC * /CTR1 * S1)
        + (/LD * INC * CTR1 * /S1) + (/LD * /INC * CTR1 * /S1)
   CTR0 := (/WR * LD * /A2) + (WR * LD * A2)
        + (/LD * INC * /CTR0) + (/LD * /INC * CTR0)
```

PRODUCT PREVIEW

PLD file for the standard interface described in Section 3.

```
Title           Standard 28F016XS / Intel486™ Interface
Pattern         PDS
Revision        1
Author          Example
Company Name    Intel
Date            2/14/94

CHIP   28F016XS_486_Interface   85C22V10   ; 85C22V10-15

; input pins
PIN    1     CLK          ; clk frequency 33mhz
PIN          ADS          ; address strobe from 486
PIN          WR           ; multiplexed read/write strobe
PIN          BLAST        ; BLAST from the 486
PIN          CE           ; CE from the address decoding logic
PIN          CFG          ; informs interface to changes to the SFI Configuration
PIN          BOFF; BOFF input to processor
PIN          A2           ; lower address lines from the 486 used
PIN          A3           ; in loading the counter
PIN          RESET        ; system reset
PIN    25    GLOBAL
;output pins
PIN          /ADV         ; address valid input
PIN          /KEN         ; cache control
PIN          /OE          ; output enable input
PIN          /WE          ; write enable input
PIN          /BRDY        ; initiating a burst cycle, 486 input
PIN          Q0           ; state variable
PIN          Q1           ; state variable
PIN          CONT0        ; lower bit of the 2bit counter
PIN          CONT1        ; higher bit of the 2bit counter

STRING  LD '(/ADS)'       ; load
STRING  INC '(/ADV)'

STATE MOORE_MACHINE
DEFAULT_BRANCH  S0
; state assignments
S0  = /ADV * /KEN * /WE * /BRDY * /Q0 * /Q1
S1  =  ADV * /KEN * /WE * /BRDY * /Q0 * /Q1
S2  =  ADV *  KEN * /WE * /BRDY * /Q0 * /Q1
S3  =  ADV *  KEN * /WE * /BRDY * /Q0 *  Q1
S4  =  ADV *  KEN * /WE *  BRDY * /Q0 * /Q1
S5  = /ADV *  KEN * /WE *  BRDY * /Q0 * /Q1
S6  = /ADV * /KEN * /WE * /BRDY * /Q0 *  Q1
S7  = /ADV *  KEN * /WE * /BRDY * /Q0 * /Q1
S8  = /ADV *  KEN * /WE * /BRDY * /Q0 *  Q1
S9  =  ADV *  KEN * /WE *  BRDY * /Q0 *  Q1
S10 = /ADV *  KEN * /WE * /BRDY *  Q0 *  Q1
S11 = /ADV * /KEN * /WE * /BRDY *  Q0 * /Q1
```

PRODUCT PREVIEW

```
S12 = /ADV * /KEN *  WE * /BRDY * /Q0 * /Q1
S13 = /ADV * /KEN *  WE * /BRDY * /Q0 *  Q1
S14 = /ADV * /KEN * /WE *  BRDY *  Q0 * /Q1

; state transitions
S0  :=  ADS * /BOFF          -> S0        ; start of an access
    + /ADS * /WR * /BOFF   -> S1
    + /ADS *  WR * /BOFF   -> S11
S1  := /CFG * /CE             -> S6        ; not reconfigured
    +  CFG * /CE              -> S2        ; reconfig active low
    +  CE                     -> S0
S2  := /CFG *  BOFF          -> S7        ; if chip enable is de-asserted,
    +  CFG *  BOFF           -> S3        ; quit the access and return
    + /BOFF                   -> S0
S3  := /CFG *  BOFF          -> S8
    +  CFG *  BOFF           -> S4
    + /BOFF                   -> S0
S4  := /BLAST + /BOFF       -> S0        ; situations will only ocur during
    +  BLAST                  -> S5        ; a BOFF.
S5  := /BLAST + /BOFF       -> S0        ; continous cycling until BLAST is
    + /CFG *  BLAST          -> S10       ; presented - end the burst cycle
    +  CFG *  BLAST          -> S5
S6  := /BOFF                  -> S0
    +  BOFF                   -> S2
S7  := /BOFF                  -> S0
    +  BOFF                   -> S3
S8  := /BOFF + /BLAST       -> S0
    +  BOFF                   -> S9
S9  := /BOFF                  -> S0
    +  BOFF                   -> S5
S10 := /BOFF                  -> S0
    +  BOFF                   -> S5
S11 := /CE                    -> S12       ; situation will only occur during
    +  CE + /BOFF             -> S0        ; during a BOFF.
S12 := /BOFF                  -> S0
    +  BOFF                   -> S13
S13 := /BOFF                  -> S0
    +  BOFF                   -> S14
S14 :=  VCC                   -> S0

EQUATIONS
 ; implement RESET
   GLOBAL.RSTF = /RESET
 ; implement 2-bit burst counter
   CTR1 := (LD * A3) + (/LD * INC * /CTR1 * S1)
        + (/LD * INC * CTR1 * /S2) + (/LD * /INC * CTR1 * /S2)
    CTR0 := (/WR * LD * A2) + (/LD * INC * /CTR0) + (/LD * /INC * CTR0)
 ; output enable control, triggered on falling clock edge
   OE := S2 + S3 + S4 + S5 + S7 + S8 + S9 + S10
   OE.CLKF = /CLK
```

PRODUCT PREVIEW

Filename:	297504_3.DOC
Directory:	C:\TESTDOCS\DOCS
Template:	C:\WORD\ZAN____1.DOT
Title:	486
Subject:	
Author:	Ken Mckee
Keywords:	
Comments:	
Creation Date:	09/01/95 11:29 AM
Revision Number:	7
Last Saved On:	01/12/96 9:47 AM
Last Saved By:	Ward McQueen
Total Editing Time:	54 Minutes
Last Printed On:	01/12/96 9:48 AM
As of Last Complete Printing	
Number of Pages:	28
Number of Words:	7,855 (approx.)
Number of Characters:	44,777 (approx.)