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TECHNICAL PAPER

Interfacing the 28F016XS to the i960® Microprocessor Family

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CONTENTS

1.0 INTRODUCTION

This technical paper describes several designs interfacing the high-performance 28F016XS flash memory to the i960® microprocessor family. All designs are based on preliminary 28F016XS specifications. Please contact your Intel or distribution sales office for up-to-date specifications before finalizing any design.

The 28F016XS is a 16-Mbit block erasable flash memory with a high-performance synchronous pipelined read interface. This optimized interface can sustain a high read transfer rate and makes the 28F016XS the ideal flash memory component when interfacing to a burst processor, such as the i960 microprocessor. The 28F016XS combines ROM-like nonvolatility, DRAM-like read performance and in-system updateability in one memory technology. These characteristics enable code execution directly from the 28F016XS, replacing the costly practice of shadowing code from HDD or ROM to DRAM for improved performance. With the 28F016XS, you can construct a high-performance, cost-effective system solution for use with a burst microprocessor.

The 28F016XS performs synchronous pipelined reads. Up to three accesses can be initiated before reading data output from the initial cycle. This synchronous pipelined structure makes it ideal for use with the i960 microprocessor. The 28F016XS takes full advantage of the processor's burst transfer mechanism, bringing significant system performance enhancements to an i960 microprocessor-based application. This technical paper describes processor-to-memory interfaces that exploit these capabilities to achieve maximum system performance. Figures 1 and 2 illustrate relative system performance enhancements that the 28F016XS brings to an i960 microprocessor-based environment, compared to other memory technologies. The benchmark parameters are documented in Appendix B.

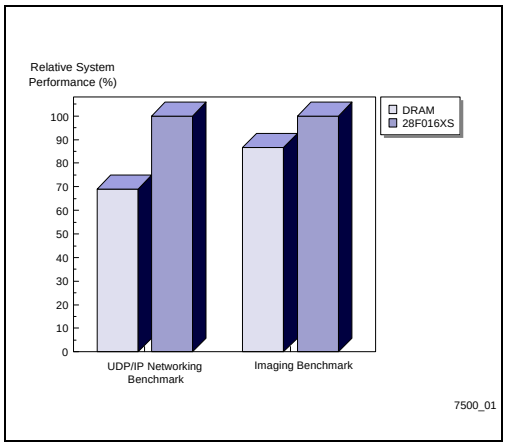


Figure 1. Relative System Performance of the 28F016XS Compared to Other Memory Technologies in an i960 KB-25 Microprocessor-Based Design

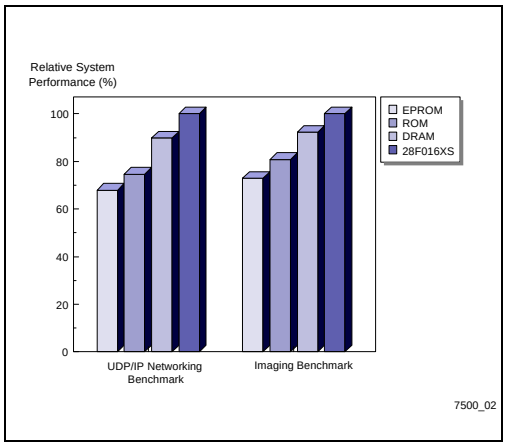


Figure 2. Relative System Performance of the 28F016XS Compared to Other Memory Technologies in an i960 CA-33 Processor-Based Design

2.0 i960 CA-33 MICROPROCESSOR INTERFACE

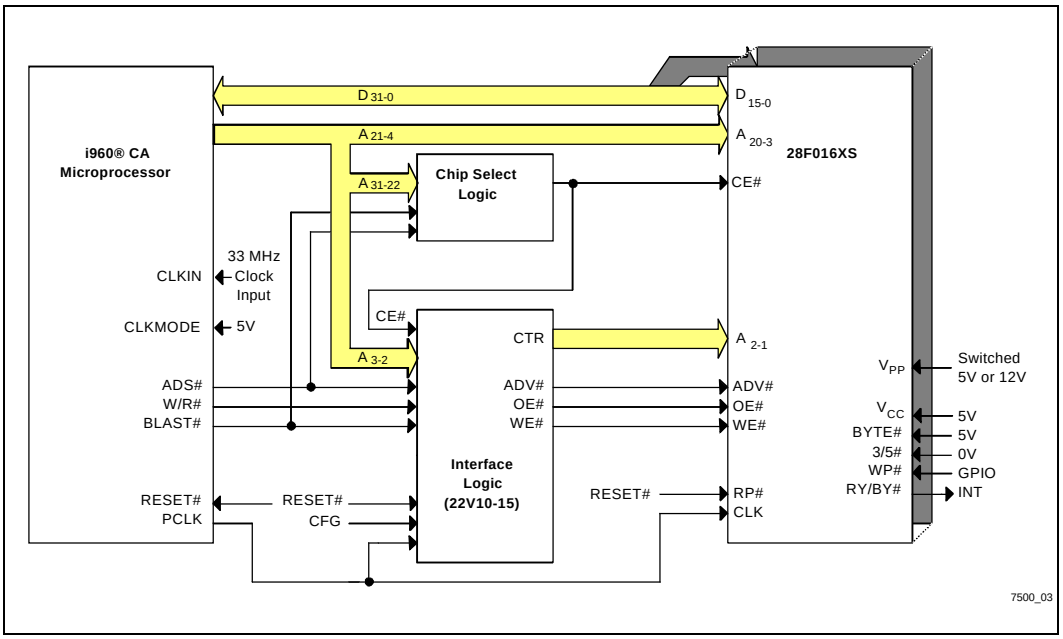


Figure 3. Minimal Logic Required in Interfacing the 28F016XS-15 to the i960 CA-33 Microprocessor to Sustain 3-0-0-0-2-0-0-0. . . Burst Pipelined Read Performance up to 33 MHz

Using this interface, an i960 CA-33 microprocessor-based system executing code directly out of the 28F016XS can achieve 3-0-0-0-2-0-0-0. . .wait-state read performance. This interface supports both burst transfers and address pipelining. For schematic and programmable logic device (PLD) files contact your Intel or distribution sales office.

2.1 Circuit Description

This section describes the 28F016XS-15 interface to the i960 CA-33 microprocessor. The block diagram for this design is illustrated in Figure 3.

Memory Configuration

This design uses two 28F016XS-15s, in x16 mode, to match the i960 CA microprocessor's 32-bit data bus, providing 4 Mbytes of flash memory. Signals $A_{21–4}$ from the i960 CA microprocessor and $CTR_{1–0}$ from the PLD select locations within the 28F016XS memory space, arranged as 1-Meg double words. A two-bit counter, implemented in the PLD, loads from the processor's lower addresses at the beginning of each memory cycle and generates subsequent burst addresses on outputs $CTR_{1–0}$. The counter feeds burst addresses to the 28F016XSs to prevent access stalling, while the devices wait for the processor to supply the next address.

Chip Select Logic

Chip select decode logic may use A_{31-22} to generate an active low chip select signal, CE#, for the 28F016XS-15 memory space and other system peripherals. The chip select drives CE_0# on each 28F016XS-15 and a control input to the PLD. The 28F016XS-15's CE_1# input is grounded.

In support of address pipelining, the chip select logic latches CE#, holding it active throughout the duration of the memory access. This will prevent potential CE# problems caused by using combinatorial logic when utilizing the address pipelining capability of i960 CA microprocessor.

If address pipelining functionality is not implemented, simple combinatorial logic can be utilized in generating the system CE# for the 28F016XS memory space, and the chip select logic shown in Figure 3 does not examine BLAST# and ADS#. For many systems using the upper address bits in a linear selection scheme may provide a sufficient number of chip select signals, thus eliminating system chip select decode logic. (See Figure 4 for an example of using linear selection for chip selects.) When using a linear chip select scheme however, the software must avoid using addresses that may select more than one device, which could result in bus contention.

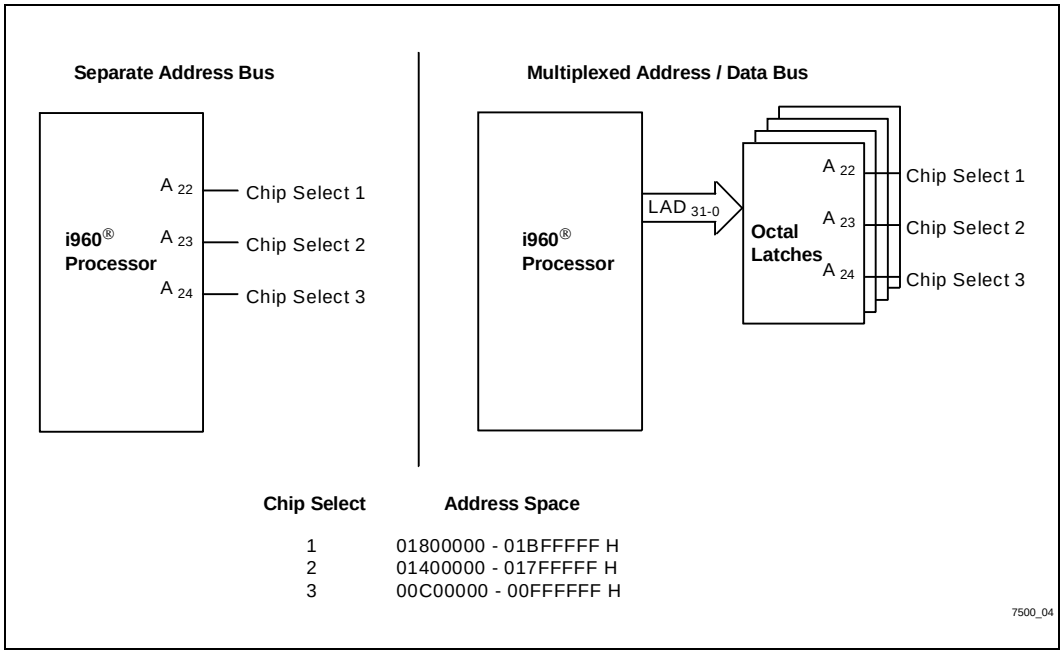


Figure 4. Example of Using Linear Chip Selection

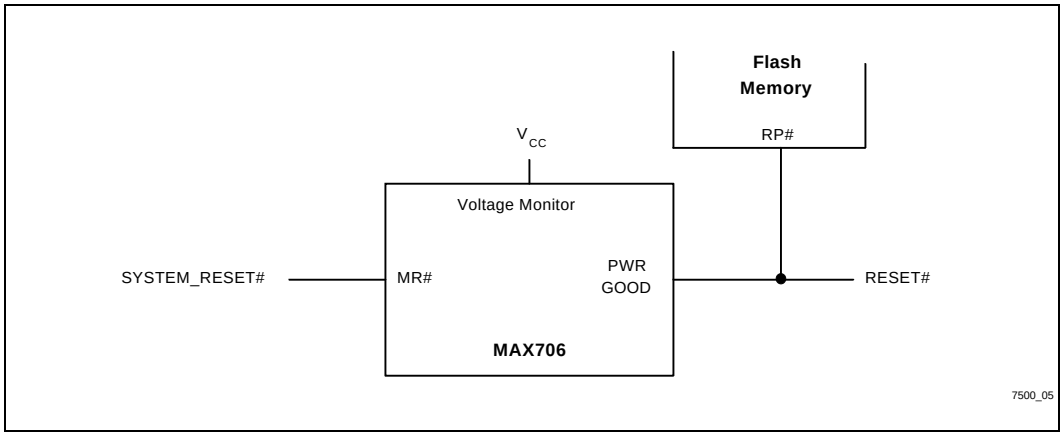


Figure 5. Example RESET Generation Circuitry

CLK Option

A 33 MHz clock signal drives the i960 CA microprocessor CLKIN input. Driving CLKMODE to a logic "1" configures the i960 CA microprocessor for a 1x CLK input. The i960 CA microprocessor outputs an internally-referenced 33 MHz clock on its PCLK1 and PCLK2 pins (the signals on PCLK1 and PCLK2 are identical), which drives the CLK inputs of the PLD and the 28F016XS-15s.

Reset

An active-low reset signal, RESET#, connects to the RESET# inputs of the i960 CA microprocessor, and PLD, and to the RP# input of the 28F016XS-15s. Figure 5 illustrates a suggested logic configuration for generating RESET#.

Interface Control Signals

The i960 CA-33 microprocessor external bus signals, BLAST#, ADS# and W/R#, serve as inputs to the state machine. The state machine controls the two-bit counter and generates OE#, WE# and ADV#. The counter is loaded at the beginning of the memory access, then generates the initial and subsequent burst addresses to the 28F016XS-15s. ADV# indicates that a valid address is available to the 28F016XS-15. Addresses are latched and a read cycle is initiated on rising CLK edges with ADV# active. During write operations, the 28F016XS-15s latch data on the rising edge of WE# if the applicable timing requirements are satisfied.

Configuration Signal

A general purpose input/output (GPIO) generates a configuration signal (CFG) input to the state machine. The configuration signal must reset to logic "0" on power-up and system reset to ensure that the operation of the state machine matches the initial configurations of the 28F016XS-15s and i960 CA microprocessor. After optimizing the 28F016XS-15s and i960 CA microprocessor, the system must drive CFG to a logic "1."

Additional 28F016XS Control Signals

The BYTE# input to the 28F016XS-15s is tied to 5.0V to configure the 28F016XS-15s for x16 mode, and A_0 and 3/5# inputs are tied to GND (A_0 is only used for byte addressing). A GPIO controls the write protect input, WP#, to the 28F016XS-15s. As shown in Figure 3, the 28F016XS-15 is compatible with either a 5.0V or a 12.0V V_{PP} voltage and is completely write protected by switching V_{PP} to GND. When V_{PP} drops below V_{PPLK}, the 28F016XS-15 will not complete program and erase operations successfully. Figure 3 also illustrates the RY/BY# output connected to a system interrupt for background erase operation. RY/BY#, WP#, and V_{PP} implementation are application dependent. See the Additional Information section of this technical paper for documentation that cover these topics in more detail.

2.2 Software Interface Considerations

Boot-Up Capability/Configuration

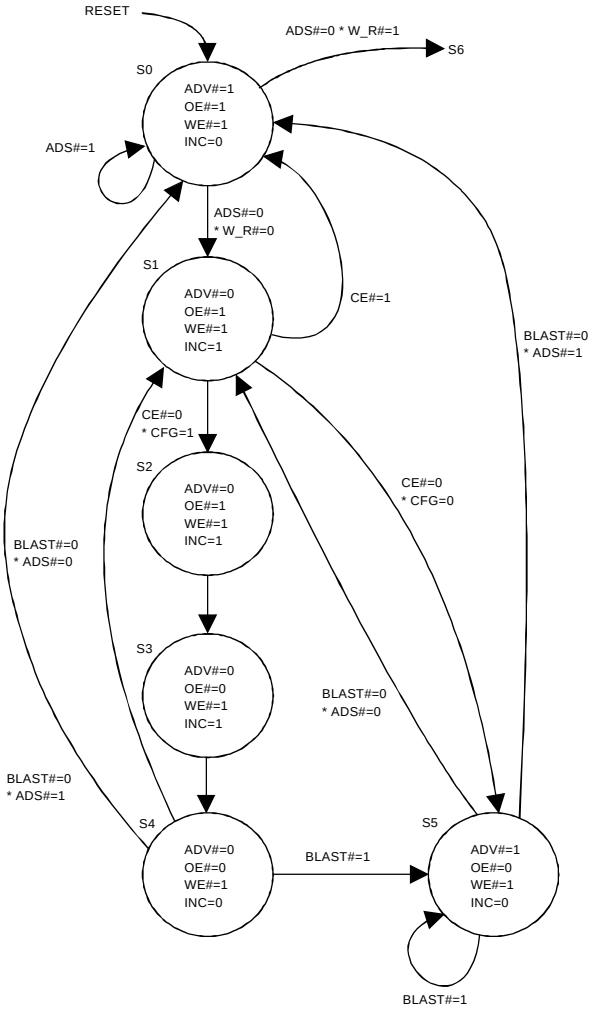
This interface supports processor boot-up from the 28F016XS memory space upon power-up or system reset. However, the boot code must follow some restrictions until it has properly configured the 28F016XS-15s, i960 CA microprocessor and CFG valve. In the default configuration state, the i960 CA microprocessor supports only non-burst reads and writes. Program control should jump to an area of RAM to execute the configuration sequence. The code will configure the 28F016XS-15s and all necessary i960 CA microprocessor programmable attributes before setting the CFG input to logic "1." Table 1 illustrates the required configuration settings for both the 28F016XS-15s and i960 CA-33 microprocessor.

Table 1. Configuration Settings for the 28F016XS-15 and i960 CA-33 Microprocessor Employing Address Pipelining at 33 MHz

Part	Parameter	Setting
28F016XS-15 (5V V_{CC})	SFI Configuration	2
i960 CA-33 Microprocessor	Ready Inputs	OFF
	Byte Ordering	LITTLE ENDIAN
	Bus Width	32-BIT
	Wait-States: Nrad	3
	Nrdd	0
	Nwad	2
	Nwdd	2
	Nxda	0
	Address Pipelining	ON
	Burst Mode	ON

2.3 Single and Burst Read Cycle Description at 33 MHz

Refer to the read cycle timing diagrams (Figures 7 and 8) and the state diagram (Figure 6) for the following read cycle discussion.



NOTE:
OE# and WE# are clocked on the inverted CLK edge

Figure 6. Read State Diagram of Single and Address Pipelined Burst Control Interface Shown in Figure 3

Initial Configuration

Figure 7 illustrates a read cycle with the 28F016XS-15s and i960 CA microprocessor in a power-up/reset configuration state. The initial configuration permits only non-burst transfers. The i960 CA microprocessor initiates a read cycle by asserting ADS# with W/R# = "0." At N = 1, the two-bit counter loads the values on the processor's lower address lines, A_{3-2}. The state machine asserts ADV# for the next clock (N = 2), where the 28F016XS-15 will latch in the address if CE# is asserted. If CE# is not asserted, the state machine returns to inactive state at N = 2.

If the flash memory is selected, the state machine will assert ADV# for only one clock before entering a hold state where it waits for the processor to assert BLAST#. The state machine asserts OE# (to meet timing requirements OE# is falling-edge triggered) on the falling edge between N = 2 and N = 3 to enable the 28F016XS-15 data output buffers. With SFI Configuration = 4, the data will be valid at the N = 7. The 28F016XS-15s will hold data on the bus until the i960 CA microprocessor asserts BLAST#. During the clock period following N = y, the state machine returns to its inactive state and de-asserts OE#, tri-stating the 28F016XS-15 data outputs.

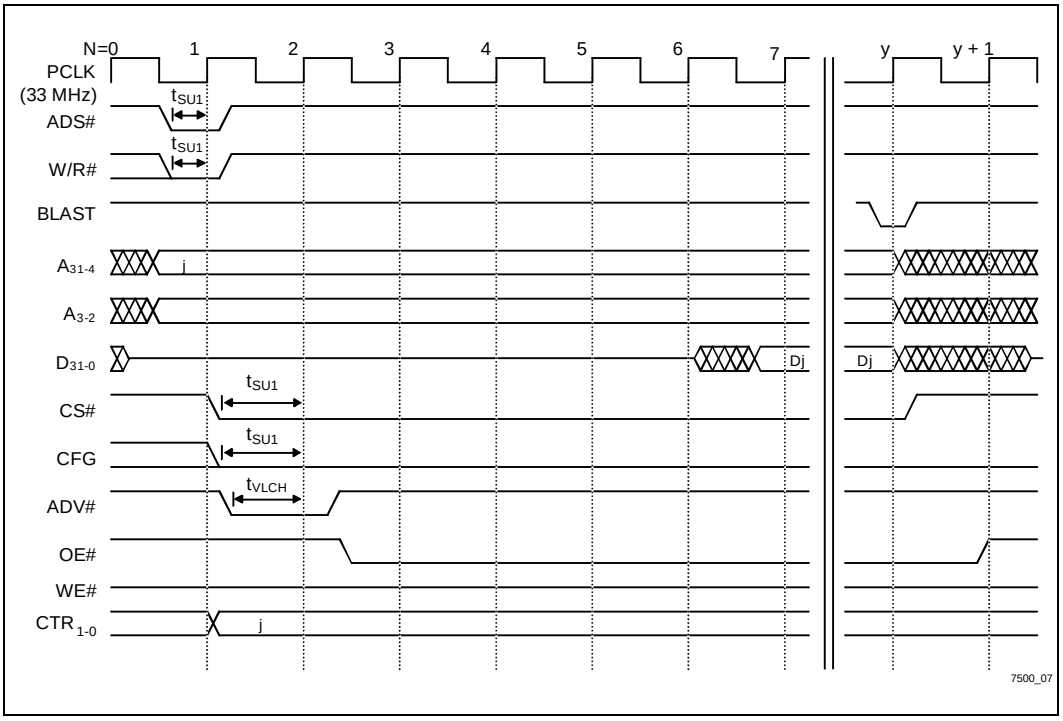


Figure 7. Example Read Cycle, Initial Configuration, Showing Key Specifications Requiring Consideration

Optimized Configuration

Figure 8 illustrates a two double-word burst read followed by a four double-word burst read with the 28F016XS-15s, i960 CA microprocessor and state machine configured for optimum read performance. With CFG = "1," the counter increments the two lower bits of the address at N = 2, N = 3 and N = 4, and ADV# remains asserted so that the 28F016XS-15 latches in four successive addresses at N = 2 through 5. With SFI Configuration = 2, the first data will be available at N = 5 for the processor to read. If a second read cycle follows the current read cycle, the i960 CA microprocessor will assert ADS# one clock after asserting BLAST#. The state machine will respond by immediately re-entering the read cycle. Otherwise, the state machine will return to its inactive state waiting for a new access targeting the 28F016XS memory space.

When implementing the i960 CA microprocessor address pipelining capability, the state machine controlling CE# monitors the upper address lines, ADS# and BLAST#. CE# is held active upon detecting an access targeting the flash memory space until BLAST# is asserted with ADS# de-asserted. When BLAST# and ADS# are active at the same time, a pipelined read access is in progress. If the current pipelined access targets the 28F016XS memory space, the CE# state machine will hold CE# active until BLAST# is sampled active again.

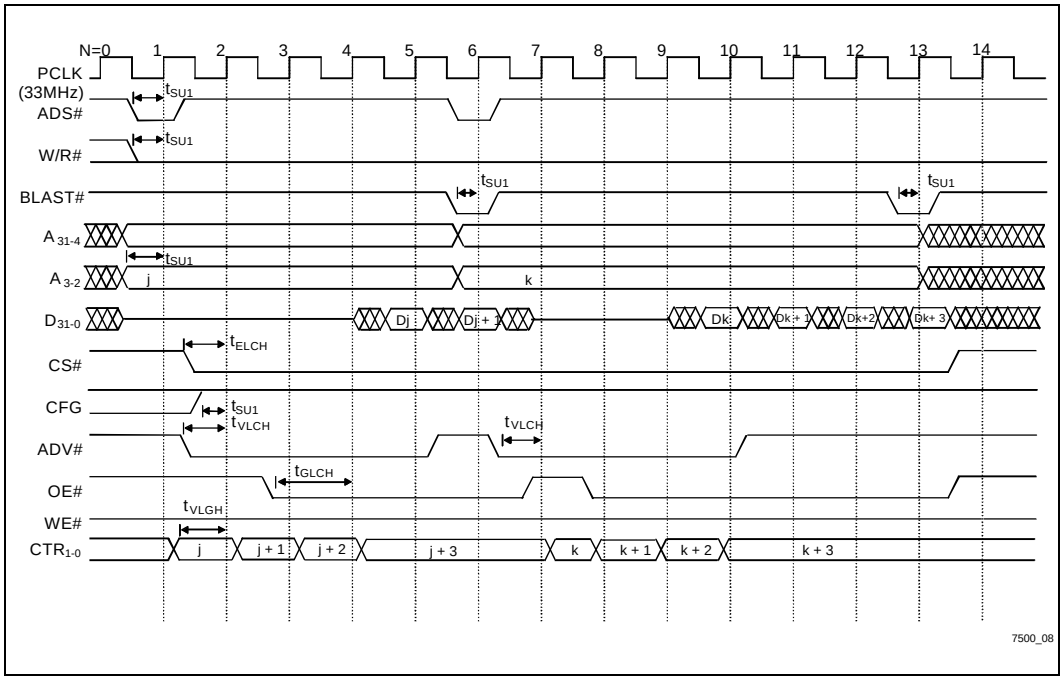


Figure 8. Example Two Double-Word Burst Read Followed by Pipelined Four Double Word Burst Read Showing Key Specifications Requiring Consideration

Critical Timings

Table 2 describes the critical timings illustrated in Figures 7 and 8. One such critical timing is the data hold time. The i960 CA-33 microprocessor requires a 5 ns hold time after the clock edge. The 28F016XS-15 guarantees a 5 ns data hold after clock, meeting the processor's hold requirement with 0 ns of margin.

This design provides 7 ns of margin to meet the 3 ns setup time of the i960 CA-33 microprocessor data inputs, outputting data t_{CHQV} after a rising CLK edge.

Another critical timing concerns CE# during pipelined read accesses. Since the 28F016XS-15 specifies zero data hold from CE# going high, the chip select state machine must hold CE# active for 5 ns to satisfy the i960 CA-33 microprocessor data input hold specification of 5 ns. Hence, the chip select state machine holds CE# active for an additional clock period after detecting BLAST# active.

The i960 CA-33 microprocessor control outputs ADS# and W/R# have 3 ns of margin and BLAST# has 5 ns of margin to meet the 22V10-15 input setup requirement.

Consult the appropriate datasheets for complete timing information.

Table 2. Example Read Cycle Timing Specifications at 5V V_{CC}

Part	Symbol	Parameter	Minimum Specified Value (ns)
22V10-15	t_{SU1}	Input Setup Time to CLK	9
i960 CA-33	T_{IS1}	Input Setup D_{31-0}	3
Microprocessor	T_{IH1}	Input Hold D_{31-0}	5
28F016XS-15	t_{ELCH}	CE# Setup to CLK	25
	t_{VLCH}	ADV# Setup to CLK	15
	t_{AVCH}	Address Setup to CLK	15
	t_{GLCH}	OE# Setup to CLK	15

NOTE:
Consult appropriate datasheets for up-to-date specifications.

2.4 Single and Burst Write Cycle Description at 33 MHz

Refer to the write cycle timing diagrams and the state diagram (Figure 9) for the following write cycle discussion.

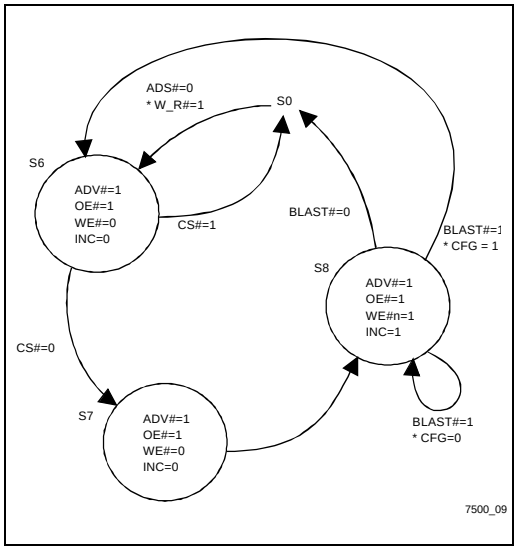


Figure 9. Write State Diagram for the Interface Logic Shown in Figure 3

Initial Configuration

Figure 10 illustrates a write cycle. In the reset/power-up configuration state, the interface supports only non-burst writes. The i960 CA microprocessor initiates a write cycle by asserting ADS# with W/R# = "1." At N = 1, the two-bit counter loads the values on address bits A_{3-2}. The state machine asserts WE# (to meet timing requirements, WE# is falling-edge triggered) on the falling edge between N = 1 and N = 2. WE# remains asserted for two clock periods, in order to meet the 28F016XS-15 timing requirements. The state machine then enters a holding state until the processor asserts BLAST#, after which time the interface state machine will return to an idle state.

Optimized Configuration

Figure 11 illustrates an optimized two double-word burst write cycle. When the first data write is completed at N = 4, the counter increments the two lower address bits, and the state machine asserts WE# on the next falling clock edge to begin the next the 28F016XS-15 data write. The i960 CA microprocessor must provide the next data during the clock period following N = 4. The data writes continue to the next consecutive addresses until the i960 CA microprocessor asserts BLAST#, indicating the end of the burst write cycle.

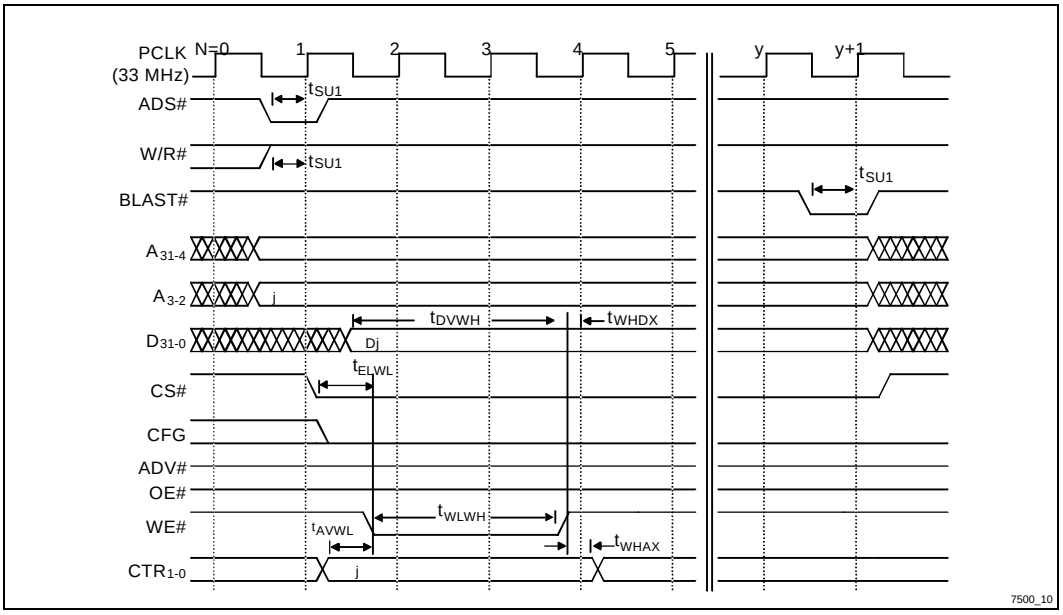


Figure 10. Example Write Cycle, Initial Configuration, Showing Key Specifications Requiring Consideration

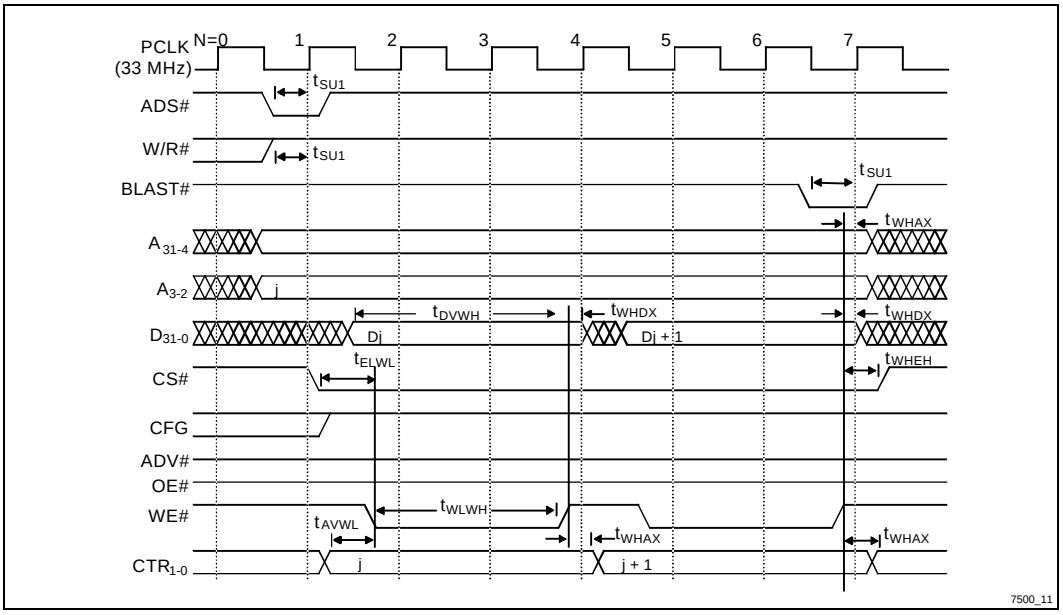


Figure 11. Example Two Double-Word Burst Write Illustrating Key Specifications Requiring Considerations

Critical Timings

Table 3 describes the critical timings illustrated in Figures 10 and 11.

One critical hold time to notice is t_{WHAX}. WE# is guaranteed to transition within 8 ns from the falling clock edge. Therefore, the t_{WHAX} requirement has 2 ns of margin for CTR_{1-0} and 5 ns of margin for A_{31-4} inputs.

Also notice that CTR_{1-0} must be valid before WE# is asserted. CTR_{1-0} are guaranteed valid 8 ns after the rising clock edge, providing 9 ns of margin.

Consult the appropriate datasheets for full timing information.

Table 3. Example Write Cycle Timing Parameters at 5V V_{CC}

Part	Symbol	Parameter	Minimum Specified Value (ns)
22V10-15	t_{SU1}	Input Setup Time to CLK	9
28F016XS-15	t_{ELWL}	CE# Setup to WE# Going Low	0
	t_{AVWL}	Address Setup to WE# Going Low	0
	t_{WLWH}	WE# Pulse Width	50
	t_{DVWH}	Data Setup to WE# Going High	50
	t_{WHDX}	Data Hold from WE# High	0
	t_{WHAX}	Address Hold from WE# High	5
	t_{WHEH}	CE# Hold from WE# High	5

NOTE:
Consult appropriate datasheets for up-to-date specifications.

3.0 Optimized i960 JF MICROPROCESSOR INTERFACE

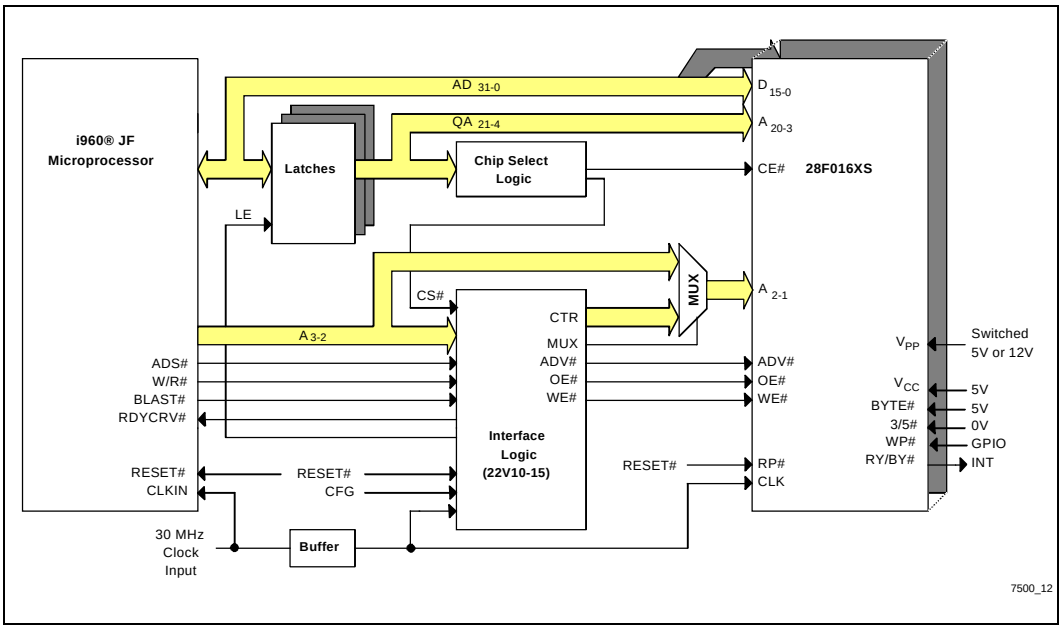


Figure 12. Minimal Interface Logic Required in Interfacing the 28F016XS-15 to the i960 JF-33 Microprocessor to Sustain 2-0-0-0 Burst Read Performance up to 30 MHz

Using this particular design, the 28F016XS interface to the i960 JF-33 microprocessor can achieve 2-0-0-0 wait-state read performance up to 30 MHz, supporting burst transfers. Contact your Intel or distribution sales office for schematic and PLD files for the design documented in the section.

See Section 4.0 for an alternative i960 JF design.

3.1 Circuit Description

This design, illustrated in Figure 12, uses two 28F016XS-15s to match the 32-bit data bus of the i960 JF-33 microprocessor. Four octal latches, enabled by the LE signal, de-multiplex the 32-bit address from the AD bus. The latched address bits $QA_{21–4}$ and the counter outputs $CTR_{1–0}$ from the PLD select locations within the 28F016XS memory space. A two-bit counter implemented in the PLD loads and increments the processor's lower address lines at the beginning of each memory cycle. The processor supplies the 28F016XS-15s with the initial address during a read transaction, and the counter provides the subsequent burst addresses for the remaining duration of the read transaction.

CLK Option

A 30 MHz clock signal drives the i960 JF microprocessor CLKIN input. The buffer delays the system CLK and drives the PLD and 28F016XS-15s. The buffer introduces an intentional system clock skew, which provides additional time for the processor to meet the 28F016XSs' address setup time on the initial memory access. At a slower operating frequency, this intentional delay may not be required to satisfy the 28F016XSs' address setup specification.

Multiplexer (MUX)

To achieve this wait-state profile, the processor loads the 28F016XSs with the initial address directly. The interface logic enables the MUX to permit the processor's lower address lines, $A_{3–2}$, access to the lower flash memory address lines during the initial access of a burst or single read transaction. Next, the interface logic switches the data flow path through the MUX. The integrated two-bit

counter then takes over, driving the 28F016XSs' A_{2-1} address inputs. The counter supplies the flash memory with consecutive burst addresses for the remaining duration of the read transaction.

Reset

An active-low reset signal, RESET#, drives the RESET# inputs of the i960 JF microprocessor and PLD and 28F016XS-15s. Figure 5 illustrates a suggested logic configuration for generating RESET#.

Interface Control Signals

The processor's ADS# and W/R# signals, just as in the i960 CA microprocessor design, serve as inputs to the state machine. The state machine controls an integrated two-bit counter and generates the OE#, WE# and ADV# signals for the 28F016XS-15s. The state machine also generates the RDYRCV# signal to the i960 JF microprocessor to control the wait-state profile.

Configuration Signal

A general purpose input/output (GPIO) generates the configuration signal (CFG) for input to the state machine. The configuration signal must be reset to logic "0" on power-up and system reset to ensure coherency between the state machine and 28F016XS-15s. After optimizing the 28F016XS-15s, the reconfiguration signal must switch to a logic "1" to take advantage of the new configuration.

Additional Control Signals

For information regarding 3/5#, BYTE#, WP#, RY/BY# and Vpp, see Section 2.1.

3.2 Software Interface Considerations

Boot-Up Capability

This interface supports processor boot-up from the 28F016XS-15 memory space after power-up or system reset. The initial system configuration will execute 4-1-1-1 wait-state read performance until the SFI Configuration is set to 2 and CFG input is set to logic "1." Program control should jump to an area of RAM to execute the configuration sequence. A pseudocode flow for this configuration sequence is shown below.

Execute Device Configuration command sequence
Activate CFG signal
End

The SFI Configuration must be set to 2 before the CFG input is set to logic "1." Thereafter, burst read wait-state performance will improve to 2-0-0-0.

3.3 Burst Read Cycle Description

Refer to the read cycle timing diagrams and state diagram (Figure 13) for the following discussions of the read cycle.

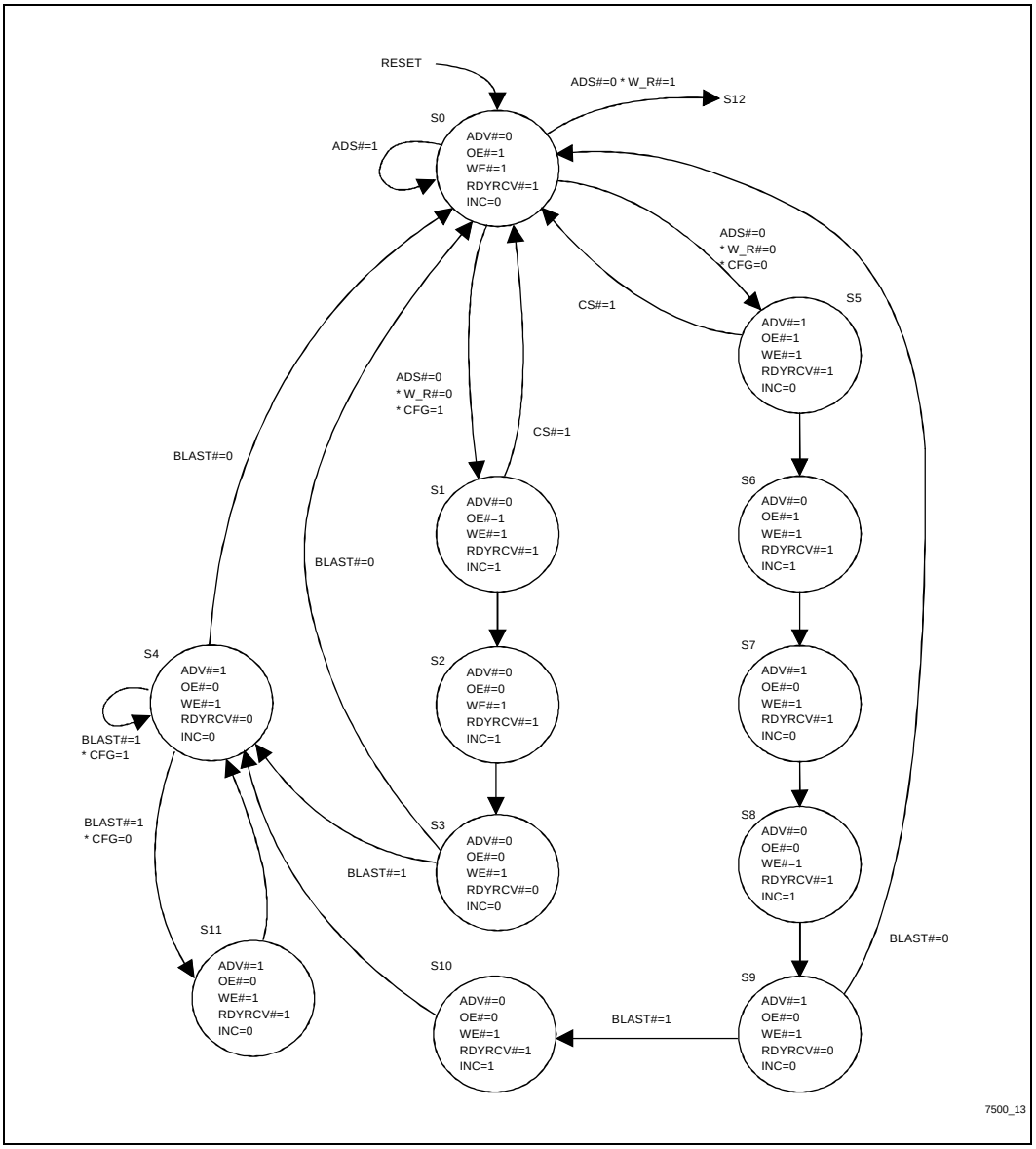


Figure 13. Read State Diagram of Burst Control Interface Shown in Figure 12

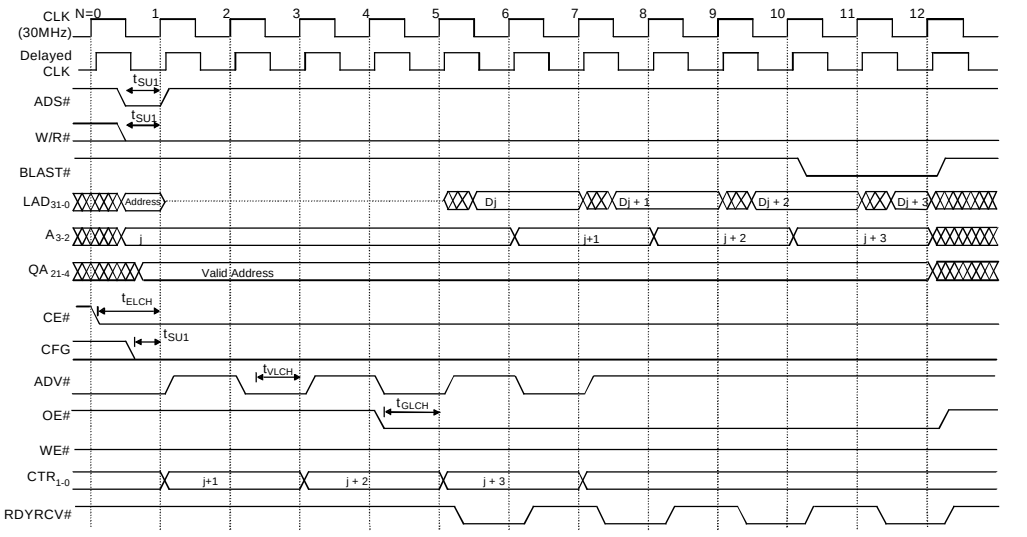


Figure 14. Example Four Double-Word Burst Read in Initial Configuration Showing Key Specifications Requiring Consideration

Initial Configuration

Figure 14 illustrates a four double-word burst read cycle with the 28F016XS-15s and state machine in a reset/power-up configuration state.

Initially, the interface logic drives LE, ADV# and MUX active while waiting for the processor to initiate a read cycle targeting the 28F016XSs. With the MUX active, the processor drives the lower flash memory address lines in anticipation of a flash memory access. During this anticipation state, CE# is active to prevent a t_{ELCH} violation on the first access initiated by the processor. The delayed CLK also prevents a possible timing violation from occurring by providing the processor with sufficient time to meet the 28F016XSs' t_{AVCH} specification.

When the i960 JF microprocessor initiates a read cycle by asserting ADS# with W/R# = "0," the state machine loads and increments the two-bit counter. The counter is incremented upon the initial load sequence because the processor supplies the flash memory with the initial address.

The state machine will de-assert ADV# at N = 1 and switches the data flow path through the MUX. The two-bit counter then drives the flash memory's lower address lines for the remaining duration of the read transaction. The state machine asserts ADV# at N = 3 to load the next read address into the 28F016XS-15s. De-asserting ADV# for one clock cycle (at N = 2, 4, 6 and 8) between accesses forces the 28F016XS-15s to hold data output for two clock cycles (access stretching), which allows time for the data to stabilize and meet the timing requirements of the i960 JF microprocessor bus.

While ADV# is asserted, the counter increments, providing the flash memory with successive burst addresses. The state machine asserts OE# at N = 4 to enable the 28F016XS-15 data output buffers. With the SFI Configuration = 4, the data will be valid at the i960 JF microprocessor data inputs at N = 6, 8, 10 and 12.

The state machine asserts RDYRCV# to inform the i960 JF microprocessor that data is valid. RDYRCV# is returned active at N = 6, 8, 10 and 12. Upon detecting BLAST# active, the interface will transition to its idle state where it waits for the start of a new bus cycle.

Optimized Configuration

Figure 15 illustrates a four double-word burst read with the 28F016XS-15s and state machine configured for optimum read performance. While the state machine waits for the i960 JF microprocessor to initiate a read cycle, ADV#, LE and MUX are held active providing the processor access to the flash memory's lower address lines.

After the first access is initiated at N = 1, ADV# is held active and the counter increments through the remaining burst sequence. Data from the initial access will be available at N = 4. Subsequent data will be valid at N = 5, 6 and 7. All other signal monitoring and generation is identical to the initial configuration read cycle documented in the preceding section.

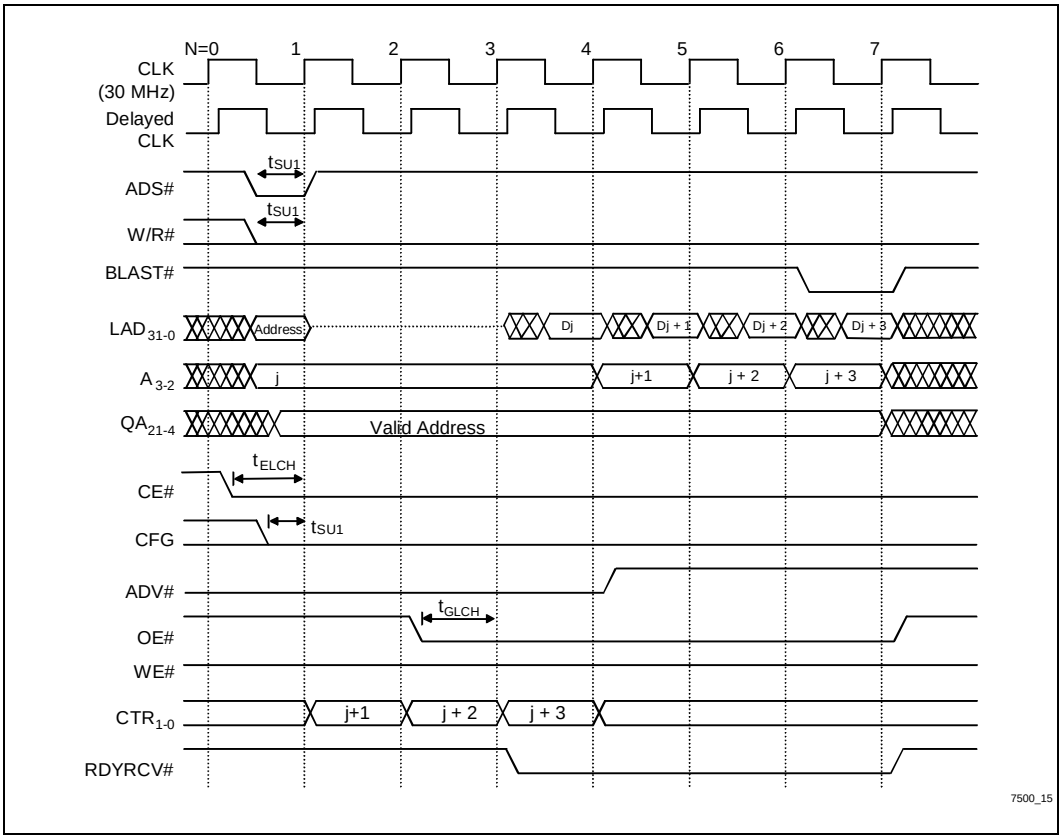


Figure 15. Example Four Double-Word Burst Read Illustrating Important Timing Parameters Requiring Consideration

Critical Timings

In these two configurations, there are some critical timings that need to be examined. Table 4 depicts these critical timings which are illustrated in Figures 14 and 15.

First, the buffer delay can cause timing violations if not chosen correctly. The purpose of the buffer is to provide sufficient time for the processor to load the 28F016XSs with the initial address during a read transaction. Therefore, the buffer must have a minimum delay that satisfies the flash memory's t_{AVCH}.

$$\text{Latch Delay} - t_{OV1} - t_{AVCH} - 1/\text{CLKIN} = \text{Buffer Delay}$$

As the previous equation illustrates, the minimum buffer delay is dependent upon several different variables: CLKIN frequency and latch delay. At a slow operation frequency, the interface does not require a buffer delay.

The buffer can also affect the processor's data setup time. Hence, the buffer must have a maximum delay of no greater than:

$$1/\text{CLKIN} - t_{CHQV} - t_{IS1} = \text{Buffer Delay}$$

Consult the appropriate datasheets for complete timing information.

Table 4. Example Read Cycle Timing Parameters at 5V V_{CC}

Part	Symbol	Parameter	Minimum Specified Value (ns)
Buffer	$t_{PHL,PLH}$	Buffer Delay	1.5
22V10-15	t_{SU1}	Input Setup Time to CLK	9
28F016XS-15	t_{ELCH}	CE# Setup to CLK	25
	t_{VLCH}	ADV# Setup to CLK	15
	t_{AVCH}	Address Setup to CLK	15
	t_{GLCH}	OE# Setup to CLK	15

NOTE:
Consult appropriate datasheets for up-to-date specifications.

3.4 Burst Write Cycle Description

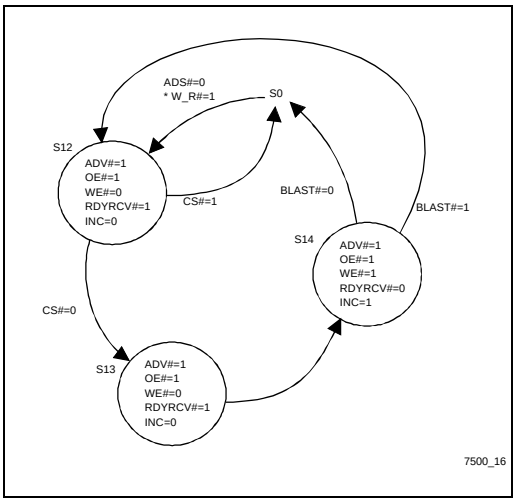


Figure 16. Write State Diagram of Burst Control Interface Shown in Figure 12

Write Configuration

Figure 17 illustrates a two double-word burst write cycle. The i960 JF microprocessor initiates a write cycle by asserting ADS# with W/R# = "1." When detecting a write operation, the state machine immediately switches the data flow path through the MUX. The counter is given sole control to drive the 28F016XSs' lower address lines. At N = 1 with ADS# = "0," the two-bit counter loads the values on the processor's lower address lines. The state machine asserts WE# (to meet timing requirements, WE# is falling-edge triggered) on the falling edge between N = 1 and N = 2. WE# remains asserted for four clock periods, in order to meet 28F016XS-15 timing requirements. The state machine asserts RDYRCV# for N = 4 to inform the i960 JF microprocessor to supply the next data. At N = 4, the counter increments the two lower address bits, and the state machine asserts WE# on the next falling clock edge to begin the next data write to the 28F016XS-15s. The data writes continue until the processor asserts BLAST#, noting the end of the current write transaction. The SFI Configuration has no effect on the write cycle.

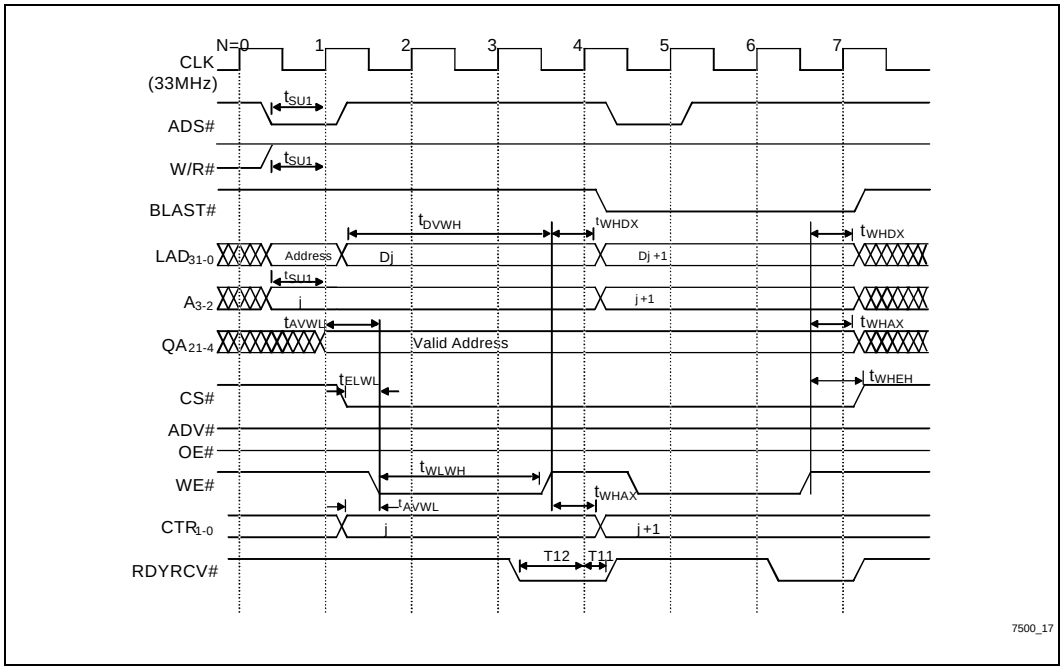


Figure 17. Two Double-Word Burst Write

Critical Timings

Table 5 describes the critical timings illustrated in Figure 17.

Notice that CTR_{1-0}, and CS# must be valid before WE# is asserted. CTR_{1-0} are guaranteed to be valid 8 ns after the rising clock edge, providing 12 ns of margin.

Consult the appropriate datasheets for full timing information.

Table 5. Example Write Cycle Timing Parameters at 5V V_{CC}

Part	Symbol	Parameter	Minimum Specified Value (ns)
22V10-15	t_{SU1}	Input Setup Time to CLK	9
28F016XS-15	t_{ELWL}	CE# Setup to WE# Going Low	0
	t_{AVWL}	Address Setup to WE# Going Low	0
	t_{WLWH}	WE# Pulse Width	50
	t_{DVWH}	Data Setup to WE# Going High	50
	t_{WHDX}	Data Hold from WE# High	0
	t_{WHAX}	Address Hold from WE# High	5
	t_{WHEH}	CE# Hold from WE# High	5

NOTES:
Consult appropriate datasheets for up-to-date specifications.

4.0 Standard i960 JF MICROPROCESSOR INTERFACE

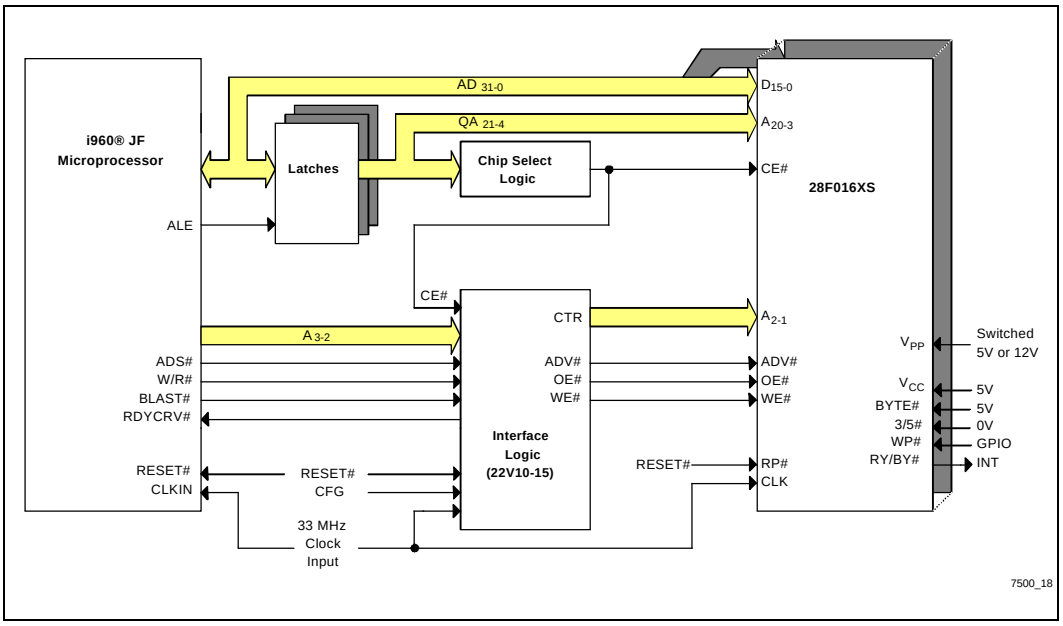


Figure 18. Minimal Interface Logic Required in Interfacing the 28F016XS-15 to the i960 JF-33 Microprocessor to Sustain 3-0-0-0 Burst Read Performance up to 33 MHz

The 28F016XS-15 interface to the i960 JF-33 microprocessor, illustrate in Figure 18, delivers 3-0-0-0 wait-state read performance up to 33 MHz. The design requires only one 22V10 to handle all interfacing requirements. Contact your Intel or distribution sales office for schematic and PLD files for the interface documented in this section.

See Section 3.0 for an alternative design.

4.1 Circuit Description

This interface is very similar to the optimized i960 JF design described in Section 3.0. This design however, eliminates the buffer and multiplexer requirement. For specific circuitry information involved in this standard interface, reference Section 3.0.

CLK Option

Unlike the optimized design in Section 3.0, a buffer is not implemented in this interface. The 33 MHz system clock drives the processor, PLD and flash memory. To reduce system clock skew, position the PLD and 28F016XSs within close proximity to the microprocessor.

4.2 Software Interface Considerations

This interface supports processor boot-up from the flash memory space after power-up or system reset. Initially, the read wait-state performance will be 5-1-1-1 until the SFI Configuration value is modified. The 28F016XS operates at optimal performance with a SFI Configuration value of 2 at 33 MHz. Program control should jump to an area of RAM to execute a configuration sequence which optimizes the flash memory and interface state machine for the given operating frequency.

4.3 Burst Read Cycle Description at 33 MHz

Refer to the read cycle timing diagrams and state diagram (Figure 19) for the following discussions of the read cycle.

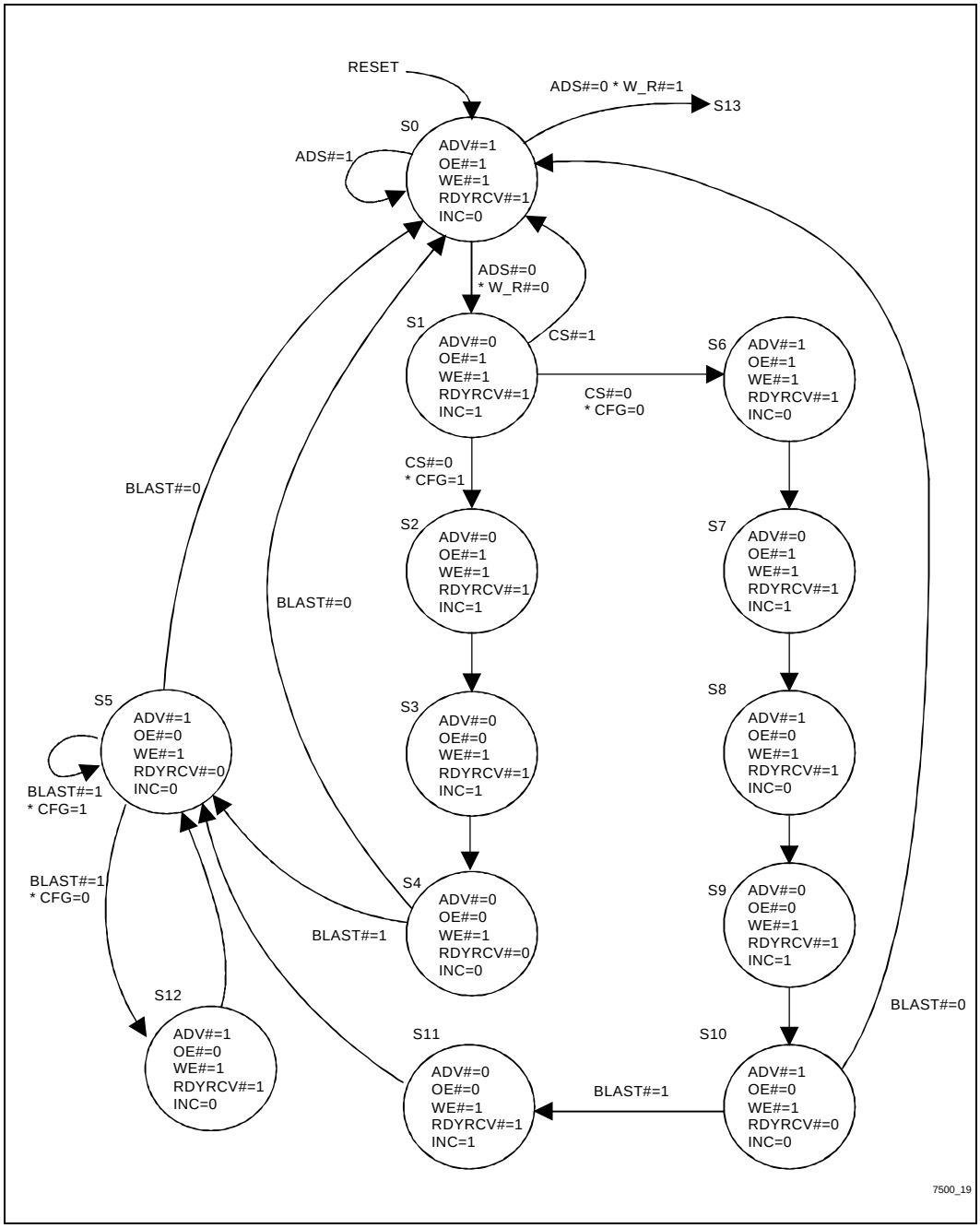


Figure 19. Read State Diagram of Burst Control Interface Shown in Figure 18

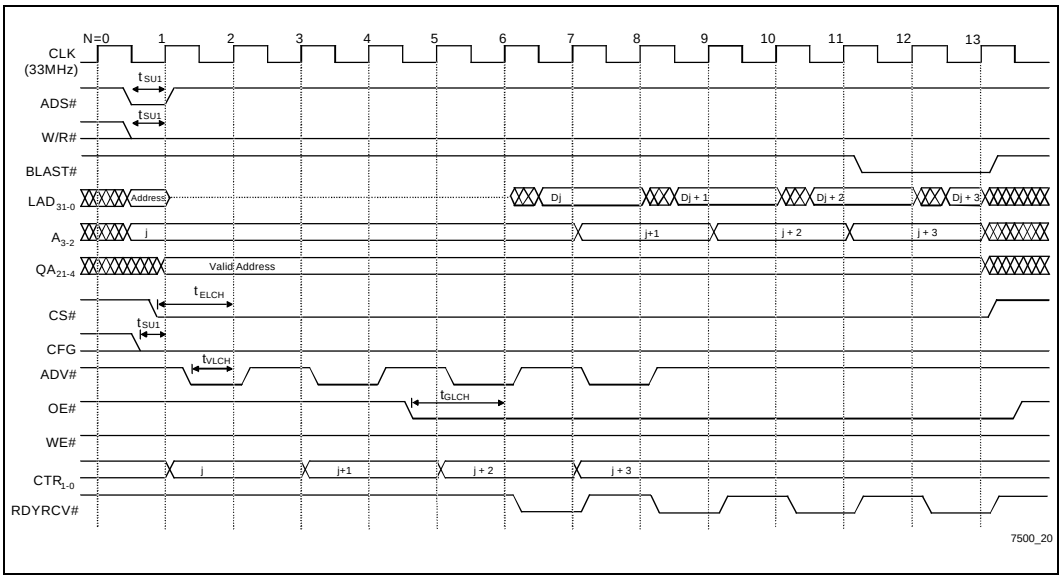


Figure 20. Example Four Double-Word Burst Read in Initial Configuration Showing Key Specifications Requiring Consideration

Initial Configuration

Figure 20 illustrates a four double-word burst read cycle with the 28F016XS-15s and the state machine in the reset/power-up configuration state. The i960 JF microprocessor initiates a read cycle by asserting ADS# with W/R# = "0." At N = 2 with ADS# = "0," the two-bit counter loads the values on address bits A_{3-2}.

The state machine asserts ADV# after clock edge N = 1. The 28F016XS-15s will latch the first address at the next rising clock edge (N=2), if CS# is asserted. If CS# is not asserted, the state machine will return to its inactive state at N = 2.

The state machine de-asserts ADV# at N = 2. The state machine then asserts ADV# at N = 3 to load the next read address into the 28F016XS-15s. De-asserting ADV# for one clock cycle (at N = 2, 4, 6 and 8) between accesses forces the 28F016XS-15s to hold data output for two clock cycles (access stretching), which allows time for the data to stabilize and meet the timing requirements of the i960 JF microprocessor.

The counter increments the two lower bits of the address at N = 3, 5 and 7 to provide the four successive burst addresses. The state machine asserts OE# at N = 4 to enable the 28F016XS-15 data output buffers. With the SFI Configuration = 4, the data will be valid at the i960 JF microprocessor data inputs at N = 7.

The state machine asserts RDYRCV# to inform the i960 JF microprocessor that data is valid. RDYRCV# is returned active at N = 7, 9, 11 and 12. When sampling BLAST# active, the state machine ends the read transfer and returns to an idle state. In the idle state, the state machine waits for the processor to initiate a new bus transaction.

Optimized Configuration

Figure 21 illustrates a four double-word burst read with the 28F016XS-15s and state machine configured for optimum read performance. With the SFI Configuration = 2, ADV# is held active and the counter increments at N = 2, 3 and 4, supplying the 28F016XS-15s with four consecutive accesses. Data from the initial access will be valid for transfer at N = 5. Subsequent data will be valid at N = 6, 7 and 8, improving the read wait-state performance to 3-0-0-0. All other signal monitoring and generation are identical to the reset/power-up configuration read cycle documented in the preceding section.

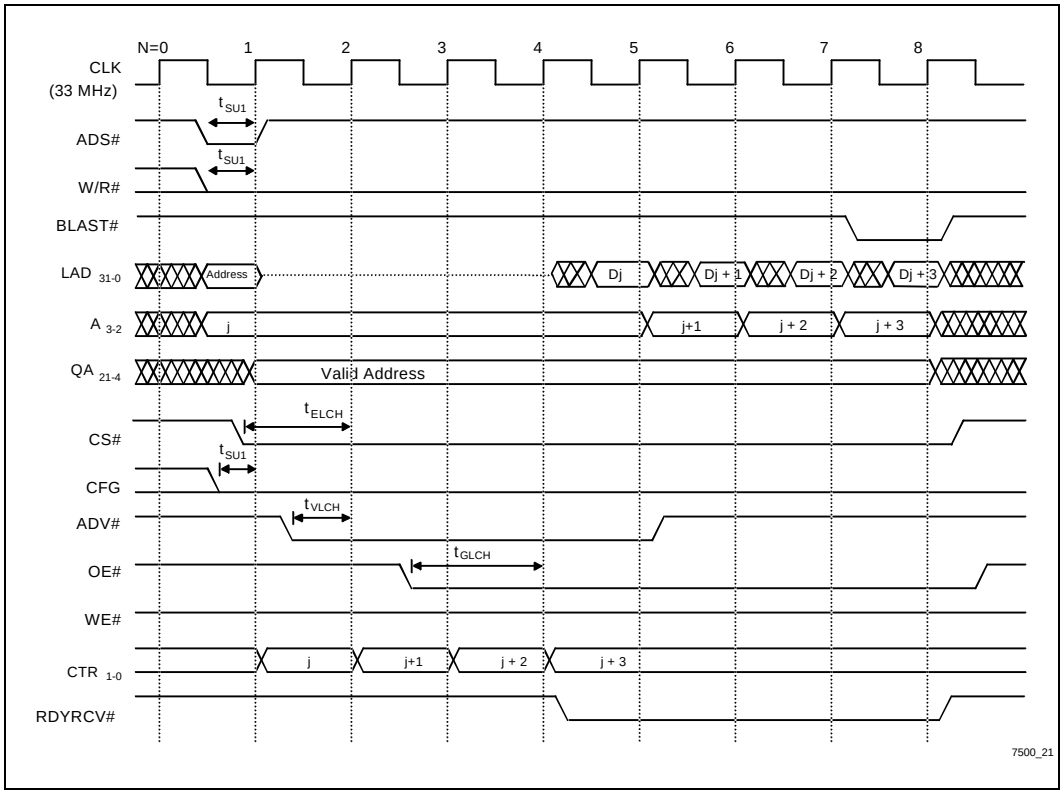


Figure 21. Example Four Double-Word Burst Read Illustrating Important Timing Parameters Requiring Consideration

Critical Timings

Table 6 describes the critical timings illustrated in Figures 20 and 21. One such critical timing is the data i960 JF hold specification, which the 28F016XS-15s meet with 0 ns margin. The 28F016XSs will hold data for 5 ns after a rising clock.

The 28F016XS-15s provide data 10 ns before the rising edge of the system clock, which satisfies the i960 JF-33 microprocessor's data input requirement.

ADV# and CTR_{1-0} are guaranteed valid 8 ns after the rising clock edge. The setup specifications for these inputs to 28F016XS-15 are each 15 ns. Since the clock period is 30 ns, this allows 7 ns margin for these timings.

RDYRCV# is guaranteed valid 8 ns after the rising clock edge, satisfying the microprocessor's setup time to rising clock edge.

Consult the appropriate datasheets for complete timing information.

Table 6. Example Write Cycle Timing Parameters at 5V V_{CC}

Part	Symbol	Parameter	Minimum Specified Value (ns)
22V10-15	t_{SU1}	Input Setup Time to CLK	9
28F016XS-15	t_{ELCH}	CE# Setup to CLK	25
	t_{VLCH}	ADV# Setup to CLK	15
	t_{AVCH}	Address Setup to CLK	15
	t_{GLCH}	OE# Setup to CLK	15

NOTE:
Consult appropriate datasheets for up-to-date specifications.

4.4 Burst Write Cycle Description at 33 MHz

The write interface for this design behaves similar to the optimized design's write interface described in Section 3.4. The only difference between the two designs is the absence of the MUX. Therefore, this design's write state machine does not have to concern itself with controlling the MUX data flow. Instead, the interface simply loads and holds the address presented by the processor for the duration of the write operation.

For further details information about this cycle and write timing waveform, refer to Section 3.4.

5.0 INTERFACING TO OTHER i960 MICROPROCESSORS

i960 CF/HA/HD/HT-16, i960 CF/HA/HD/HT-25 and i960 CF/HA/HD-33 Microprocessors

The i960 CF/HA/HD/HT microprocessor bus interfaces are compatible with the i960 CA microprocessor bus interface. Therefore, the 28F016XS-15 interfaces described in Section 2.0 for the i960 CA-33 microprocessor work equally well with these i960 micoprocessors at 25 and 33 MHz.

At 16 MHz, the interface requires a slight modification because the SFI Configuration value at 16 MHz equals 1. Therefore, the 28F016XS-15 will drive data one CLK period after initiating a read access. The interface will return READY# to the microprocessor one CLK cycle earlier as opposed to the i960 CA-33 design. Therefore, the 28F016XS-15 interface to these microprocessors, operating at 16 MHz, will deliver 2-0-0-0-1-0-0-0. . .wait-state read performance.

i960 KA and i960 KB Microprocessors

The 28F016XS interface to the i960 Kx microprocessor series will be very similar to the i960 JF interface described in Sections 3.0 and 4.0. The only difference between the two designs is the i960 Kx's lack of a BLAST# output signal. The i960 JF interfaces use this signal to determine the end to the burst transaction. Since the i960 Kx microprocessor does not have a BLAST# signal, the interface logic must examine the processor's lower address lines to determine the length of the read transaction.

For further detailed information about this interface, please reference the i960 JF interfaces. Contact your Intel or distribution sales office for schematic and PLD files for the 28F016XS interface to the i960 Kx microprocessor.

i960 SA Microprocessor, i960 SB Microprocessor

The 28F016XS's interface to the i960 Sx microprocessor series will be similar to the i960 JF microprocessor interfaces, with the following differences:

- The i960 Sx microprocessor series has a 16-bit data bus multiplexed with the lower 16 of 32 address bits. Therefore, a single 28F016XS will match the width of the data bus.
- The i960 Sx microprocessor series supports eight double-word burst transfers. Therefore, the 28F016XS interface will require a three-bit counter to generate the lower three bits of the burst addresses.

6.0 CONCLUSION

This technical paper has described the interface between the 28F016XS 16-Mbit flash memory component and the i960 microprocessor family. These designs require minimal glue logic while achieving exceptional read performance. For further information about the 28F016XS, reference the Additional Information section of this technical paper. Please contact your local Intel or distribution sales office for more information on Intel's flash memory products.

ADDITIONAL INFORMATION

Order Number	Document/Tools
297372	16-Mbit Flash Product Family User's Manual
290532	28F016XS Datasheet
297500	"Interfacing 28F016XS to the Intel486™ Microprocessor Family"
292147	AP-398, "Designing with the 28F016XS"
292146	AP-600, "Performance Benefits and Power/Energy Savings of 28F016XS Based System Designs"
292163	AP-610, "Flash Memory In-System Code and Data Update Techniques"
292165	AB-62, "Compiled Code Optimizations for Flash Memories"
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XS Benchmark Utility
Contact Intel/Distribution Sales Office	28F016XS iBIS Model
Contact Intel/Distribution Sales Office	28F016XS VHDL Model
Contact Intel/Distribution Sales Office	28F016XS Timing Designer Library File
Contact Intel/Distribution Sales Office	28F016XS Orcad and ViewLogic Schematic Symbols

REVISION HISTORY

Number	Description
001	Original Version
002	Added Optimized i960 JF Microprocessor Interface That Delivers 2-0-0-0 Wait-State Performance up to 30 MHz Removed Detailed i960 KB Microprocessor Interface Description Added i960 KB Microprocessor Interfacing Guidelines to Section 5.0, "Interfacing to Other i960 Microprocessors"
003	Added 3/5# Pin to Block Diagrams Modification made to Figure 5 in regards to recommended reset component (MAX705 changed to MAX706) Change to Figure 21, showing an optimized read at 33 MHz. Cosmetic Changes

APPENDIX A
PLD FILES

PLD file for the standard 28F016XS interface to the i960 CA Microprocessor described in Section 2.0.

```
Title           28F016XS / i960® CA Microprocessor Interface State Machine
Pattern         PDS
Revision        1
Authors         Example
Company         Intel Corporation - Folsom, California
Date            1-25-94

CHIP    STATEMACHINE    85C22V10

; inputs
PIN  1          CLK
PIN             ADS_n           ; address status - i960 CA microprocessor
PIN             W_R_n           ; W/R# - i960 CA microprocessor
PIN             BLAST_n         ; burst last - i960 CA microprocessor
PIN             CS_n            ; chip select - 28F016XS
PIN             CFG             ; 28F016XS/i960 CA microprocessor config status set input
PIN             A2              ; LAD bit 2
PIN             A3              ; LAD bit 3
PIN             RESET           ; resets all FFs in device
PIN  25         GLOBAL          ; virtual pin to implement reset

; outputs
PIN             CTR0            ; burst counter out - 28F016XS-A1
PIN             CTR1            ; burst counter out - 28F016XS-A2
PIN             /WE             ; write enable - 28F016XS
PIN             /OE             ; output enable - 28F016XS
PIN             Q0              ; state variables
PIN             Q1
PIN             /ADV            ; state variable and address valid - 28F016XS
PIN             Q3

 ; burst counter control signals
STRING  LD '(/ADS_n)'                   ; load
STRING  INC '(/ADV + ADV * Q3 * Q1 * Q0)'       ; increment

STATE  MOORE_MACHINE
DEFAULT_BRANCH S0

; state assignments
        S0 =    /Q3 * /ADV * /Q1 * /Q0
        S1 =    /Q3 *  ADV * /Q1 * /Q0
        S2 =     Q3 *  ADV * /Q1 * /Q0
        S3 =     Q3 *  ADV * /Q1 *  Q0
        S4 =    /Q3 *  ADV * /Q1 *  Q0
```

```
            S5 =   /Q3 * /ADV * /Q1 *  Q0
            S6 =   /Q3 * /ADV *  Q1 * /Q0
            S7 =    Q3 * /ADV *  Q1 * /Q0
            S8 =    Q3 * /ADV * /Q1 * /Q0

; state transitions
S0 :=    (/ADS_n * /W_R_n)     -> S1       ; READ cycle
   +     (/ADS_n * W_R_n)      -> S6       ; WRITE cycle
                              +-> S0       ; else, stay
S1 :=    (/CS_n * /CFG)          -> S5     ; 28F016XS selected, initial configurations
   +     (/CS_n * CFG)           -> S2     ; 28F016XS selected, 28F016XS and i960 CA microprocessor configured
                             +-> S0         ; else, return to idle state
S2 :=    VCC                     -> S3
S3 :=    VCC                     -> S4     ; 28F016XS is configured to wait 4 clocks
S4 :=    (/BLAST_n * ADS_n)  -> S0         ; 1 double word  read
   +     (/BLAST_n * /ADS_n) -> S1         ; pipelined read
                              +-> S5       ; else, continue
S5 :=    (/BLAST_n * ADS_n)  -> S0         ; burst read finished
  +      (/BLAST_n * /ADS_n) -> S1         ; pipelined read
                              +-> S5       ; else, continue
S6 :=    /CS_n                   -> S7     ; 28F016XS selected, continue
                             +-> S0      ; else, return to idle state
S7 :=    VCC                     -> S8
S8 :=    (BLAST_n * CFG)       -> S6       ; continue burst
   +     (BLAST_n * /CFG)      -> S8       ; pre-config write
                              +-> S0       ; write is finished

; transition outputs
S0.OUTF :=      /OE * /WE
S1.OUTF :=      /OE * /WE
S2.OUTF :=       OE * /WE
S3.OUTF :=       OE * /WE
S4.OUTF :=       OE * /WE
S5.OUTF :=       OE * /WE
S6.OUTF :=       OE * /WE
S7.OUTF :=      /OE *  WE
S8.OUTF :=      /OE *  WE

EQUATIONS
  ; implement RESET
      GLOBAL.RSTF = /RESET
  ; implement 2-bit burst counter -  registered counter equations
      CTR1 := (LD * A3) + (/LD * INC * CTR0 * /CTR1)
            + (/LD * INC * /CTR0 * CTR1) + (/LD * /INC * CTR1)
      CTR0 := (LD * A2) + (/LD * INC * /CTR0) + (/LD * /INC * CTR0)
  ; flop OE and WE on falling edge
      OE.CLKF = /CLK
      WE.CLKF = /CLK
```

PLD file for the optimized 28F016XS interface to the i960 JF Microprocessor described in Section 3.0.

```
Title           Optimized 28F016XS/i960® JF Microprocessor Interface State Machine
Pattern         PDS
Revision        1
Authors         Example
Company         Intel Corporation - Folsom, California
Date            2-16-95

CHIP        STATEMACHINE        85C22V10

; inputs
PIN   1             CLK
PIN                 ADS             ; address status - i960 JF microprocessor
PIN                 W_R             ; W/R# - i960 JF microprocessor
PIN                 BLAST           ; burst last - i960 JF microprocessor
PIN                 CS              ; chip select
PIN                 CFG             ; 28F016XS/i960 JF microprocessor config status set input
PIN                 A2              ; A bit 2
PIN                 A3              ; A bit 3
PIN                 RESET           ; resets all FFs in device
PIN   25            GLOBAL          ; virtual pin to implement reset

; outputs
PIN                 CTR0            ; burst counter out - 28F016XS-A1
PIN                 CTR1            ; burst counter out - 28F016XS-A2
PIN                 /WE             ; write enable - 28F016XS
PIN                 /OE             ; output enable - 28F016XS
PIN                 /RDYRCV         ; wait-state control
PIN                 MUX             ; control data flow through the multiplexer
PIN                 Q0              ; state variables
PIN                 Q1
PIN                 /ADV            ; state variable and address valid - 28F016XS
PIN                 Q3

 ; burst counter control signals
STRING  LD '(/ADS)'                 ; load
STRING  INC '(/ADV + /RDYRCV * Q3 * Q1 * Q0)'    ; increment

STATE MOORE_MACHINE
DEFAULT_BRANCH S0

; state assignments
            S0  =   /RDYRCV * /Q3 *  ADV * /Q1 * /Q0 * /OE * /WE * /MUX
            S1 =    /RDYRCV * /Q3 *  ADV * /Q1 *  Q0 *  OE * /WE* MUX
            S2  =   /RDYRCV * /Q3 *  ADV *  Q1 * /Q0 *  OE * /WE * MUX
            S3  =    RDYRCV * /Q3 *  ADV *  Q1 *  Q0 *  OE * /WE* MUX
            S4  =    RDYRCV * /Q3 * /ADV * /Q1 *  Q0 *  OE * /WE* MUX
            S5  =   /RDYRCV * /Q3 * /ADV *  Q1 * /Q0 * /OE * /WE* MUX
```

```
            S6  =   /RDYRCV *  Q3 *  ADV * /Q1 * /Q0 *  OE * /WE * MUX
            S7  =   /RDYRCV * /Q3 * /ADV *  Q1 *  Q0 *  OE * /WE* MUX
            S8  =   /RDYRCV *  Q3 *  ADV * /Q1 *  Q0 *  OE * /WE* MUX
            S9  =  RDYRCV *  Q3 * /ADV * /Q1 * /Q0 *  OE * /WE* MUX
            S10 =  /RDYRCV *  Q3 *  ADV *  Q1 * /Q0 *  OE * /WE* MUX
            S11 =  /RDYRCV *  Q3 * /ADV * /Q1 *  Q0 *  OE * /WE* MUX
            S12 =  /RDYRCV *  Q3 * /ADV *  Q1 * /Q0 * /OE *  WE* MUX
            S13 =  /RDYRCV *  Q3 * /ADV *  Q1 *  Q0 * /OE *  WE* MUX
            S14 =   RDYRCV *  Q3 * /ADV *  Q1 *  Q0 * /OE * /WE* MUX

; state transitions
S0 :=     (/ADS * /W_R *  CFG)  -> S1       ; READ cycle
   +      (/ADS * /W_R * /CFG) ->S5
   +      (/ADS *  W_R)          -> S13     ; WRITE cycle
                               +-> S0       ; else, stay
S1 :=      /CS                   -> S2       ; 28F016XS selected, init configurations
   +        CS                   -> S0       ; 28F016XS selected, optimized configured
S2 :=     VCC                    -> S3
S3 :=     (/BLAST)               -> S0       ; 1 double word read
                               +-> S4       ; else, continue
S4 :=     /BLAST                 -> S0       ; burst read finished
   +      (BLAST *  CFG)         -> S4       ; continue, optimized configuration
   +      (BLAST * /CFG)         -> S11      ; continue, initial configuration
S5 :=     VCC                    -> S6
S6 :=     VCC                    -> S7
S7 :=     VCC                    -> S8
S8 :=     VCC                    -> S9
S9 :=     /BLAST                 -> S0       ; BLAST -  end of the burst read transaction
   +      BLAST                  -> S10
S10:=     VCC                    -> S4
S11:=     VCC                    -> S4
S12:=     CS                     -> S0       ; write cycle control
   +      /CS                    -> S14
S13:=     VCC                    -> S15
S14:=     BLAST                  -> S13      ; BLAST - end of burst write transaction
   +      /BLAST                 -> S0

EQUATIONS
   ; implement RESET
        GLOBAL.RSTF = /RESET
   ; implement 2-bit burst counter -  registered counter equations
CTR1 := (/WR * LD * A3 * /A2) + (WR * LD * A3) + (/LD * INC * CTR0 * /CTR1)
         + (/LD * INC * /CTR0 * CTR1) + (/LD * /INC * CTR1)
CTR0 := (/WR * LD * /A2) + (WR * LD * A2) + (/LD * INC * /CTR0) + (/LD * /INC * CTR0)
```

PLD file for the standard 28F016XS interface to the i960 JF Microprocessor described in Section 4.0.

```
Title           28F016XS/i960® JF Microprocessor Interface State Machine
Pattern         PDS
Revision        1
Authors         Example
Company         Intel Corporation - Folsom, California
Date            8-16-94

CHIP        STATEMACHINE        85C22V10

; inputs
PIN    1            CLK
PIN                 ADS             ; address status - i960 JF microprocessor
PIN                 W_R             ; W/R# - i960 JF microprocessor
PIN                 BLAST           ; burst last - i960 JF microprocessor
PIN                 CS              ; chip select
PIN                 CFG             ; 28F016XS/i960 JF microprocessor config status set input
PIN                 A2              ; A bit 2
PIN                 A3              ; A bit 3
PIN                 RESET           ; resets all FFs in device
PIN   25            GLOBAL          ; virtual pin to implement reset

; outputs
PIN                 CTR0            ; burst counter out - 28F016XS-A1
PIN                 CTR1            ; burst counter out - 28F016XS-A2
PIN                 /WE             ; write enable - 28F016XS
PIN                 /OE             ; output enable - 28F016XS
PIN                 /RDYRCV         ; wait-state control
PIN                 Q0              ; state variables
PIN                 Q1
PIN                 /ADV            ; state variable and address valid - 28F016XS
PIN                 Q3

 ; burst counter control signals
STRING  LD '(/ADS)'                 ; load
STRING  INC '(/ADV + /RDYRCV * Q3 * Q1 * Q0)'    ; increment

STATE MOORE_MACHINE
DEFAULT_BRANCH S0

; state assignments
            S0  =       /RDYRCV * /Q3 * /ADV * /Q1 * /Q0 * /OE * /WE
            S1  =       /RDYRCV * /Q3 *  ADV * /Q1 * /Q0 * /OE * /WE
            S2  =       /RDYRCV * /Q3 *  ADV * /Q1 *  Q0 *  OE * /WE
            S3  =       /RDYRCV * /Q3 *  ADV *  Q1 * /Q0 *  OE * /WE
            S4  =        RDYRCV * /Q3 *  ADV *  Q1 *  Q0 *  OE * /WE
            S5  =        RDYRCV * /Q3 * /ADV * /Q1 *  Q0 *  OE * /WE
            S6  =       /RDYRCV * /Q3 * /ADV *  Q1 * /Q0 * /OE * /WE
```

```
            S7  =   /RDYRCV *  Q3 *  ADV * /Q1 * /Q0 *  OE * /WE
            S8  =   /RDYRCV * /Q3 * /ADV *  Q1 *  Q0 *  OE * /WE
            S9  =   /RDYRCV *  Q3 *  ADV * /Q1 *  Q0 *  OE * /WE
            S10 =   RDYRCV *  Q3 * /ADV * /Q1 * /Q0 *  OE * /WE
            S11 =  /RDYRCV *  Q3 *  ADV *  Q1 * /Q0 *  OE * /WE
            S12 =  /RDYRCV *  Q3 * /ADV * /Q1 *  Q0 *  OE * /WE
            S13 =  /RDYRCV *  Q3 * /ADV *  Q1 * /Q0 * /OE *  WE
            S14 =  /RDYRCV *  Q3 * /ADV *  Q1 *  Q0 * /OE *  WE
            S15 =   RDYRCV *  Q3 * /ADV *  Q1 *  Q0 * /OE * /WE

; state transitions
S0 :=    (/ADS * /W_R)          -> S1      ; READ cycle
   +     (/ADS *  W_R)          -> S13     ; WRITE cycle
                               +-> S0      ; else, stay
S1 :=    (/CS * /CFG)           -> S6      ; 28F016XS selected, init configurations
   +     (/CS * CFG)            -> S2      ; 28F016XS selected, optimized configured
                               +-> S0      ; else, return to idle state
S2 :=    VCC                    -> S3
S3 :=    VCC                    -> S4      ; 28F016XS is configured to wait 4 clocks
S4 :=    (/BLAST * ADS)         -> S0      ; 1 double word read
                               +-> S5      ; else, continue
S5 :=    /BLAST                 -> S0      ; burst read finished
   +     (BLAST *  CFG)         -> S5      ; continue, optimized configuration
   +     (BLAST * /CFG)         -> S12     ; continue, initial configuration
S6 :=    VCC                    -> S7
S7 :=    VCC                    -> S8
S8 :=    VCC                    -> S9
S9 :=    VCC                    -> S10
S10:=    /BLAST                 -> S0      ; BLAST -  end of the burst read transaction
   +     BLAST                  -> S11
S11:=    VCC                    -> S5
S12:=    VCC                    -> S5
S13:=    CS                     -> S0      ; write cycle control
   +     /CS                    -> S14
S14:=    VCC                    -> S15
S15:=    BLAST                  -> S13     ; BLAST - end of burst write transaction
   +     /BLAST                 -> S0

EQUATIONS
  ; implement RESET
      GLOBAL.RSTF = /RESET
  ; implement 2-bit burst counter -  registered counter equations
      CTR1 := (LD * A3) + (/LD * INC * CTR0 * /CTR1)
            + (/LD * INC * /CTR0 * CTR1) + (/LD * /INC * CTR1)
      CTR0 := (LD * A2) + (/LD * INC * /CTR0) + (/LD * /INC * CTR0)
```

APPENDIX B
BENCHMARK PERFORMANCE ANALYSIS

The following section provides detailed memory technology information used in the performance analysis (UDP/IP Networking and Imaging Benchmarks) contained in the introduction. The performance analysis was based on actual memory component performance in an i960 processor-based environment. System interface delay between microprocessor and memory was not included in the analysis. The two benchmarks illustrate relative system memory performance.

A. 28F016XS Flash Memory

28F016XS is capable of 3-1-1-1-1-1-1-1. . .read performance at 5.0V V_{CC} and 33 MHz or 25 MHz (2-0-0-0-0-0-0-0. . .in terms of wait-states). The benchmarking analysis is shown below:

	UDP/IP Networking Benchmark	Imaging Benchmark
	Time (sec)	*Time (sec)*
i960 KB-25 Microprocessor	1.30	1.64
i960 CA-33 Microprocessor	.89	.89
i960 CF-33 Microprocessor	.53	.59

B. 16-Mbit DRAM

16-Mbit DRAMs were, at the time this technical paper was published, only beginning to ramp into production. Only advance information for the wider x16, 16-Mbit DRAMs was available for use in the calculations that follow.

Sequential reads allow use of the DRAM fast page mode. Assumed DRAM specifications are shown below:

- 80 ns t_{RAC}, 40 ns t_{AA} (5.0V V_{CC})
- 256 word (512 byte) page buffer

Therefore, 16-Mbit DRAMs are capable of 3-2-2-2-2-2-2-2. . .read performance at 33 MHz and 25 MHz (2-1-1-1-1-1-1-1 in terms of wait-states. . .). The benchmarking analysis is shown below:

	UDP/IP Networking Benchmark	Imaging Benchmark
	Time (sec)	*Time (sec)*
i960 KB-25 Microprocessor	1.88	1.89
i960 CA-33 Microprocessor	1.06	1.03
i960 CF-33 Microprocessor	.59	.64

C. 4-Mbit EPROM

Calculations that follow used the x16 version of the 4-Mbit EPROM (Intel 27C400 or equivalent).

The assumed 5.0V V_{CC} 4-Mbit EPROM random access time is 150 ns. Therefore, 4-Mbit EPROMs are capable of 5-5-5-5-5-5-5-5. . .read performance at 5.0V V_{CC} and 33 MHz (4-4-4-4-4-4-4-4. . .in terms of wait-states). The benchmarking analysis is shown below:

	UDP/IP Networking Benchmark	Imaging Benchmark
	Time (sec)	***Time (sec)***
i960 KB-25 Microprocessor	NA	NA
i960 CA-33 Microprocessor	1.56	1.49
i960 CF-33 Microprocessor	.78	.81

D. 16-Mbit PAGED MASK ROM

Calculations that follow used the x16 version of the 16-Mbit paged mask ROM, which is not yet widely available from multiple vendors. The x8, 16-Mbit paged mask ROM is the more common version today.

Sequential reads allow use of the mask ROM page mode. The assumed 5.0V V_{CC} 16-Mbit mask ROM random access time is 150 ns, with 75 ns accesses in page mode (4-word page). Therefore, 16-Mbit mask ROMs are capable of 5-3-3-3-5-3-3-3. . .read performance at 5.0V V_{CC} and 33 MHz (4-2-2-2-4-2-2-2. . .in terms of wait-states). The benchmarking analysis is shown below:

	UDP/IP Networking Benchmark	Imaging Benchmark (sec)
	Time (sec)	***Time (sec)***
i960 KB-25 Microprocessor	NA	NA
i960 CA-33 Microprocessor	1.35	1.30
i960 CF-33 Microprocessor	.71	.73

Filename:	297500_3.DOC
Directory:	C:\TESTDOCS\DOCS
Template:	C:\WORD\ZAN____1.DOT
Title:	28F016XS / i960 Interface
Subject:	
Author:	Ken Mckee
Keywords:	
Comments:	
Creation Date:	08/28/95 10:16 AM
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