28F008S3

SPECIFICATION UPDATE

Release Date: February 1997

Order Number 297799-003

The 28F008S3 may contain design defects or errors known as errata. Characterized errata that may cause the behavior of these products to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
09/10/96	-001	Document includes all known errata to date (original version).
12/01/96	-002	Removed CE# glitch sensitivity erratum. Modified CE#-high erratum. Added RP# Control erratum.
02/01/97	-003	Removed CE#-high erratum.

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the third release of the 28F008S3 Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published. Functional descriptions for this product are found in the *Byte-Wide Smart 3 FlashFile™ Memory Family 4, 8, and 16 Mbit Datasheet*.

Affected Documents/Related Documents

Title	Order
Byte-Wide Smart 3 FlashFile™ Memory Family 4, 8, and 16 Mbit Datasheet	290598

Nomenclature

Errata are design defects or errors. These may cause the behavior of these products to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to *Byte-Wide Smart 3 FlashFile™ Memory Family 4, 8, and 16 Mbit Datasheet*. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings			Page	Status	Errata
	A-1, -3	A-6	A-8			
1	X	X	X	7	Fix	Deep Power-Down Current
2	X	X	X	8	Fix	Block Locking and Unlocking
3	X	X		9	Fixed	CE#-High Time
4	X			11	Fixed	CE# Glitch Sensitivity
5	X	X	X	13	Fix	RP# Control during Power-Up

Specification Changes

Number	Steppings			Page	Status	Specification Changes
	A-1, -3	A-6	A-8			
N/A				14		None in this Specification Update revision.

Specification Clarifications

Number	Steppings			Page	Status	Specification Clarifications
	A-1, -3	A-6	A-8			
N/A				14		None in this Specification Update revision.

Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
N/A		14		None in this Specification Update revision.

IDENTIFICATION INFORMATION

Markings

The Finished Processing Order (FPO) number correlates to a specific device stepping as illustrated in the table below:

Stepping(1,2)	Identifier
A-1,-3	Ninth digit on topside FPO mark (third line) = J, K, L, M, or N
A-6	Ninth digit on topside FPO mark (third line) = P or Q
A-8	Ninth digit on topside FPO mark (third line) = U or V

NOTE:

1. Device steppings are based on continuous updates made in manufacturing and testing of the device and represent the current material shipped.
2. A-0, -2, -4, -5, and -7 material was never sampled.

ERRATA

1. Deep Power-Down Current

PROBLEM: I_{CCD} deviates from the published specification. Please replace the existing to *Byte-Wide Smart 3 FlashFile™ Memory Family 4, 8, and 16 Mbit Datasheet* I_{CCD} specification with the following information:

Sym	Parameter	Notes	2.7V V_{CC}		3.3V V_{CC}		Unit	Test Conditions
			Typ	Max	Typ	Max		
I_{CCD}	V_{CC} Deep Power-Down Current	1		12		12	µA	RP# = GND ± 0.2V I_{OUT} (RY/BY#) = 0 mA

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).

IMPLICATION: The increased current requirements may have an impact on power supply loading or battery life.

WORKAROUND: None.

STATUS: A fix for this erratum has been identified and will be implemented in the next component stepping. Refer to Summary Table of Contents to determine the affected stepping.

AFFECTED PRODUCTS: A-1, -3, -6, and -8 steppings are affected by this erratum.

2. Block Locking and Unlocking

PROBLEM: The block locking and unlocking security feature is currently nonfunctional. Attempts to lock and unlock blocks may cause subsequent byte write and/or block erase failures. If a subsequent operation fails, a device protection error will cause the problem. The component incorrectly reads a block lock-bit as being set when it is actually cleared.

IMPLICATION: Block locking feature is disabled. This erratum effects the following commands: Set Master Lock-Bit, Set Block Lock-Bits, and Clear Block Lock-Bits.

WORKAROUND: To prevent the accentual setting and clear of block lock-bits, Intel sets the Master Lock-Bit during the test flow. This disables the ability to lock and unlock block via software only. However, blocks can still be locked and unlocked if 12V is applied to the component's RP# input. To prevent this from occurring, do not apply 12V to the RP# input.

If data security is of utmost importance, lower V_{PP} voltage equal to or less than V_{PPLK} during normal operations. With V_{PP} equal to or less V_{PPLK}, the device is protected against all data manipulation operations.

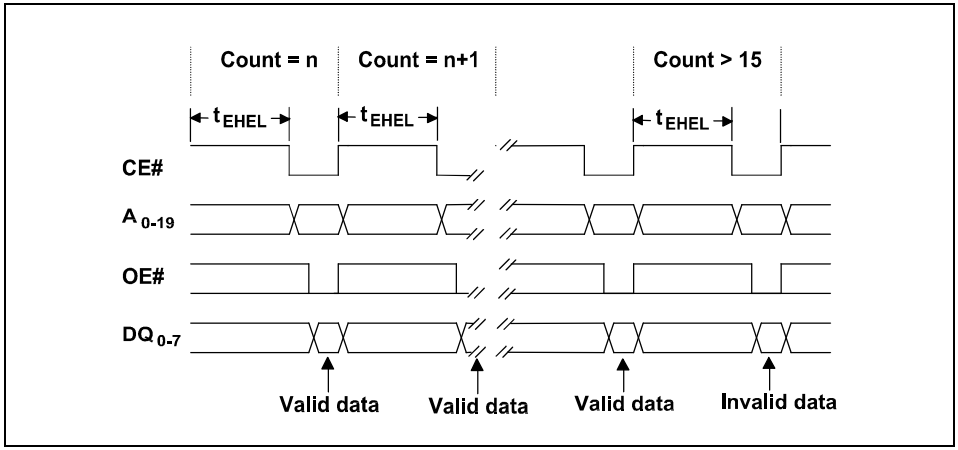
STATUS: A fix for this erratum has been identified and will be implemented in the next component stepping. Refer to Summary Table of Contents to determine the affected stepping.

AFFECTED PRODUCTS: A-1, -3, -6, and -8 steppings are affected by this erratum.

3. CE#-High Time

PROBLEM: The component may return invalid data if more than fifteen successive read operations are performed where CE# is deasserted between each read and the corresponding CE#-high pulse width resides within the specifications outlined in the table below.

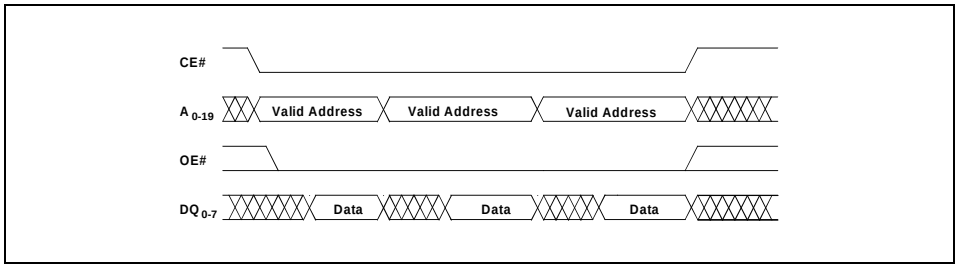
Stepping	CE#-High Pulse Width (t_{EHEL})	
	Min	Max
A-1 and -3	100 ns	40 µs
A-6	240 ns	700 ns



Successive Read Operations That Have Long CE#-High Pulse Widths

Read the implications section, which follows, to determine whether or not your design may be affected by this erratum.

IMPLICATION: The use of the flash memory will affect the exposure to this anomaly. Systems that execute code directly out of the flash memory will be less susceptible to the problem because the flash memory is continuously being accessed for information at a fast rate. If this is the case, CE# may be driven active while only the address changes to retrieve subsequent data from the component (see the figure below, *Access the Flash with CE# Active*) or the CE#-high time will be very short (less than 100 ns) to maximize read throughput. If it is determined that your applications accesses the flash memory in this manner, you will not have problem with this erratum.



Access the Flash with CE# Active

If it is determined that CE#-high time violations occur, carefully examine subsequent reads. If the ratio of good to bad (CE#-high times within the specifications outlined in the table above) reads is high, your system may not have a problem. For every bad read the system performs, five good reads for A-1 and A-3 stepping and two good reads for A-6 stepping are needed to cancel the effect of the bad read. So, carefully analyze the flash memory CE# input to understand the CE#-high characteristic.

WORKAROUND: If it is determined that your system can produce this CE#-high occurrence, here are solutions to help work around this erratum:.

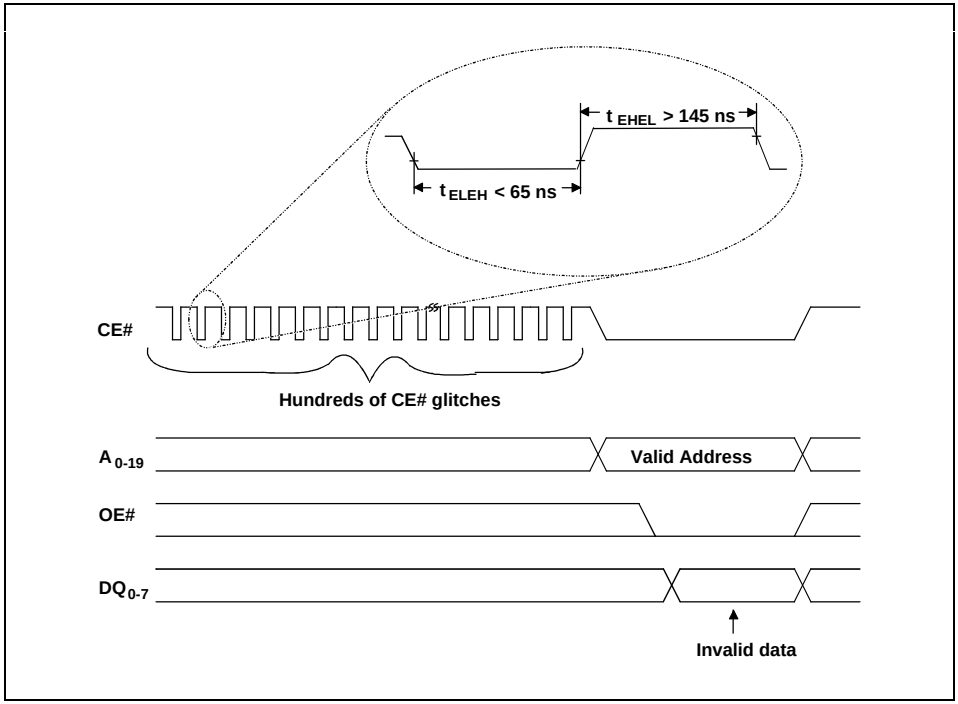
1. Read more than four good reads for A-1 and A-3 stepping and only one read for A-6 stepping during each assertion of CE#, as illustrated in the figure above.
2. Issue a Byte Write command and program FFh to any location before executing a read operation. Programming FFh will not alter stored data, but it will give the component sufficient time to prepare for the read operation.

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: A-1, -3, and -6 steppings are affected by this erratum.

4. CE# Glitch Sensitivity

PROBLEM: A noisy CE# control signal may cause an invalid read. This erroneous read only occurs after the device has received over one hundred consecutive short CE# glitches (t_{EHEL} < 65 ns) with intermittent CE#-high time (t_{EHEL}) greater than 145 ns (see the figure below, *A Long Series of CE# Glitches May Induce an Invalid Read*).



A Long Series of CE# Glitches May Induce an Invalid Read

After valid data is read, the device must receive another series of CE# glitches (typically over one hundred) to induce an invalid read. CE# glitches sequences, other than defined in the figure above, have no adverse effect.

IMPLICATION: This erratum may affect read operations in systems that have a lot of noise on the flash memory's CE# input. If CE# is generated asynchronously from the upper address lines, noise on CE# can sometimes occur when upper address lines transition from one state to another. However, applications that access flash memory sequentially will have stable upper address lines and will therefore produce fewer CE# glitches. Systems that execute code from flash memory or download code from flash memory into DRAM will usually access the device sequentially; therefore, they will be less susceptible to this erratum.

Carefully analyze the flash memory CE# input. If no glitches are seen on this signal when accessing other devices, your system does not have a problem. If glitches are detected, more in-depth system characterization is need to identify susceptibility to this erratum.

It is important to understand how these glitches manifest themselves in order to determine whether or not they will cause a problem.

1. In systems that flow unlatched addresses to CE# control logic, the decode logic may generate CE# glitches when the address bus transitions from one state to another. However, the µP/µC address switching frequency is usually very fast (somewhere in the order of 1/2 the µP/µC operating frequency) which will cause the glitches high time to be less than 145 ns. If the CE#-high time is less than 145 ns, the glitch has no effect on the component.

   Note: Most µP/µC with integrated chip select logic use latched outputs and therefore may not have CE# glitches.

2. If the address bus is not pulled up or pulled down during idle bus cycles, the address bus may be left in an undetermined state. This condition may cause CE# glitches.

WORKAROUND: If it is determined that the CE# causes a problem, possible solutions to help workaround this erratum are suggested as follows.

Hardware solution:

Add system logic to prevent CE# glitches such as latched CE# control logic or pullup/pulldown resistors to the address bus.

Software solution for data storage applications:

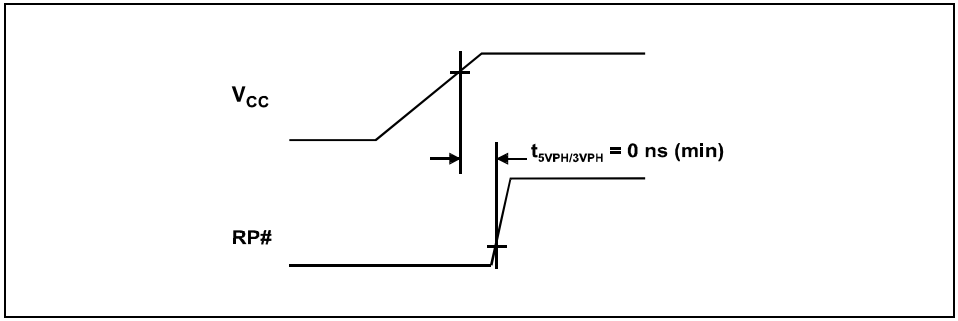
If the device receives over one hundred consecutive CE# glitches, issue a Byte Write command and program FFh to any location before executing a read operation. Programming FFh will not alter stored data, but it will give the component sufficient time to prepare for the read operation.

STATUS: This erratum has been fixed. Refer to Summary Table of Contents to determine the affected steppings.

AFFECTED PRODUCTS: A-1 and -3 steppings are affected by this erratum.

5. RP# Control during Power-Up

PROBLEM: RP# must be held low while V_{CC} ramps to a valid level during power transitions.



Hold RP# Active While V_{CC} Ramps

Holding RP# low during power-up blocks spurious write initiated by system control logic which may occur as the system voltage transitions to a stable level. Intel recommends the use of RP# for CPU/memory reset synchronization, write protection, and deep power-down mode.

IMPLICATION: This erratum only affects power-up operations. Systems that tie the flash memory's RP# input to the system RESET# signal typically will not have a problem with erratum because the RESET# signal is usually held low during the power-up sequence to properly synchronize the CPU. However, systems that ties RP# directly to V_{CC} will be more exposed to this problem. So, carefully analyze RP# during the power-up condition to fully understand its behavior.

WORKAROUND: If it is determined that this erratum may cause a problem, here is a possible workaround:

Use a simple RC delay network to hold RP# low during the power-up condition or tie the RP# input to the system RESET# signal. This workaround will eliminate your exposure to this problem and also provide your design with addition power-up security.

STATUS: A fix for this erratum has been identified and will be implemented in the next component stepping. Refer to Summary Table of Contents to determine the affected stepping.

AFFECTED PRODUCTS: A-1, -3, -6, and -8 steppings are affected by this erratum.

SPECIFICATION CHANGES

There are no specification changes in this Specification Update revision.

SPECIFICATION CLARIFICATIONS

There are no specification clarifications in this Specification Update revision.

DOCUMENTATION CHANGES

There are no documentation changes in this Specification Update revision.