28F200BV/CV
28F002BV

SPECIFICATION UPDATE

Release Date: February 1997

Order Number: 297612-004

The 28F200BV/CV and 28F002BV may contain design defects or errors known as errata. Characterized errata that may cause the 28F200BV/CV and 28F002BVs' behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333 other Countries 708-296-9333

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
04/06/95	-001	Initial release of this document. Includes the following: Reduced V_{LKO} (Automotive), t_{PHWL}/t_{PHEL} Pushout, CE# delay from RP# High, t_{PLPH} Reset Pulse Width, Erroneous Erase Fail Flag Operation, t_{PLQZ} - New Spec, V_{PP} Low Flag Operation, TTL-Level Control Signals, t_{WHEH} -CE# Timing Errata/ A_{-1} Timing Errata.
12/21/95	-002	Extensive revision of entire document: B-step information added, new Affected Material format used, Stepping Identification Information added. Errata improved for B-step: Reset Pulse Width, t_{PLPH} - New Spec. New errata: Third Write Pulse, Extended Temp Cold Programming, Low-Voltage Erase Time, Datasheet Erratum. New addenda: Input Slew Rate, Capacitance Specs, V_{CC} Ramp Time, Max Erase Times.
05/01/96	-003	This is the new format for the Specification Update document. It contains all identified errata published prior to this date. Reduced V_{LKO} (Automotive Temp) removed, since it was incorporated into datasheet. V_{CC} Ramp Time (Datasheet Clarification) rewritten.
02/03/97	-004	Reference to BE/CE (2.7V V_{CC}, extended temp) removed from this document. This device is not available.

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the fourth release of the 28F200BV/CV and 28F002BV Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*.

Affected Documents/Related Documents

Title	Order
2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet	290531

Nomenclature

Errata are design defects or errors. These may cause the 28F200BV/CV and 28F002BVs' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings		Page	Status	Errata
	A	B			
1	X		7	Fixed	t_{PHWL}/t_{PHEL} out of spec. B-step fixed.
2	X		8	Fixed	Must wait 100 ns after reset before read.
3	X		9	Fixed	Erase status flag may erroneously indicate fail.
4	X		10	Fixed	A-step production has V_{PP}-low flag disabled.
5	X		12	Fixed	TTL-levels require V_{IHMIN} = 4.0V on control pins.
6	X		13	Fixed	Write or address timing changes for A-step.
7	X	X	17	No Fix	t_{WHWL}/t_{EHEL} out of spec after 2-write sequence.
8	X	X	19	Eval	Ext temp, V_{CC} = 3.3V ± 0.3V must program within T = 0°C – +85°C.
9		X	20	Fix	Erase time and current may increase when V_{CC} = 3.3V ± 0.3V, V_{PP} = 5V ± 10%.

Specification Changes

Number	Steppings		Page	Status	Specification Changes
	A	B			
1	X	X	21	Doc	New t_{PLPH} spec defined with values for A-, B-step.
2	X	X	22	Doc	New t_{PLQZ} spec defined with values for A-, B-step.

Specification Clarifications

Number	Steppings		Page	Status	Specification Clarifications
	A	B			
1	X	X	23	Doc	Clarifies V_{CC} ramp rate requirements.

Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
1	-001	24	Doc	Input rise/fall times added to datasheet.
2	-001	24	Doc	Input/output capacitance specs added.
3	-001	25	Doc	Max block erase times added to datasheet.
4	-002/-003	25	Doc	Editing mistake in Revisions -002/-003 of datasheet.

IDENTIFICATION INFORMATION

Markings

Stepping	Identifier
A-Step Engineering Sample	1. “ES” on topside mark. 2. Ninth digit on topside FPO mark (third line) = “C”
A-Step Production	Not available: none produced.
B-Step Engineering Sample	1. “ES” on topside mark. 2. Ninth digit on topside FPO mark (third line) = “D” or “E”
B-Step Production	1. Ninth digit on topside FPO mark (third line) = “D” or “E”

ERRATA

1. t_{PHWL}/t_{PHEL} Pushout

PROBLEM: Affected material does not meet its t_{PHWL}/t_{PHEL} specification for write operations in both 3.3V and 5V V_{CC} operations. This problem has been fixed in the B-step version of the product. The erratum specifications are below:

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PHWL}/t_{PHEL}(Datasheet)	1	0.45	µs
t_{PHWL}/t_{PHEL}(A-step Erratum)	8	6	µs

The specification t_{PHWL} (RP# High Recovery to WE# Going Low) is the minimum time between the RP# signal going high to WE# going low. The specification t_{PHEL} (RP# High Recovery to CE# Going Low) is the minimum time between the RP# signal going high to CE# going low.

IMPLICATION: The erratum affects the delay from coming out of a reset until a command write can be executed on the part (affects both WE#-controlled and CE#-controlled command sequences).

WORKAROUND: Verify system timings to ensure this does not impact your design.

STATUS: This erratum has been fixed in the B-step. Refer to Summary Table of Changes to determine the affected stepping(s).

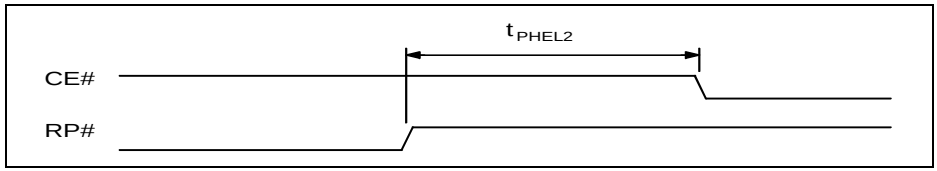
AFFECTED PRODUCTS: All A-step material is affected. B-step material is not affected. All engineering samples and A-step production units of the listed products are affected. This problem has been fixed in the B-step version of the product.

These products are affected. . .				. . .under these operating conditions		
Name	Package	Step	Marking	V_{CC}	V_{PP}	Temp
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B, AB28F200BR-T/B	All	A	Ninth digit of topside FPO mark (third line) = “C”	All	All	All

2. CE# Delay from RP# High

PROBLEM: Affected material requires a delay between coming out of reset (RP# signal going high) and beginning a read operation (CE# going low). This minimum specification must be followed to ensure valid data is read during subsequent read operations.

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PHEL2}	100	100	ns



Timing Diagram for Required Delay

IMPLICATION: Applications that do not meet the required delay may read invalid data from the device are impacted.

WORKAROUND: This timing must be followed for A-step material, but not for B-step material. Verify system timings to ensure this does not impact your design.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All A-Step material is affected. B-step material is not affected.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temperature**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B, AB28F200BR-T/B	All	A	Ninth digit of topside FPO mark (third line) = “C”	All	All	All

3. Erroneous Erase Fail Flag Operation

PROBLEM: Due to a logic timing problem, affected units may indicate a block erase error in the Status Register when, in fact, proper block erasure has occurred. The relevant bit of the Status Register is SR.5 (Erase Status), which is shaded on the diagram below. Normally, SR.5 = 1 indicates an error in block erasure, and SR.5 = 0 indicates successful block erase. If SR.5 = 0 following an erase operation, the erase operation was completed successfully. If SR.5 = 1 following an erase operation, the bit was most likely set incorrectly due to the logic timing problem.

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTE:
Please see Section 3.3.2 of the *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* for more information on Status Register operation.

IMPLICATION: Applications using the Status Register to verify successful erase will have erase failures that will affect operation.

WORKAROUND: The erase status flag (SR.5) should be ignored by masking this bit in your software. To confirm a successful block erase, read back the contents of a block to verify that all bytes contain FFH (all bits in block equal 1). Alternatively, reissue the Block Erase command until a successful erase is reported in the Status Register. Because of these limitations, block cycling for affected material should be limited to 10,000 cycles for both commercial and extended temperature ranges. Reissuing the Erase command upon an error bit counts as another block erase cycle.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All A-Step material is affected. This errata is fixed in B-step material.

These products are affected. . .				**. . .under these operating conditions**		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temperature**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B, AB28F200BR-T/B	All	A	Ninth digit of topside FPO mark (third line) = “C”	All	All	All

4. Disabled V_{PP}-Low Flag

PROBLEM: The VPPS flag in the Status Register (SR.3) has been disabled in affected products. Normally, when the VPPS flag is operational, a program or erase command initiated with V_{PP} not in range (V_{PPH1} or V_{PPH2}) will result in the erase status bit (ES = SR.5) or program status bit (DWS = SR.4) being set to "1" along with the V_{PP} status bit (VPPS = SR.3) to indicate a failed operation due to low V_{PP}. However, under this erratum, if a program or erase command is initiated with V_{PP} not in range (V_{PPH1} or V_{PPH2}), then the erase status bit (ES = SR.5) or program status bit (DWS = SR.4) will be set to "1" to indicate program or erase failure, but the V_{PP} status bit (VPPS = SR.3) will remain at "0," since the VPPS flag has been disabled.

Basically, the part will operate normally, but will not indicate when low V_{PP} is the cause of a failed program or erase operation.

The relevant bit of the Status Register is SR.3 (V_{PP} Status), which is shaded on the diagram below. Normally, SR.3 = 1 indicates an aborted operation due to V_{PP} not being switched on.

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTE:
Please see Section 3.3.2 of the *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* for more information on Status Register operation.

IMPLICATION: When an erase or program failure is experienced, the device will not indicate if low V_{PP} was the cause of the failure.

WORKAROUND: If a system design is experiencing program/erase failures under the conditions described above, issue another Erase command to complete a successful block erase. System design using the VPPS flag to detect program or erase errors should use the program and erase status bits instead.

STATUS: This erratum has been fixed in the B-step. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All A-Step material is affected. B-Step material contains a fully-operational V_{PP} low flag.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B, AB28F200BR-T/B	All	A	Ninth digit of topside FPO mark (third line) = “C”	All	All	All

5. TTL-Level Control Signals

PROBLEM: This erratum applies only to systems using TTL signal levels and V_{CC} = 5V ± 10%. If you are using CMOS inputs, this erratum does not affect your design. Due to an internal detector problem, TTL logic high level must be minimum 4.0V (instead of 2.4V) on the control pins of the device: CE#, OE#, and WE#. Standard TTL levels can continue to be used on other pins on the device. The required logic-high level is defined in the table below:

Parameter	Min	Max	Units
Input High Voltage (TTL)	4.0	V_{CC} + 0.2V	V

IMPLICATION: Applications using TTL levels will need to modify their designs to meet the higher input voltage requirements on the control signals.

WORKAROUND: This requirement must be met for proper operation of the device.

STATUS: This erratum has been fixed in B-step material. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All A-Step material using V_{CC} 5V ± 10% with TTL signal levels is affected. B-Step material is not affected.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B, AB28F200BR-T/B	All	A	Ninth digit of topside FPO mark (third line) = “C”	5V±10% (TTL levels)	All	All

6. Write Timing Erratum/Address Timing Erratum

PROBLEM: Due to logic timing problems, modifications in write or address timing are required. Two possible workarounds exist: errata A and B. Refer to the following table to determine the operating which applies to your operation conditions. Where the table says, “One of A or B,” one of either erratum A **or** B is necessary for proper functionality. Where it says, “A,” only erratum A is needed. “Not Affected” means that this erratum does not effect that operation condition.

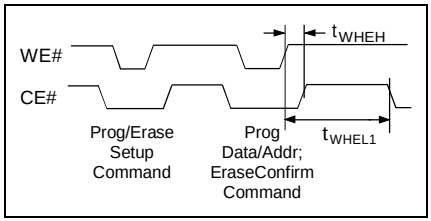
	x8-Mode Operation		x16-Mode Operation	
	V_{PP} = 5V ± 10%	**V_{PP} = 12V ± 5%**	**V_{PP} = 5V ± 10%**	**V_{PP} = 12V ± 5%**
V_{CC} = 3.3 ± 0.3V	One of A or B	A	Not Affected	A
V_{CC} = 5V ± 10%	One of A or B	One of A or B	Not Affected	Not Affected

IMPLICATION: Applications operating in an affected mode must implement the applicable workaround for proper operation.

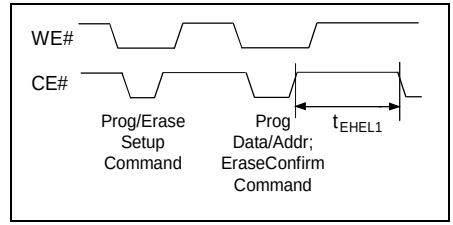
WORKAROUND:

A. t_{WHEH}- CE# Timing Erratum

Due to a logic timing problem, new timing restrictions may be necessary between the WE# and CE# signals during write operations. The timing waveforms and specifications are shown below:



Timing Waveform for WE#-Controlled Writes



Timing Waveform for CE#-Controlled Writes

Affected Parameters for WE#-Controlled Writes

Symbol	Parameter	Datasheet		Errata		Units
		Min	Max	Min	Max	
t_{WHEH}	CE# Hold Time from WE# High	0	no spec	0	5	ns
t_{WHEL1}	CE# Pulse Width High from WE# High	no spec	no spec	110		ns

NOTE:
Erratum timing for t_{WHEL1}, given above, is required only after the second WE# pulse in a WE# controlled write sequence.

Basically, these new errata specifications for WE#-controlled writes require the system timing to:

1. Take CE# to logic high no earlier than WE# goes high and no later than 5 ns after WE# goes high.
2. Hold CE# high for at least 110 ns, starting from the time WE# goes high.

Affected Parameters for CE#-Controlled Writes

Symbol	Parameter	Datasheet		Errata		Units
		Min	Max	Min	Max	
t_{EHEL1}	CE# Pulse Width High from WE# or CE# High, whichever occurs last	20	no spec	110		ns

NOTE:
The erratum timing for t_{EHEL1}, given above, is required only after the second CE# pulse in a CE# controlled write sequence.

A system can also use the alternative CE#-controlled writes with the specifications given in the datasheet with the addition of t_{EHEL1},which must have a pulse width of 110 ns, as shown above.

These timing specifications must be met for proper operation of the device. The flash memory chip select must go inactive within 5 ns of a program/erase operation and remain inactive for a period of 110 ns before going active again. Consider the following options for meeting the t_{WHEL1} or t_{EHEL1} requirement :

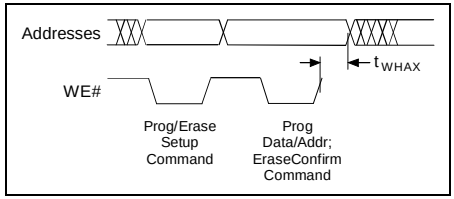
1. Follow a program/erase two-write sequence with an access to another memory so as not to decode the flash memory chip select for the required period of time.
2. Insert one or more no-op commands following a program/erase two-write sequence, again to ensure the flash memory chip select is disabled for the required period of time.

Depending on your system implementation, the t_{WHEH} requirement may require additional logic to ensure the required t_{WHEH} timing. Evaluate your system timing to ensure the new write requirements can be met. This erratum has been fixed in B-step material.

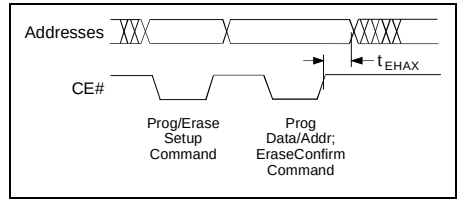
B. Address Timing Erratum

Due to a logic timing problem, new timing restrictions may be necessary on the lowest order address pin. This pin is the A_{-1} address pin for 28F200 products in x8-mode and the A_{10} address pin for 28F002 x8-only products. The timing waveforms and specifications are shown below:

Product	Affected Pin
28F200	A_{-1} (in x8 Mode)
28F002	A_{10}



Timing Waveform for WE#-Controlled Writes



Timing Waveform for CE#-Controlled Writes

Affected Parameters for WE#-Controlled Writes

Symbol	Parameter	Datasheet		Erratum		Unit
		Min	Max	Min	Max	
t_{WHAX}	Address Hold Time from WE# High (unaffected pins)	10				ns
	Address Hold Time from WE# High (affected pin: A_{-1} for 28F200 in x8, A_{10} for 28F002)	10		40		ns

Affected Parameters for CE#-Controlled Writes

Symbol	Parameter	Datasheet		Erratum		Unit
		Min	Max	Min	Max	
t_{EHAX}	Address Hold Time from CE# High (unaffected pins)	10				ns
	Address Hold Time from CE# High (affected pin: A_{-1} for 28F200 in x8, A_{10} for 28F002)	10		40		ns

This new erratum specification requires the system timing in x8-mode to hold the affected address pin valid for 40 ns from the time WE# goes high (for WE#-controlled writes) or from the time CE# goes high (for CE#-controlled writes).

These timing specifications must be met for proper operation of the device. Additional logic may be needed to meet these requirements.

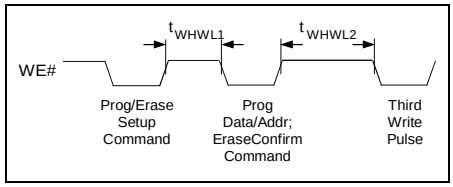
STATUS: This erratum has been fixed in B-step material. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All A-Step material is affected, depending on operating mode (see table in description). B-Step material is not affected. Refer to Summary Table of Changes to determine the affected stepping(s).

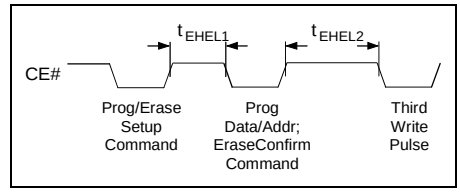
These products are affected. . .				**. . .under these operating conditions**		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B, AB28F200BR-T/B	All	A	Ninth digit of topside FPO mark (third line) = “C”	All	All	All

7. Third Write-Pulse t_{WHWL}/t_{EHEL} Specification Erratum

PROBLEM: This erratum affects designs issuing program or erase commands to the flash device with V_{CC} = 3.3 ± 0.3V. Operation with V_{CC} = 5V ± 10% is not affected. The program and erase functions are initiated using a two-write sequence, with the program or erase setup command being written to the part, then the data program or erase confirm being written on the next cycle after a time t_{WHWL1} (t_{EHEL1} for CE#-controlled writes) between the write low pulses. Following the second write in a two-write sequence; the WE# (CE#) signal must stay high for 35 ns before going low again for a third write pulse, shown as the t_{WHWL2} (t_{EHEL2}) on the right in the below. The value of t_{WHWL1} (t_{EHEL1}) between the first and second write in the sequence remains at its datasheet specification. The specified and erratum values are shown in the table which follows.



Timing Waveform Showing Two t_{WHWL} Specifications



Timing Waveform Showing Two t_{EHEL} Specifications

	Product	BV–60		BV–80/BV–120		
	V_{CC}	3.3 ± 0.3V				
	Load	50 pF				
Parameter		**Spec**	**Errata**	**Spec**	**Errata**	**Units**
t_{WHWL2} (min, third write only)		20	40	30	40	ns
t_{EHEL2} (min, third write only)		20	40	30	40	ns

IMPLICATION: Violating the errata conditions described in this erratum can cause the Write State Machine to abort the program or erase operation in progress and report a successfully completed operation in the Status Register, although in reality, the operation has not completed successfully.

WORKAROUND: Note, however, that even without this erratum, it is not useful for the system to write to the flash device after a program sequence until the Status Register reports that the program operation has completed, since the State Machine is designed to ignore all instructions while a program operation is in progress. Writing the Status Register read command to the device is not necessary since the device defaults to

outputting Status Register data while the program operation is in progress. In the case of an erase operation, the only valid command that should be written to the device while an erase operation is in progress is the erase suspend command. In this situation, the system must wait for the erratum value of t_{WHWL2} (t_{EHEL2}) before requesting an erase suspend.

STATUS: This is a permanent change. No fix is planned.

AFFECTED PRODUCTS: All A- and B-step materials are affected when operating at 3.3 ± 0.3V V_{CC}.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B	All	A, B	Ninth digit of topside FPO mark (third line) = “A” or “C” or “D” or “E”	3.3 ± 0.3V	All	All

8. Extended Temperature Programming Limitations

PROBLEM: Affected material has the following limitations on operating parameters:

Parameter	Min	Max	Unit
Extended Temperature Range (Program only)	0	+85	°C

Because on-chip program circuitry is sensitive to very low temp operation, this material must be programmed within the temperature range of 0°C to +85°C. Read and erase operation is unaffected over the full extended temperature operating range (–40°C to +85°C).

IMPLICATION: This erratum limits the temperature range over which affected material can be programmed.

WORKAROUND: Contact your Intel representative for workaround information.

STATUS: A fix for this errata is being evaluated. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: All A and B-step material is affected when operating at 3.3 ± 0.3V V_{CC} and programming at –40°C to 0°C.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B	All	A, B	Ninth digit of topside FPO mark (third line) = “A” or “C” or “D” or “E”	3.3 ± 0.3V	All	-40°C to 0°C (program)

NOTE:
Products using commercial temperature, or not programming over this temperature range are not affected.

9. Low-Voltage Erase Time/Current Erratum

PROBLEM: Block erase times for affected material may intermittently exceed erase time and I_{PPE} current specifications when operating with V_{CC} = 3.3 ± 0.3V and V_{PP} = 5V ± 10% over specified cycling limits. Typical erase times are not affected. The increased erase time and I_{PPE} erase current only occur together and do not occur independently of each other. The errata erase times and currents are given in the tables below:

Errata Erase Times (V_{CC} = 3.3 ± 0.3V, V_{PP} = 5V ± 10%

Parameter	DS Spec	Errata	Unit
Maximum Block Erase Time (Boot/Parameter)	7	20	s
Maximum Block Erase Time (Main)	14	20	s

Errata I_{PPE} Specification (V_{CC} = 3.3 ± 0.3V, V_{PP} = 5V ± 10%

Parameter	DS Spec	Errata	Unit
I_{PPE} (max, during errata occurrence only)	30	40	mA

IMPLICATION: Applications operating under the affected conditions may intermittently see longer than normal erase times, accompanied by increased erase current.

WORKAROUND: Ensure that system operation is not affected by errata parameters.

STATUS: A fix is planned. This errata will be updated to identify fixed material when it becomes available. Refer to Summary Table of Changes to determine the affected stepping(s).

AFFECTED PRODUCTS: Some B-step material is affected when erasing at V_{CC} = 3.3 ± 0.3V and V_{PP} = 5V ± 10%.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F002BV-T/B, PA28F200BV-T/B, E28F200CV-T/B, E28F200BV-T/B, TE28F002BV-T/B, TB28F200BV-T/B, TE28F200CV-T/B, TE28F200BV-T/B	All	B	Ninth digit of topside FPO mark (third line) = "D"	3. 3± 0.3V	5V ± 10%	All

NOTE:
Designs not using B-step material or the 3V V_{CC} / 5V V_{PP} voltage combination are not affected. All B-step units of the listed products that meet the application and marking criteria are affected. A-step is not affected.

SPECIFICATION CHANGES

1. New t_{PLPH} Specification Definition and Values

DESCRIPTION:

This item defines a new specification that will be added to the datasheet. This specification is t_{PLPH} and is defined as the minimum time that RP# must be held low in order to produce a valid reset of the device.

The first data row of the table below lists t_{PLPH} values for A-step material and the second data row lists t_{PLPH} values for B-step material.

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PLPH} (Reset Pulse Width) **A-Step**	250	250	ns
t_{PLPH} (Reset Pulse Width) **B-Step**	150	60	ns

Timing Diagram for t_{PLPH} Specification

IMPLICATION: Systems that are not asserting the reset signal low longer than t_{PLPH} may not be properly resetting the flash component.

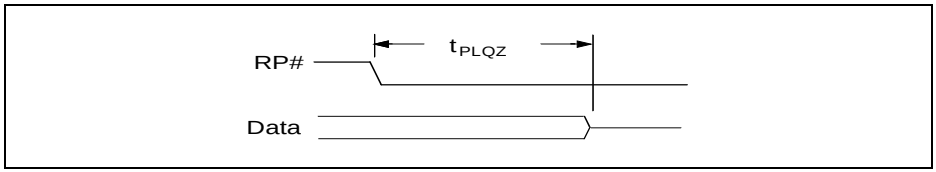
AFFECTED PRODUCTS: While both A-step and B-step material are affected, note that the parameter values for t_{PLPH} are different between A-step and B-step. Reference the identification information for clarification on distinguishing between steppings.

2. New t_{PLQZ} Specification Definition and Values

PROBLEM: This item defines a new specification that will be added to the datasheet. This specification is t_{PLQZ}, and is defined as the maximum time after RP# goes to logic low until the flash data pins go to high-impedance state. The first data row of the table below lists t_{PLQZ} values for A-step material and the second data row lists t_{PLQZ} values for B-step material (typical output loads).

AC Characteristics: Read Only Operations

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PLQZ} (RP# Low to Output High Z) **A-step**	250	250	ns
t_{PLQZ} (RP# Low to Output High Z) **B-step**	150	60	ns



Timing Diagram for t_{PLQZ} Specification

IMPLICATION: Because the flash requires a time t_{PLQZ} after reset goes low until the data pins go to high-impedance, systems that do not meet this specification may have problems with bus contention.

AFFECTED PRODUCTS: While both A-step and B-step material are affected, note that the parameter values for t_{PLQZ} are different between A-step and B-step. Reference the identification information for clarification on distinguishing between steppings.

SPECIFICATION CLARIFICATIONS

1. V_{CC} Ramp Time Clarification

PROBLEM: The *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* (Order 290531-001 and 290531-002, Sections 5.1 and 6.1) specifies timings for V_{CC} voltage switching. As defined in these datasheets, these timing specs, t_{5VPH} and t_{3VPH}, require RP# to be held low during a V_{CC} ramp until 2 µs after V_{CC} has stabilized above its minimum voltage specification. Because this requirement may be difficult to meet in a system design, this datasheet clarification defines new guidelines for V_{CC} ramp-up and changes. Basically, the specs require a delay of 2 µs only when the V_{CC} ramp at a rate faster than 1V/100 µs, and define the delay time between V_{CC} reaching V_{CCMIN} and the first device operation. These specs are no longer tied to the operation of the RP# pin. However, RP# = GND during power-up is still recommended to protect against spurious write signals between V_{LKO} and V_{CCMIN}. The new requirement is summarized in the table below:

V_{CC} Ramp Rate	Required Timing
≤ 1V/100 µs	No delay required.
> 1V/100 µs	A delay time of 2 µs is required before any device operation is initiated, including read operations, command writes, program operations, and erase operations. The delayis measured beginning from the time V_{CC} reaches V_{CCMIN} (3.0V for 3.3V operation and 4.5V for 5V operation).

NOTE:

1. These requirements must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3V and 5.0V operation, the system should first transition V_{CC} from the existing voltage range to GND, and then to the new voltage. Any time the V_{CC} supply drops below V_{LKO}, the chip will be reset, aborting any operations pending or in progress.
3. These guidelines must be followed for any V_{CC} transition from GND.

DOCUMENTATION CHANGES

1. Input Slew Rate

ITEM: Two figure notes were inadvertently left out of the initial release of the *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* (order 290531-001) for the affected products. The notes describe test conditions and specify that input signal rise and fall times (from 10% to 90%) must be less than 10 ns. The table below contains the missing notes and to which figure numbers they apply. Please evaluate possible impact on system designs. These notes will have been added to the next revision of the datasheet.

Figure Number	Text of Missing Note
13, 23	AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic 1 and V_{OL} (0.45 V_{TTL}) for a logic 0. Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.
15, 25	AC test inputs are driven at 3.0V for a logic 1 and 0.0V for a logic 0. Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

2. Capacitance Specifications

ITEM: This addendum adds the capacitance values in the table below to the datasheets for the affected material. Please evaluate possible impact on system designs. These notes will be added to the next revision of the datasheet.

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	10	12	pF	V_{OUT} = 0V

NOTE:
Sampled, not 100% tested.

3. Max Erase Time Specifications

ITEM: This addendum adds the maximum erase time values in the table below to the datasheets for the affected material. Previously, only typical numbers were given in the datasheet. This information will be added to the next revision of the datasheet.

Block Erase Timings (Commercial and Extended Temperature)

	V_{PP}	5V ± 10%				12V ± 5%				
	V_{CC}	3.3 ± 0.3V		5V ± 10%		3.3 ± 0.3V		5V ± 10%		
Parameter		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Boot/Parameter Block Erase Time		0.84	7	0.8	7	0.44	7	0.34	7	s
Main Block Erase Time		2.4	14	1.9	14	1.3	14	1.1	14	s

NOTES:

1. Max erase times are specified under worst case conditions. The max erase times are tested at the same value independent of V_{CC} and V_{PP}. See Note 2 for typical conditions.
2. Typical conditions are +25°C with V_{CC} and V_{PP} at the center of the specified voltage range. Production programming using V_{CC} = 5.0V, V_{PP} = 12.0V typically results in a 60% reduction in programming time.

4. Datasheet Erratum (WP# Description)

ITEM: Revisions -002 and -003 of the *2-Mbit (128K x 16, 256K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* contain an editing error in the pin description for the WP# pin (Section 1.5, Table 2). The error is in the last “NOTE” paragraph of that description. The sentence, “This pin is not available on the 44-lead PSOP package,” is not applicable to the 4-Meg product and should not be there. (This was an accidental carry-over from the *8-Mbit (512K x 16,1024 x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*.) The corrected paragraph will read: “**NOTE:** This feature is overridden and the boot block unlocked when RP# is at V_{HH}. See Section 3.4 for details on write protection.”

This erratum will be corrected in the next revision of the datasheet.