28F016SV
SPECIFICATION UPDATE

Release Date: February 1997

Order Number 297554-009

The 28F016SV may contain design defects or errors known as errata. Characterized errata that may cause the 28F016SV's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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Germany 44-0-1793-421-333 other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
10/24/94	-001	Document includes all known errata to date (Original Version)
01/23/95	-002	Added: Device Revision Codes 01H and 02H. V_{CC} Deep Power-Down Current Queueable Operation Delay after Power-Up and Exit from Sleep, Power-Down, or Reset WE# and CE_X# Pulse Width High Requirements after Issuing Queueable Commands Completion with Command Error Indication and Invalid Device Operations WP# Control V_{PP} Read Current Deleted: Status Register Reads Updated: AC Characteristics for WE# and CE_X#-Controlled Page Buffer Write Operations Erase Interruptability Obsoleted: Non-Serviced Erase Suspend Command
02/22/95	-003	Added: Device Revision Code 03H 3.3V V_{CC} AC Read Characteristics Page Buffer Programming at 5V V_{PP} Deleted: Updating Global Status Register Bits 0 and 1 Active Current Consumption during Sleep Mode V_{PP} Read Current BYTE# Level during Deep Power-Down Mode Word/Byte Write Performance Obsoleted: WP# Control Page Buffer Programming at 5V V_{PP} Erase Interruptability

REVISION HISTORY, Continued

Date of Revision	Version	Description
06/28/95	-004	Added: Device Revision Code 04H 3.3V V_{CC} Requirement for Optimal Power Savings Voltage and Temperature Tolerance Requirements for Program/Erase Operations at 3.3V V_{CC}/5V V_{PP} RP# Input Level Control CE#–Controlled Page Buffer Write Operations at 3.3V V_{CC} Non-Serviced Block Erase with Stuck Block Status Register Topside Package Markings Deleted: Power-Up and Reset Timings Updated: V_{CC} Standby and Deep Power-Down Currents Obsoleted: 3.3V V_{CC} Requirement for Optimal Power Savings Non-Serviced Erase with Stuck Block Status Register
05/01/96	-005	This is the new Specification Update document. It contains all identified errata published prior to this date.
7/11/96	-006	Added: Device Revision Code 05H CE#-Controlled Write Operations Specification Change for Deep Power-Down Current Specification Change for Erase Suspend Current Specification Change for WE#-Controlled Write Operations Updated: 3.3V V_{CC} AC Read Specifications Obsoleted: V_{CC} Read Current V_{CC} Standby and Deep Power-Down Currents Voltage and Temperature Tolerance Requirement for Program/Erase Operation at 3.3V V_{CC}/5V V_{PP} RP# Input Level Control at 5V V_{CC} WE# and CE_X# Pulse Width High Requirement after Issuing Queueable Commands Queueable Operation Delay after Power-Up and Exit from Sleep, Power-Down, or Reset AC Characteristics for WE# and CE_X#-Controlled Page Buffer Write Operations Completion with Command Error Indication and Invalid Device Operations CE_X#-Controlled Page Buffer Write Operations at 3.3V V_{CC}
11/11/96	-007	Updated: Device Version Number Device Version Number and FPO Number Relationship Table
11/15/96	-008	Added: Extended Temperature 3.3V Vcc CE#-Controlled Write Operation.

REVISION HISTORY, Continued

Date of Revision	Version	Description
02/01/97	-009	Updated: 3.3V Vcc AC Read Specifications

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the ninth release of the 28F016SV Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet*.

Affected Documents/Related Documents

Title	Order
28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet	290528
16-Mbit Flash Product Family User's Manual	297372

Nomenclature

Errata are design defects or errors. These may cause the 28F016SV's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet.* Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Device Version Numbers							Page	Status	Errata
	00	01	02	03	04	05	06			
1	X	X	X	X	X	X		10	Fixed	V_{CC} Read Current
2	X	X	X	X	X	X		11	Doc	V_{CC} Standby and Deep Power-Down Currents
3	X	X	X	X				12	Fixed	3.3V V_{CC} Requirement for Optimal Power Savings
4	X	X	X	X	X	X		13	Fixed	Voltage and Temperature Tolerance Requirements for Program/Erase Operations at 3.3V V_{CC}/5V V_{PP}
5	X	X	X	X	X	X		14	Fixed	RP# Input Level Control at 5V V_{CC}
6	X	X	X	X	X	X		14	Doc	3.3V V_{CC} AC Read Specifications
7	X	X	X	X	X	X		15	Fixed	WE# and CE_X# Pulse Width High Requirements after Issuing Queueable Commands
8	X	X	X	X	X	X		16	Fixed	Queueable Operation Delay after Power-Up and Exit from Sleep, Power-Down, or Reset
9	X	X	X	X	X	X		18	Fixed	AC Characteristics for WE# and CE_X#-Controlled Page Buffer Write Operations
10	X	X	X	X	X	X		19	Fixed	Completion with Command Error Indication and Invalid Device Operations
11	X	X	X	X	X	X		23	Fixed	CE#–Controlled Page Buffer Write Operations at 3.3V V_{CC}
12	X							23	Fixed	Non-Serviced Erase Suspend Command
13	X	X		X				27	Fixed	Non-Serviced Block Erase with Stuck Block Status Register
14	X	X	X					27	Fixed	Erase Interruptability
15	X	X	X					28	Fixed	WP# Control
16	X							28	Fixed	Page Buffer Programming at 5V V_{PP}
17	X	X	X					29	Fixed	Topside Package Marking

Specification Changes

No.	Device Version Number							Page	Status	Spec Change
	00	01	02	03	04	05	06			
1							X	30	Doc	Deep Power-Down Current
2							X	31	Doc	Erase Suspend Current
3							X	31	Doc	AC Characteristic for WE#-Controlled Page-Buffer Write at 3.3V
4							X	32	Doc	3.3V V_{CC} AC Read Specifications
5							X	33	Doc	CE#-Controlled Write Operations
6							X	34	Doc	Extended Temperature CE#-Controlled Write Operations

Specification Clarifications

Number	Device Version Number							Page	Status	Errata
								35		None in this Specification Update revision.

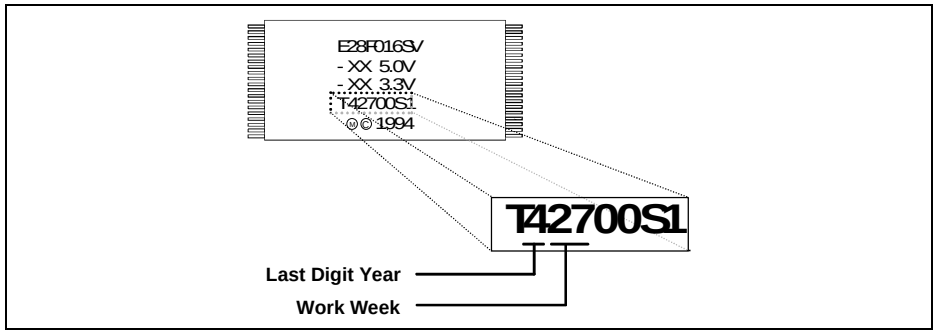
Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
		35		None in this Specification Update revision.

IDENTIFICATION INFORMATION

Markings

The Finished Processing Order (FPO) number identifies the device's testing date. The FPO number correlates to a specific a Device Version Number, as illustrated below:



FPO Number Location and Clarification

Device Version Number and FPO Number Relationship to Specific Component Stepping

Stepping	Device Revision Code[1]	FPO Number	
		Work Week	Year
A-0	00H	≤34	1994
A-1	01H	≥35[2]	1994
	02H	≥01	1995
	03H	≥14	1995
	04H	≥27	1995
A-2	05H	≥31	1995
A-4	05H	≥09	1996
B-1	06H	≥28	1996

NOTES:

1. Device Revision Codes are based on continuous improvements made in manufacturing and testing of the device and represent the current material shipped.
2. Components with FPO numbers U4460065 and U4470032 are from the A-0 Stepping. They are **not** A-1 material, as the Work Week indicates.

ERRATA

1. V_{CC} Read Currents

PROBLEM: The V_{CC} read (I_{CCR}) currents exceed the maximum specification values published in the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet*. The maximum specifications for I_{CCR} are changed to the following values.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Symbol	Parameter	Max Spec	Max New	Test Conditions
$I_{CCR}1$	V_{CC} Word/Byte Read Current	50 mA	60 mA	f = 8 MHz
$I_{CCR}2$	V_{CC} Word/Byte Read Current	30 mA	40 mA	f = 4 MHz

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C

Symbol	Parameter	Max Spec	Max New	Test Conditions
$I_{CCR}1$	V_{CC} Word/Byte Read Current	95 mA	135 mA	f = 10 MHz
$I_{CCR}2$	V_{CC} Word/Byte Read Current	55 mA	90 mA	f = 5 MHz

IMPLICATION: The increased current specifications may impact power supply loading or battery life.

WORKAROUND: Ensure that system power supply and/or battery is sufficient to meet the increased current requirements.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

2. V_{CC} Standby and Deep Power-Down Currents

PROBLEM: The V_{CC} standby (I_{CCS}) and deep power-down (I_{CCD}) currents exceed the maximum specification values published in the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet*.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{CCS}	V_{CC} Standby Current	130 µA	350 µA(1) 130 µA(2)	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	350 µA(1) 10 µA(2)	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Max	Max New	Test Conditions
I_{CCS}	V_{CC} Standby Current	130 µA	350 µA(1) 130 µA(2)	V_{CC} = V_{CC} Max, CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	350 µA(1) 10 µA(2)	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

NOTES:
1. These specification values apply to components with a Device Revision Code of 00H.
2. These specification values apply to components with Device Revision Codes 01H, 02H, 03H, 04H and 05H.

Upon entering standby and/or deep power-down mode(s), a current surge with a peak amplitude of 200 µA may occur for a duration of up to 30 seconds. This surge will only happen at most once while in one of these two modes. These errata only affect components listed in the Affected Products section.

Please note that the Reset functionality of the RP# pin is preserved, and it should still be used for the following purposes:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

IMPLICATION: The increased current specifications may impact power supply loading or battery life.

WORKAROUND: Ensure that system power supply and/or battery is sufficient to meet the increased current requirements.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, and 04H are affected. (04H eliminates the possibility of a deep power-down current surge). Note that I_{CCS} specifications have returned to datasheet values and I_{CCD} current specifications have been increased for devices with Device Version Numbers 01H, 02H, 03H, 04H, and 05H.

3. 3.3V V_{CC} Requirement for Optimal Power Savings

PROBLEM: When operating at 3.3V V_{CC}, the read voltage (V_{CC}) must ramp to 3.2V or greater (maximum voltage 3.6V) to achieve the published standby current (I_{CCS}) specifications. Once the read voltage crosses this voltage threshold, the V_{CC} tolerance requirement returns to the datasheet specification of 3.3V ± 0.3V.

IMPLICATION: If the read voltage (V_{CC}) does not ramp to 3.2V or greater (maximum voltage 3.6V), the increased current consumption may impact power supply loading or battery life.

WORKAROUND: Ramp the read voltage (V_{CC}) to 3.2V or greater (maximum voltage 3.6V) during power-up.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H and 04H are affected.

4. V_{PP} Voltage Tolerance Requirement for Program/Erase Operations at 3.3V V_{CC}

PROBLEM: When programming or erasing data at 3.3V V_{CC} and 5V V_{PP}, the program voltage (V_{PP}) is restricted to 5V ± 0.25V (5%). Additionally, when programming from the page buffer, V_{CC} is restricted (to 3.3V ± 0.15V) and the operating temperature must be between 30°C and 70°C. The table below summarizes the affected commands and associated operating conditions.

3.3V V_{CC}/5V V_{PP} Tolerance for Program/Erase Operations

Affected Commands	V_{CC}	V_{PP}	T_A (Operating Temp.)
Word/Byte Write (40H) Alternate Word/Byte Write (10H) Two-Byte Write (FBH) Block Erase (20H) Erase All Unlocked Blocks (A7H) Lock Block (77H)	3.3V ± 0.3V	5V ± 0.25V	0°C – 70°C
Page Buffer Write to Flash (0CH)	3.3V ± 0.15V	5V ± 0.25V	30°C – 70°C

Note that this erratum only affects systems operating at 3.3V V_{CC}/5V V_{PP}.

IMPLICATION: V_{PP} voltage restriction when programming or erasing data at 3.3V V_{CC} and 5V V_{PP}.

WORKAROUND: Restrict programming voltage to 5V ± 0.25V when programming or erasing data at 3.3V V_{CC} and 5V V_{PP}

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

5. RP# Input Level Control at 5V V_{CC}

PROBLEM: The device's RP# input pin must be driven to a minimum V_{IH} voltage of 3.0V when operating at 5V V_{CC}. Therefore, system RP# control logic, if implemented, must drive V_{OH} greater than 3.0V. If such logic is not employed, RP# should be tied to V_{CC} ± 0.2V.

IMPLICATION: Failure to drive RP# to 3.0V could cause the device to stay in reset.

WORKAROUND: When operation at 5V V_{CC}, drive the device's RP# input pin to a minimum V_{IH} voltage of 3.0V.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

6. 3.3V V_{CC} AC Read Characteristics

PROBLEM: The AC Read Specifications that deviate from the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* are shown below. Note that these specification changes only affect systems operating at 3.3V V_{CC}.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions		28F016SV-075			
Symbol	**Parameter**	**Min Spec**	**Min New**	**Max Spec**	**Max New**
t_{AVAV}	Read Cycle Time	75 ns	85 ns		
t_{AVQV}	Address to Output Delay			75 ns	85 ns
t_{ELQV}	CE# to Output Delay			75 ns	85 ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay			75 ns	85 ns

For components with Device Revision Number 05H, this erratum only affects page buffer read operations. All other reads (i.e., array, status register, and intelligent identifier reads) adhere to the specifications listed in the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet*.

IMPLICATION: AC read specifications are impacted.

WORKAROUND: Adhere to modified AC read specifications.

STATUS: Plans to fix this erratum are under evaluation. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H (only page buffer reads) are affected.

7. WE# & CEX# Pulse Width High Requirements after Issuing Queueable Commands

PROBLEM: The WE# and CE_X# pulse width high requirements that deviate from the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* are shown below. Note that the t_{WHWL} and t_{EHEL} specification changes only apply when writing to the device immediately following the completion of issuing a queueable command (see the *16-Mbit Flash Product Family User's Manual*, Section 11-1 for a list of queueable commands).

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions		28F016SV-075	
Symbol	**Parameter**	**Min Spec**	**Min New**
t_{WHWL}	WE# Pulse Width High	15 ns	45 ns(1)
t_{EHEL}	CE# Pulse Width High	15 ns	45 ns(1)

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016SV-065		28F016SV-070	
		V_{CC} ± 10%			28F016SV-070	
Symbol	**Parameter**		**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{WHWL}	WE# Pulse Width High		15 ns	30 ns(1)	15 ns(2)	30 ns(1)
t_{EHEL}	CE# Pulse Width High		15 ns	30 ns(1)	15 ns(2)	30 ns(1)

NOTES:

1. These new specification values only apply when writing to the device immediately following the completion of issuing a queueable command.
2. Applies to V_{CC} ± 10%, 100 pF load, TTL I/O levels corresponding to devices with order code E28F016SV-065. (See the *Device Nomenclature and Ordering Information* section of the device datasheet for more information.)

IMPLICATION: Issuing of queueable commands.

WORKAROUND: Adhere to modified AC write specifications when performing command queuing.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

8. Queueable Operation Delay after Power-Up and Exit from Power-Down or Reset

PROBLEM: With the program/erase voltage (V_{PP}) at 5V, the internal V_{PP} detector may not stabilize for up to 5 µs (illustrated by t_1 in the figure, *Queueable Operation Delay after Power-Up and Exit from Sleep, Power-Down, or Reset*, which follows) after RP# transitions inactive (high). This causes an invalid V_{PP} Level bit indication when reading the Block Status Registers and termination of program, erase or lock block operations due to invalid device V_{PP} error detection. Affected operations include Word/Byte Write (40H/10H), Single Block Erase (20H), Erase All Unlocked Blocks (A7H), Two-Byte Write (FBH), Page Buffer Write to Flash (0CH), and Lock Block (77H).

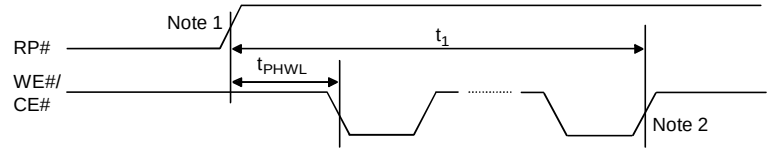
Note that this erratum only affects systems operating at 5V V_{PP}.

IMPLICATION: 5V V_{PP} power-up/reset time delay to first program or erase operation.

WORKAROUND: Upon reset, power-up, or wake-up from software sleep or hardware deep power-down, allow 5 µs (t_1) before initiating a Write/Erase command (as listed earlier) or reading the V_{PP} Level bit of the Block Status Registers (BSR.1). The figure below illustrates this timing requirement (t_1) in more detail.

Operations are initiated by the device on the rising (trailing) edge of the last WE#/CE# pulse in the command sequence. For example, when performing WE#-Controlled Writes, two-cycle command operations such as word/byte write or erase are initiated on the rising edge of the WE# pulse corresponding to the Address/Data or Confirm command.

(Three-cycle command operations are initiated on the rising edge of the third WE# pulse.) Similarly, when performing CE#-Controlled Writes, operations are initiated on the last rising CE# edge of the command sequence.



NOTES:

1. This rising edge of RP# also corresponds to the time at which the device wakes-up from software sleep mode.
2. This rising edge of WE#/CE# represents the completion of the command sequence—i.e., the time at which the command is latched into the WSM and the internal automation is initiated.

Queueable Operation Delay after Power-Up and Exit from Sleep, Power-Down, or Reset

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

9. AC Characteristics for WE#— and CE_X#—Controlled Page Buffer Write Operations

PROBLEM: The AC Characteristics for WE#– and CE#–Controlled Page Buffer Write Operations that deviate from the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* are shown below. Note that these specification changes only affect writes to the page buffer.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions		28F016SV-075		28F016SV-120	
Symbol	**Parameter**	**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{AVWL}	Address Setup to WE# Going Low	0 ns	25 ns	0 ns	25 ns
t_{AVEL}	Address Setup to CE# Going Low	0 ns	25 ns	0 ns	25 ns

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%		28F016SV-065		28F016SV-070			
		V_{CC} ± 10%				28F016SV-070		28F016SV-080	
Symbol	**Parameter**			**Min Spec**	**Min New**	**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{AVWL}	Address Setup to WE# Going Low			0 ns	15 ns	0 ns	15 ns	0 ns	15 ns
t_{AVEL}	Address Setup to CE# Going Low			0 ns	15 ns	0 ns	15 ns	0 ns	15 ns

IMPLICATION: Page buffer write operations are affected.

WORKAROUND: When writing to the page buffer, adhere to the modified AC write specifications.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, and 05H are affected.

10. Completion with Command Error Indication and Invalid Device Operations

PROBLEM: Systems in which software, after initiating device automation via a queueable command sequence, writes another command(s) to the device before automation completes may initiate unintended device operations.

IMPLICATION: Designs that could encounter this condition include the following (dependent on the specific Device Revision Code):

Device Revision Code	Design Condition
00H, 01H	Systems that use the command queuing capability.
00H, 01H	Systems that poll for automation completion using the Extended Status Registers (thereby writing the Read Extended Status Register command after initiating automation).
00H, 01H	Systems that write the "Read Compatible Status Register" command after initiating device automation and before reading the Compatible Status Register. (This command is actually unnecessary as the device, after receiving queueable commands or command sequences, automatically transitions to a mode where it outputs Compatible Status Register data when read.)
00H, 01H	Systems that use the software Sleep and/or Abort commands.
00H, 01H	Systems that use the Erase Suspend command.
00H, 01H, 02H, 03H, & 04H	Systems that use Page Buffer programming.

These unintended operations can produce an invalid command error indication in components with Device Revision Codes 00H and 01H. A command error is indicated by a "1" in the following Status Register bits:

Compatible Status Register Bit 5: Erase Status

Bit 4: Data-Write Status

Global Status Register Bit 5: Device Operation Status

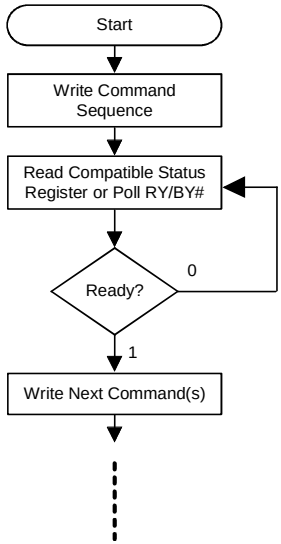
Block Status Register (Block 0) Bit 5: Block Operation Status

In addition, the unintended device operation can initiate inadvertent program or erase attempts to Block 0 in systems which use the Sequential/Single Load to Page Buffer Commands (74H and E0H, respectively). Data alteration can only occur if Block 0 is not locked and V_{PP} equals V_{PPH}. Components with Device Revision Codes 00H, 01H, 02H, 03H, and 04H may exhibit this phenomenon.

WORKAROUND: The following options listed below outline possible corrective actions required to avoid this errata. (Any one of the options will eliminate this errata.)

Option 1: Polling for "Ready" Indication

Systems that poll the RY/BY# pin or WSMS bit (CSR.7) for "Ready" indication before writing another command to the device will not encounter this errata. This is illustrated in the *Example System Software Flowchart, etc.* figure below, and flowcharts 11-1 and 11-2 (without erase suspend) of the *16-Mbit Flash Product Family User's Manual.*



NOTE:

System software does not write the Read Compatible Status Register command before reading status register data.

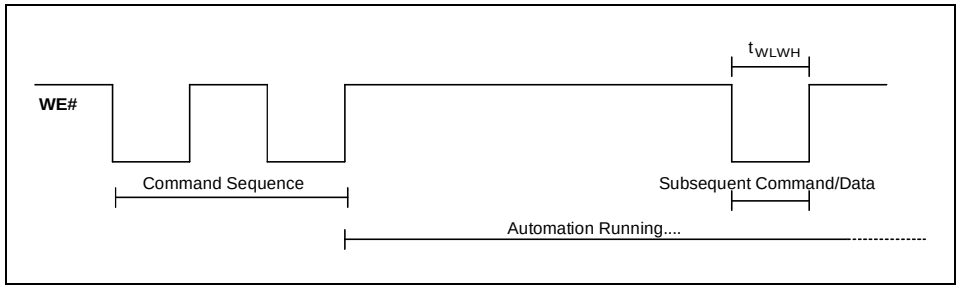
Example System Software Flowchart That Will Not Encounter "Completion with Command Error or Invalid Device Operation" Condition

Option 2: WE# and CE# Pulse Width Restrictions

For WE#-Controlled Write Operations, a WE# pulse width defined by the ranges of parameter t_{WLWH} in the table below, will result in a system that does not exhibit this errata (note: timings are also bounded by specifications in the device datasheet). When performing CE#-Controlled Write Operations, this restriction equally applies to the CE# pulse width (t_{ELEH}).

WE# and CE# Specifications That Will Not Cause the "Completion with Command Error or Invalid Device Operation" Condition

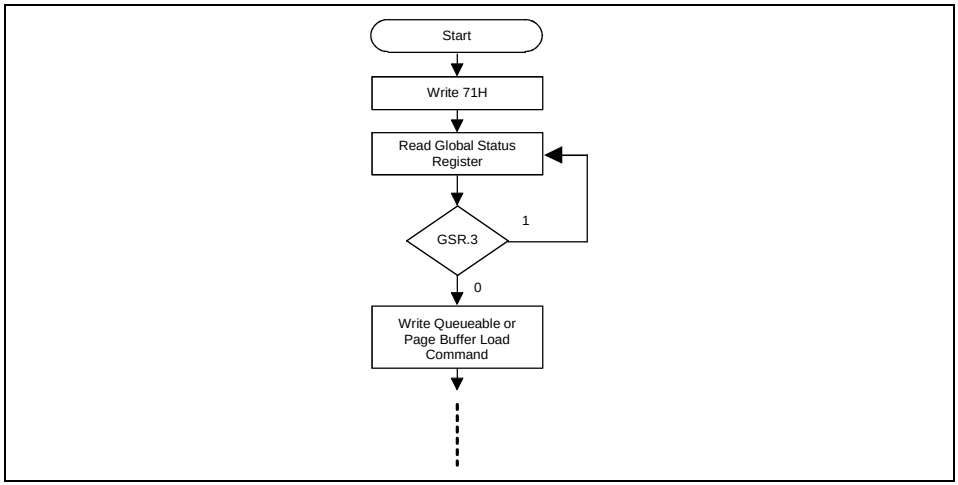
V_{CC} Supply Voltage	t_{WLWH}	t_{ELEH}
5V	<75 ns	<75 ns
3.3V	<100 ns	<100 ns



Timing Waveform Showing Specification Ranges That Will Not Cause the "Completion with Command Error or Invalid Device Operation" Condition

Option 3: Checking Command Queue Availability before Writing to a Page Buffer (Applicable **only** to components with Device Revision Codes 02H, 03H and 04H)

Before writing Sequential (E0H) or Single (74H) Load to Page Buffer command sequences, poll the QS bit (GSR.3) to determine queue availability. If the queue is available, system software can write a Page Buffer Load command sequence to the device, as shown in the *Example System Software Flowchart, etc.* figure below. This is analogous to the procedure outlined in Chapter 11 of the *16-Mbit Flash Product Family User's Manual* for issuing queueable commands.



Example System Software Flowchart That Will Not Encounter "Invalid Device Operation" Condition through Checking Queue Status
(ONLY VALID FOR COMPONENTS WITH DEVICE REVISION CODE 02H, 03H and 04H)

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 00H, 01H, 02H, 03H, 04H, and 05H are affected.

11. CE#–Controlled Page Buffer Write Operations at 3.3V V_{CC}

PROBLEM: CE#–Controlled Page Buffer Write operations at 3.3V V_{CC} are not functional.

IMPLICATION: This erratum affects the Single/Sequential Load to Page Buffer (75H/E0H) commands. Note that this erratum only affects systems operating at 3.3V V_{CC}.

WORKAROUND: When operating at 3.3V V_{CC}, use WE-Controlled Page Buffer Write operations.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 00H, 01H, 02H, 03H, 04H, and 05H are affected.

12. Non-Serviced Erase Suspend Command

PROBLEM: If an Erase Suspend command is issued late in the Erase algorithm, it will not be recognized by 28F016SV components listed in the Affected Devices section, and erase will complete. This Erase Suspend command will **not** be discarded.

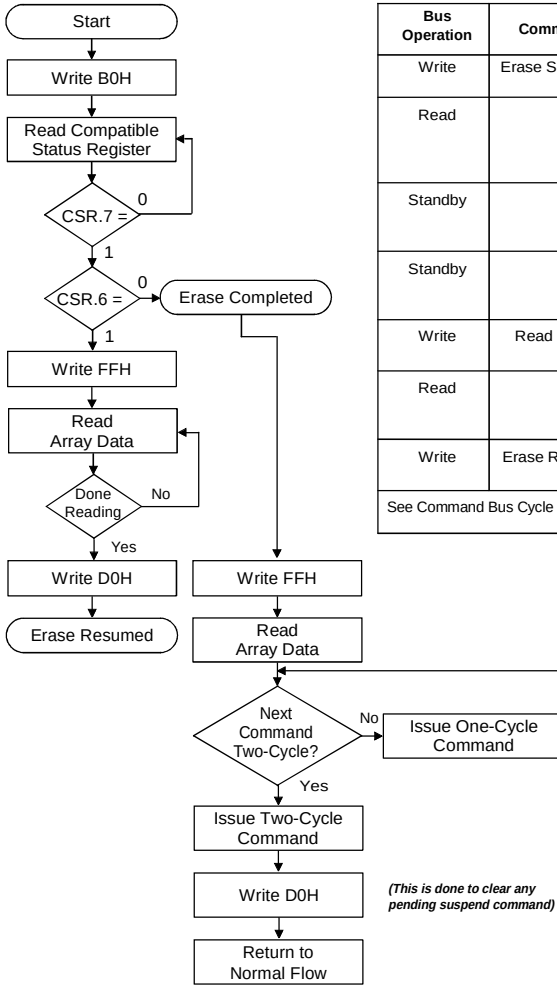
IMPLICATION: The following conditions are affected by this unserviced Suspend command:

A. If another Erase command is issued at some time later, the device then assumes that the pending Suspend request is still valid and will automatically Suspend the current Erase.

B. If any queueable command is in the command queue waiting for execution while another queueable command is in progress, the Write State Machine will suspend its operation after completing the current command. (Refer to the *16-Mbit Flash Product Family User's Manual*, Section 11-1 for the queueable command list.)

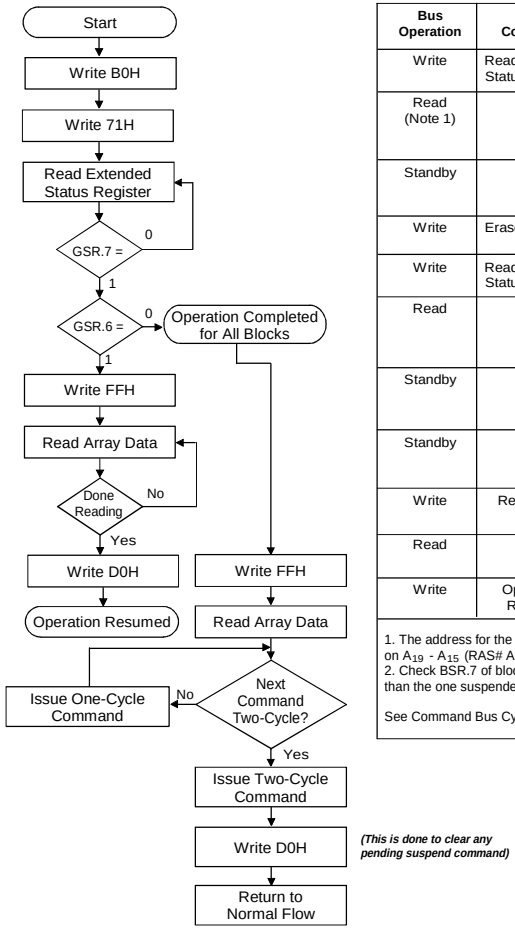
Note that the device will not service the Suspend command if it is powered-down (RP# transitioning low) prior to either condition A or B.

WORKAROUND: A software workaround to this erratum inserts a redundant Resume command (D0H) immediately following any Two-Cycle Command (Word Write, Block Erase, Lock Block, or Upload Status Bits) in the Erase Suspend flowcharts. Modified Erase Suspend to Read Array flowcharts (Figures 11-3 and 11-12 of *the 16-Mbit Flash Memory Product Family User's Manual*) detailing this workaround are shown in the following figures, *Erase Suspend to Read Array with Compatible Status Register and Erase Suspend to Read Array with Extended Status Register*. This erratum results in the *Erase Suspend with Compatible Status Register* flowchart being incompatible with the 28F008SA *Erase Suspend* flowchart.



Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X
Read		Q = CSRD Toggle RAS#, CAS# or OE# to Update CSRD A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A = X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X
See Command Bus Cycle notes for description of codes.		

Erase Suspend to Read Array with Compatible Status Register



Bus Operation	Command	Comments
Write	Read Extended Status Register	D = 71H A = X

Read (Note 1)		Q = BSRD
		Toggle RAS#, CAS # or OE# to Update BSRD.
		A = 1H

Standby		Check BSR.7 1 = Block Ready 0 = Block Busy
Write	Erase Suspend	D = B0H A = X
Write	Read Extended Status Register	D = 71H A = X

Read		Q = GSRD
		Toggle RAS#, CAS # or OE# to Update GSRD.
		A = 2H

Standby		Check GSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check GSR.6 1 = Operation Suspended 0 = Operation Completed
Write	Read Array	D = FFH A = X
Read		Q = AD A = AA
Write	Operation Resume	D = D0H A = X

1. The address for the desired BSR to be read must be supplied on A_{19} - A_{15} (RAS# Address A_9 - A_5).
2. Check BSR.7 of block to be read. This should be a block other than the one suspended, or queued for an operation.

See Command Bus Cycle notes for description of codes.

Erase Suspend to Read Array with Extended Status Register

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Number 00H are affected.

13. Non-Serviced Block Erase with Stuck Block Status Register

PROBLEM: If software polls the BS bit of the Block Status Register for block erase completion (BSR.7 = 1) and immediately issues a subsequent block erase command sequence before the WSMS bit of the Compatible Status Register or Global Status Register indicate "Ready" (CSR.7/GSR.7 = 1), the device may not service the subsequent erase operation. This scenario also causes the BS bit of the subsequent block to remain in the "Busy" state (BSR.7 = 0).

IMPLICATION: Block erase operations may be left unserviced.

WORKAROUND: To avoid this erratum, system software should poll CSR.7 (as shown in Figure 11-2 of the *16-Mbit Flash Product Family User's Manual*) or GSR.7, instead of BSR.7, to determine the completion of a block erase operation before issuing subsequent block erase commands.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H and 03H are affected.

14. Erase Interruptability

PROBLEM: The following 28F016SV features are affected:

A. Write during Erase: Queuing a Write command when an Erase command is in progress

B. Queuing Multiple Block Erase Commands

IMPLICATION: Systems that need to queue multiple block erase commands or systems that need to queue a write during erase.

WORKAROUND: Do not attempt to send another queueable command if an Erase command is in the queue or in progress (see the *16-Mbit Flash Product Family User's Manual* queueable commands list, Section 11-1). However, an Erase Suspend or a Sleep command can still be issued while an Erase is in progress.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 00H, 01H and 02H are affected.

15. WP# Control

PROBLEM: Block erase can prematurely terminate as the result of software Abort commands, hardware RP# activation or V_{CC} transition outside of the normal operating range. In these non-standard scenarios, there exists a small probability that the block's lock-bit will become set, locking the block if WP# is active.

IMPLICATION: Systems may inadvertently lock blocks. The system will not be able to write or erase locked blocks while WP# is held low.

WORKAROUND: System software can detect premature termination of block erase by executing the Upload Status command on device power-up. If both BSR.5 and GSR.5 are set, indicating premature block erase termination, the system should re-attempt erase with WP# inactive.

System hardware should be designed to either control WP# (both active and inactive levels must be supported) or should set WP# inactive at all times. Setting WP# always-active (i.e., connecting it to GND) is not recommended as this configuration will not enable recovery from inadvertent lock during premature block erase termination.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 00H, 01H and 02H are affected.

16. Page Buffer Programming at 5V V_{PP}

DESCRIPTION: With V_{PP} at 5V, page buffer programming operations may incorrectly program the high byte of each word to the flash array.

IMPACT: This erratum affects the Page Buffer Write to Flash (0CH) Command in systems operating at 5V V_{PP}.

WORKAROUND: In 5V V_{PP} environments use Word/Byte Write or Two-Byte Write command. Note that page buffer programming operations at 12V V_{PP} function correctly for all devices.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Code 00H are affected.

17. Topside Package Marking

PROBLEM: The 28F016SV's topside package marking for 3.3V V_{CC} operation incorrectly indicated an access speed of 85 ns prior to Work Week 20, 1995 (see the Identification Information section). All devices produced after Work Week 20, 1995 show an access speed of 75 ns, reflecting the true datasheet specification. As such, this marking error only affects components listed in the Affected Products section.

IMPLICATION: Invalid 3.3V access speed specified on package.

WORKAROUND: Disregard 3.3V access speed topside marking for 28F016SV packages. Adhere to datasheet specifications.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 00H, 01H, and 02H (prior to Work Week 20, 1995) are affected.

SPECIFICATION CHANGES

1. Deep Power-Down Currents

PROBLEM: The deep power-down (I_{CCD}) current specification is changed to 10 µA. This change will be integrated into the next the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* revision.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	10 µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Max	Max New	Test Conditions
I_{CCD}	V_{CC} Deep Power-Down Current	5 µA	10 µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V

Please note that the Reset functionality of the RP# pin is preserved, and it should still be used for the following purposes:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

AFFECTED PRODUCTS: All components.

2. V_{PP} Erase-Suspend Current

PROBLEM: The V_{PP} erase-suspend (I_{PPES}) current specification is changed to 200 µA. This change will be integrated into the next *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* revision.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# Pin Set High for 3.3V Operations

Symbol	Parameter	Max Spec	Max New	Test Conditions
I_{PPES}	V_{PP} Erase Suspend Current	50 µA	200 µA	V_{PP} = V_{PPH1} or V_{PPH2} Block Erase in Progress

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C
3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Max	Max New	Test Conditions
I_{PPES}	V_{PP} Erase-Suspend Current	50 µA	200 µA	V_{PP} = V_{PPH1} or V_{PPH2} Block Erase in Progress

AFFECTED PRODUCTS: All components.

3. AC Characteristic for WE#-Controlled Page-Buffer Write at 3.3V

PROBLEM: The CE# setup to WE# going low timing specification is changed to 10 ns. This change will be integrated into the next *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* revision.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Symbol	Parameter	Max Spec	Max New	Test Conditions
t_{ELWL}	CE# Setup to WE# Going Low	0 ns	10 ns	

AFFECTED PRODUCTS: All components are affected.

4. 3.3V V_{CC} AC Read Characteristics

PROBLEM: The AC Read Specifications that deviate from the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* are shown below. Note that these specification changes only affect systems operating at 3.3V V_{CC}.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions		28F016SV-075			
Symbol	**Parameter**	**Min Spec**	**Min New**	**Max Spec**	**Max New**
t_{AVAV}	Read Cycle Time	75 ns	85 ns		
t_{AVQV}	Address to Output Delay			75 ns	85 ns
t_{ELQV}	CE# to Output Delay			75 ns	85 ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay			75 ns	85 ns

For components with Device Revision Number 06H, this erratum only affects page buffer read operations. All other reads (i.e., array, status register, and intelligent identifier reads) adhere to the specifications listed in the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet*.

IMPLICATION: AC read specifications are impacted.

WORKAROUND: Adhere to modified AC read specifications.

STATUS:. This will remain a permanent specification change on future device revisions Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 00H, 01H, 02H, 03H, 04H, 05H, and 06H (Page Buffer Only) are affected.

5. CE_X#—Controlled Write Operations

PROBLEM: The AC Characteristics for CE_X#–Controlled Write Operations that deviate from the *28F016SV 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet* are shown below.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions		28F016SV-075	
Symbol	**Parameter**	**Min Spec**	**Min New**
t_{ELEH}	CE# Pulse Width	60 ns	65 ns

V_{CC} = 5V ± 0.5V, 5V ± 0.25V, T_A = 0°C to +70°C

Versions		V_{CC} ± 5%	28F016SV-065(1)		28F016SV-070(1)	
		V_{CC} ± 10%			28F016SV-070(2)	
Symbol	**Parameter**		**Min Spec**	**Min New**	**Min Spec**	**Min New**
t_{ELEH}	CE# Pulse Width		40 ns	45 ns	40(1) ns, 45(2) ns	45(1) ns, 50(2)ns
t_{EHEL}	CE# Pulse Width High		15 ns	15 ns	30(1) ns, 15(2) ns	15(1,2) ns

NOTES:
1. See the high speed AC Input/Output Reference Waveforms and AC Testing Load Circuit.
2. See the standard AC Input/Output Reference Waveforms and AC Testing Load Circuit.

IMPLICATION: CE_X#-Controlled write operations are affected.

WORKAROUND: When writing to flash memory using CE_X#-Controller write operations, adhere to the modified AC write specifications else, implement WE#-Controlled writes.

STATUS:. This will remain a permanent specification change on future device revisions Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 06H are affected.

6. Extended Temperature. CE_X#—Controlled Page Buffer Write Operations

PROBLEM: Systems using the DT28F016SV (Extended Temperature 28F016SV) implementing CE_x# controlled page buffer write operations in the 3.3V V_{CC} operating range, must limit V_{CC} to within 5% of 3.3V.

IMPLICATION: CE_X#-Controlled page buffer write operations at 3.3V V_{CC} are affected.

WORKAROUND: When writing to flash memory using CE_X#-controlled page buffer write operations at 3.3V V_{CC}, adhere to a 5% V_{CC} tolerance else, implement WE#-Controlled writes or non-page buffer CE# controlled writes.

STATUS: This will remain a permanent specification change on future device revisions. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Version Numbers 06H are affected.

SPECIFICATION CLARIFICATIONS

There are no specification clarifications in this Specification Update revision.

DOCUMENTATION CHANGES

There are no documentation changes in this Specification Update revision.